Monolithic Pixel Detectors for high-precision tracking in HI experiments

L. Musa - CERN

International Conference on Science and Technology for FAIR in Europe
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Monolithic Pixel Sensors for high-precision tracking in HI experiments

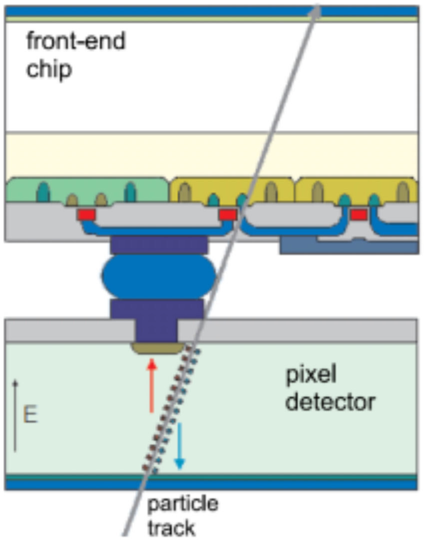
OUTLINE

- Pixel Detectors in HEP
- Going beyond the performance of current Hybrid Pixel Detectors
- CMOS Pixel Sensors
- Use of CPS in HI experiments: STAR HFT, CBM MVD, ALICE ITS Upgrade

Disclaimer: this is not a review of Monolithic Pixel Detectors, but rather focuses on CMOS Pixel Sensors in HI experiments

The world of Silicon Pixel Detectors

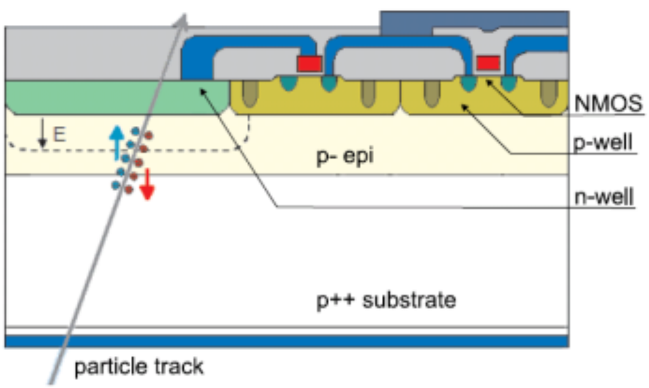
Hybrid Pixel Detector



N. Wermes (Univ. of Bonn)

- Sensor based on silicon junction detectors produced in a planar process
- High resistivity wafers (few kW•cm) with diameters of 4” – 6”
- Specialized producers (~10 world wide) ➔ **high cost**
- Readout Chip: ASIC - CMOS sub-micron technology
- (**Costly**) Interconnect technology based on flip-chip bonding

Monolithic Pixel Detector



N. Wermes (Univ. of Bonn)

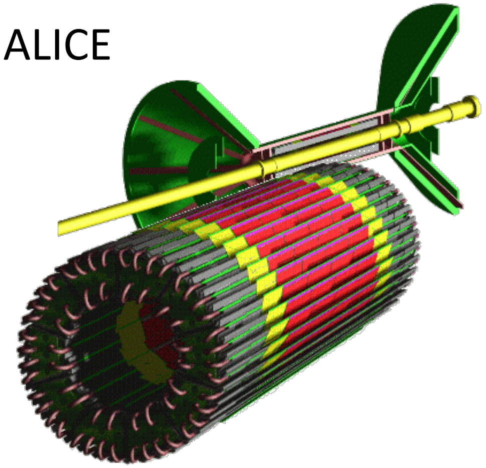
- Charge generation volume integrated into the ASIC
- Exist in many different flavours: CCDs, CMOS MAPS, HV/HR CMOS, DEPFET, SOI, …
- This talk will focus on CMOS Monolithic Active Pixel Sensors (CMOS MAPS) = CMOS Pixel Sensors (CPS)
  - **Standard industrial CMOS process**
  - **Thin, high granularity**

Pixel Detectors in HEP Experiments

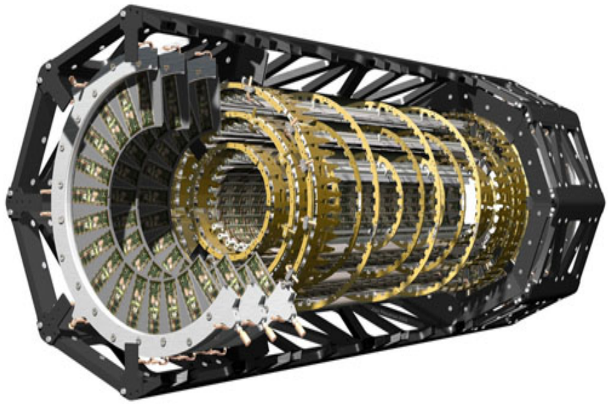
Hybrid Pixel Detectors at the hart of the LHC Experiments

Different sensor technologies, designs, operating condition

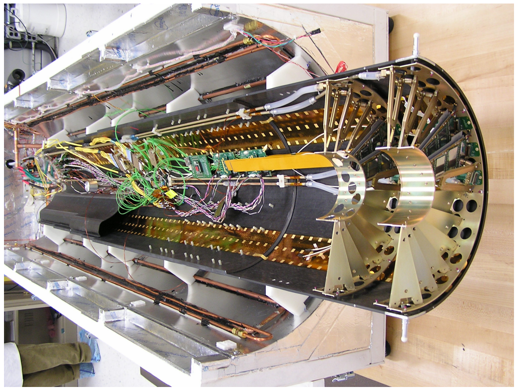
ALICE



ATLAS



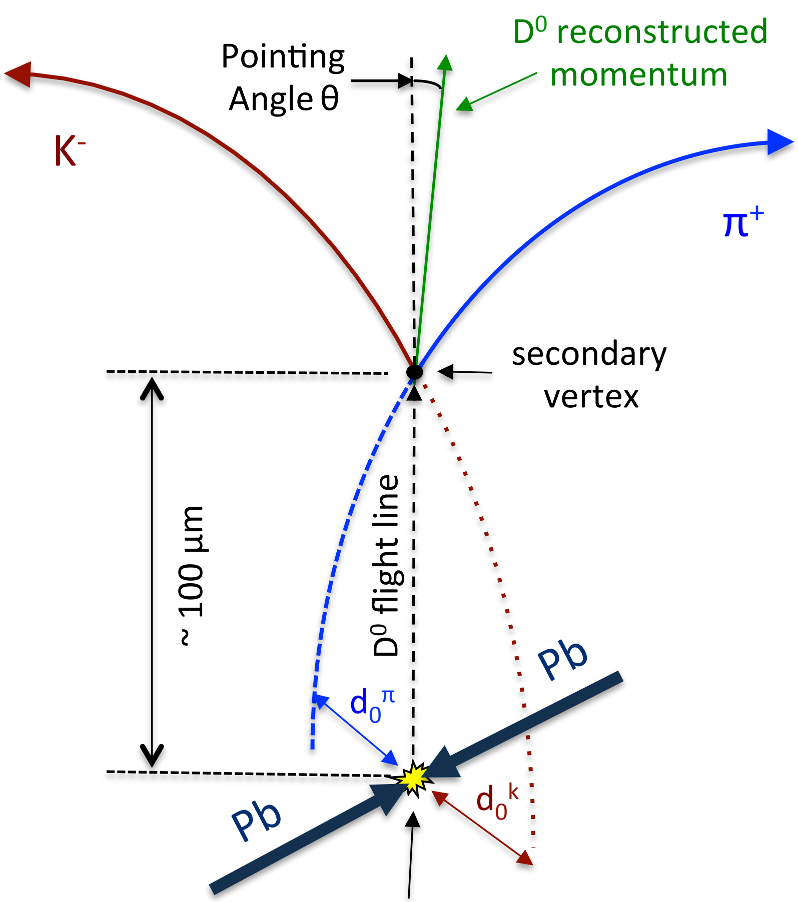
CMS



Parameters	**ALICE**	**ATLAS**	**CMS**
Nr. layers	2	3	3
Radial coverage [mm]	**39** - 76	**50** - 120	**44** – 102
Nr of pixels	9.8 M	80 M	66 M
Surface [m^2]	0.21	1.7	1
Cell size ($r\phi$ x z) [μm^2]	50 x 425	50 x 400	100 x 150
Silicon thickness (sens. + ASIC) - x/X_0 [%]	0.21 + 0.16	0.27 + 0.19	0.30 + 0.19

Performance – Secondary vertex determination

Example: D^0 meson

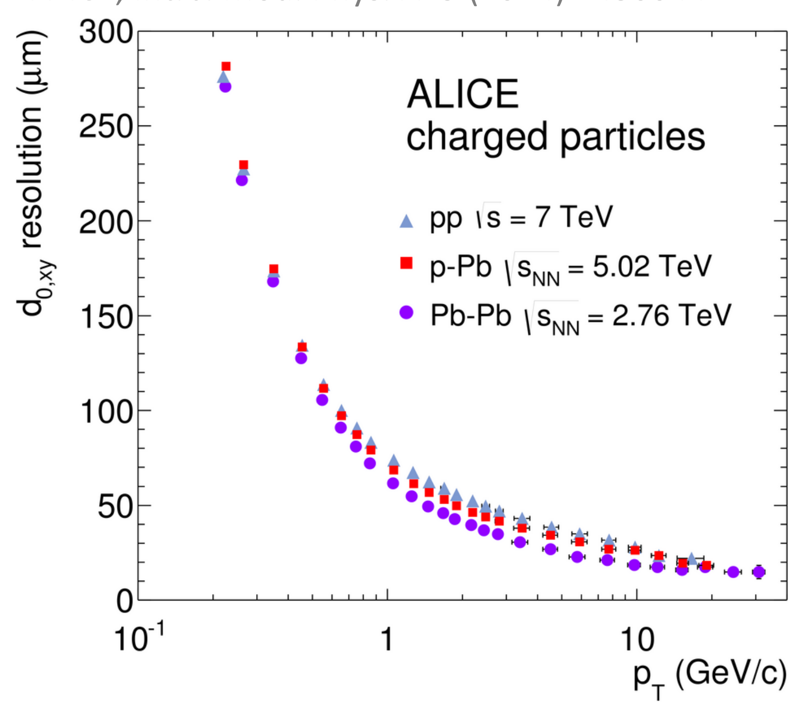


Analysis based on decay topology and invariant mass technique

Open charm

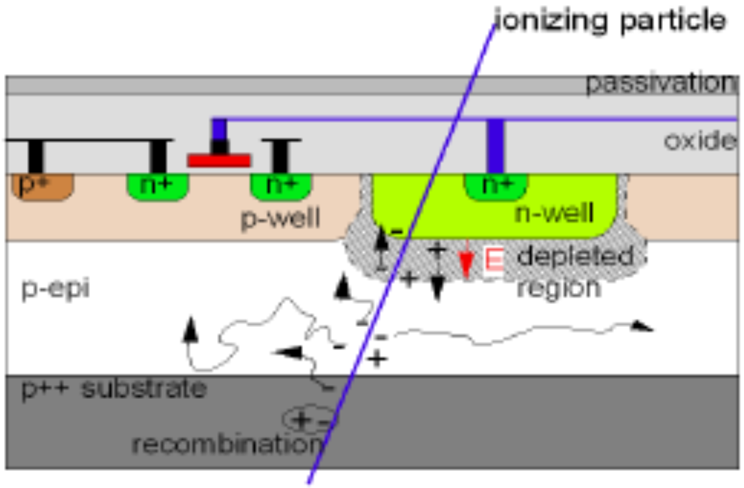
Particle	Decay Channel	cτ (µm)
D^0	$K^- \pi^+$ (3.8%)	123
D^+	$K^- \pi^+ \pi^+$ (9.5%)	312
D_s^+	$K^+ K^- \pi^+$ (5.2%)	150
Λ_c^+	$p K^- \pi^+$ (5.0%)	60

ALICE, Int. J. Mod. Phys. A29 (2014) 1430044



Classical CMOS Pixel Sensor

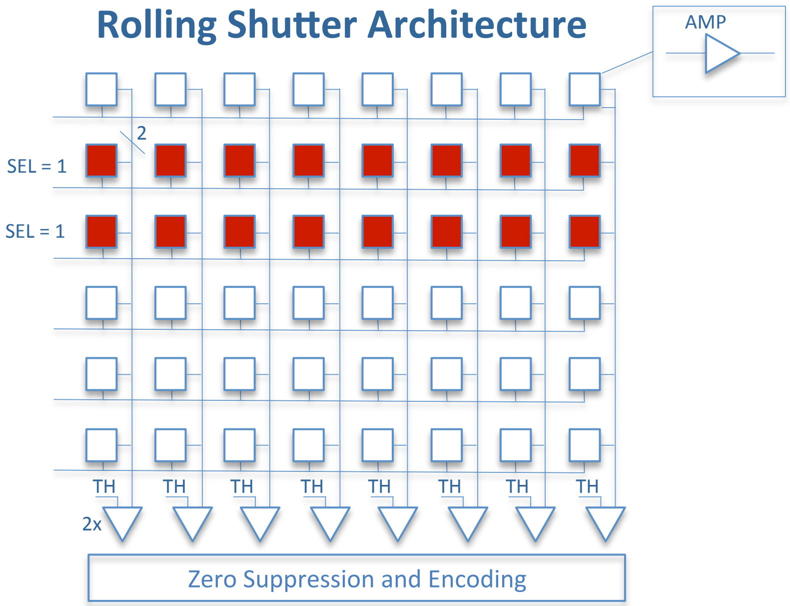
- n-well charge collector in p-type epitaxial layer
- Signal generated in a high-resistivity (> 1 kΩcm) epi-layer ~20μm thick (larger values possible)
- (Early versions with thin and low resistivity epi-layer)
- MIP produces ~80 e-h pairs per micron



M. Winter et al. (IPHC)

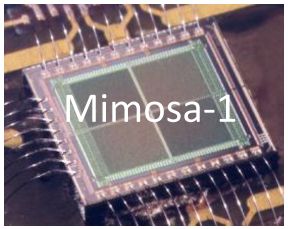
- epi-layer not fully depleted
- Charge collected by (mostly) diffusion and drift
- Longer charge collection time
- More sensitive to radiation induced displacement damage in the epi layer
- Only one transistor type in the active area (NMOS)
- Often use rolling shutter architecture for reading out the matrix

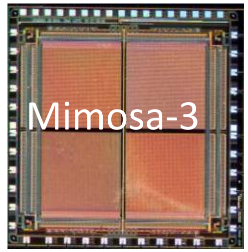
Rolling Shutter Architecture

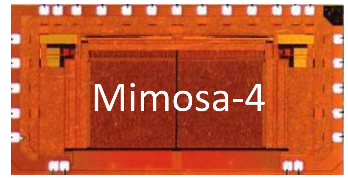


Monolithic Pixel Detectors in HI Experiments

Owing to the industrial development of CMOS imaging sensors and the intensive R&D work within the HEP community (IPHC, RAL, …)







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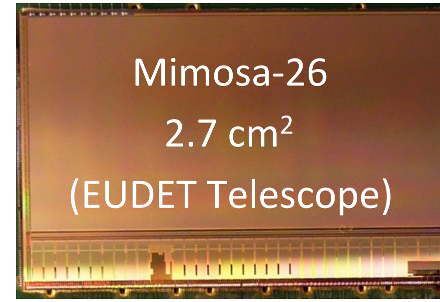
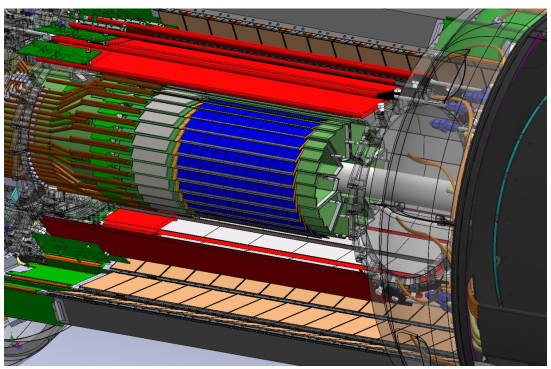
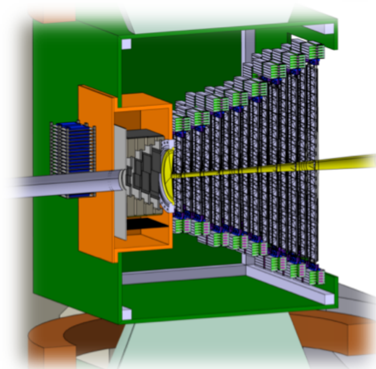
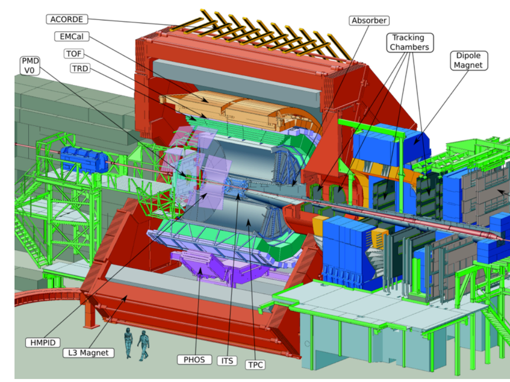


R. Turchetta, M. Winter

… several HI experiments have selected CMOS pixel sensors for their inner trackers







STAR HFT
0.16 m^2 – 356 M pixels

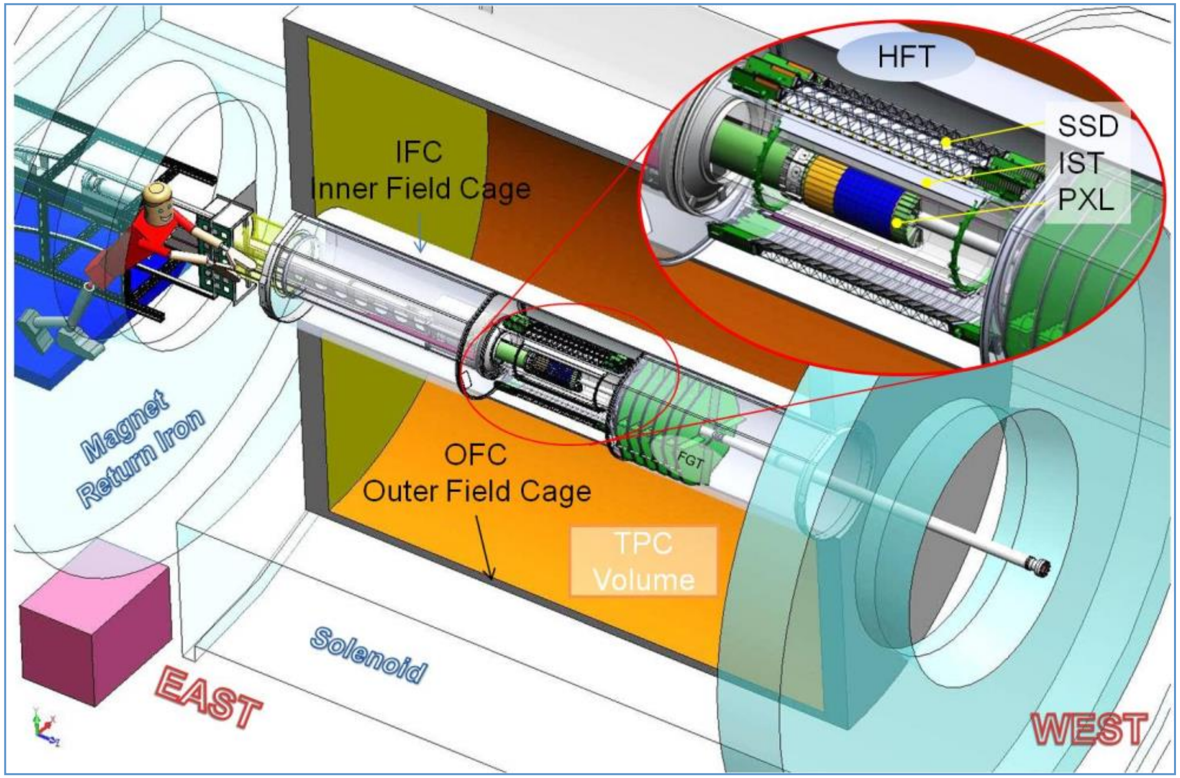
2014 - First CPS Detector

CBM MVD
0.08 m^2 – 146 M pixel

ALICE ITS Upgrade (and MFT)
10 m^2 – 12 G pixel

Synergy on sensor development

STAR Upgrade - Heavy Flavor Tracker (HFT)

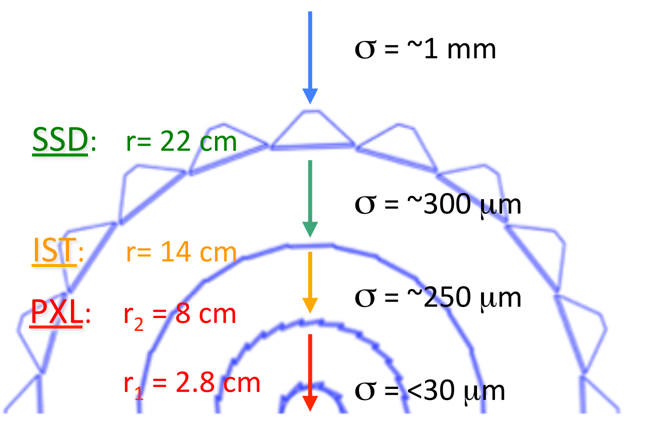


L. Greiner (LBL) / CPIX-2014

TPC – Time Projection Chamber (main tracking detector in STAR)

HFT – Heavy Flavor Tracker

- SSD – Silicon Strip Detector
- IST – Inner Silicon Tracker
- PXL – Pixel Detector



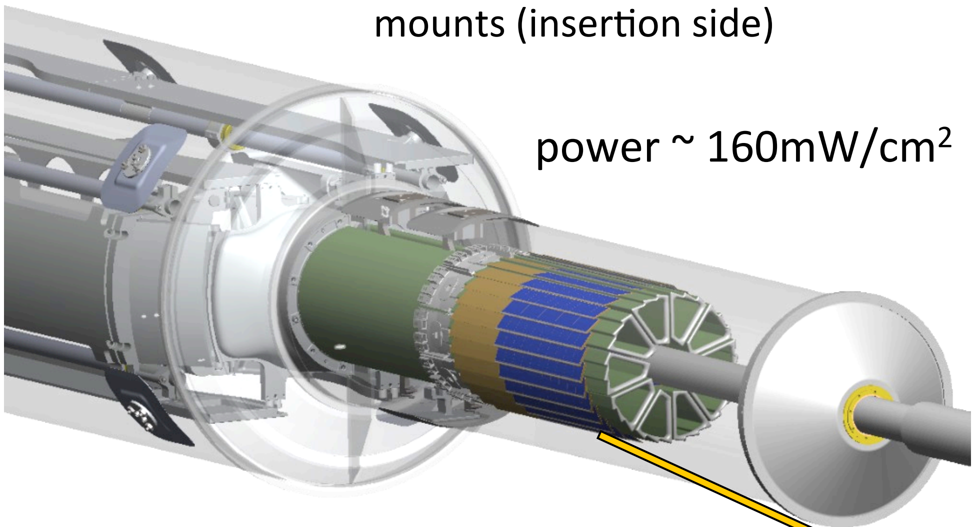
Tracking inward from the TPC with graded resolution

STAR Pixel Detector (PXL)

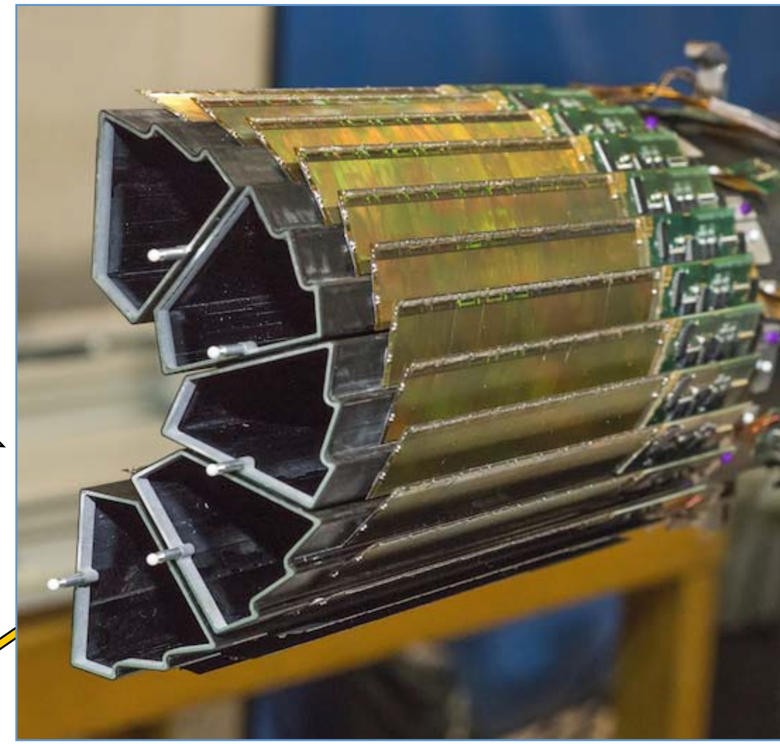
L. Greiner (LBL) / CPIX-2014

Mechanical support with kinematic mounts (insertion side)

power ~ 160mW/cm^2

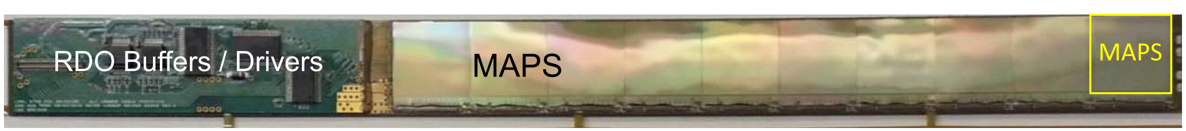


Key dates
- 3-sector prototype May 2013
- **Full detector Jan 2014**



- Insertion from one side
- 2 layers
- 10 sectors total (in 2 halves)
- 4 ladders/sector

Ladder with 10 MAPS sensors (~ 2×2 cm each)



2-layer kapton flex cable with Al traces

20 cm

carbon fiber sector tubes (~ 200 µm thick)

STAR PXL – Detector Design Characteristics

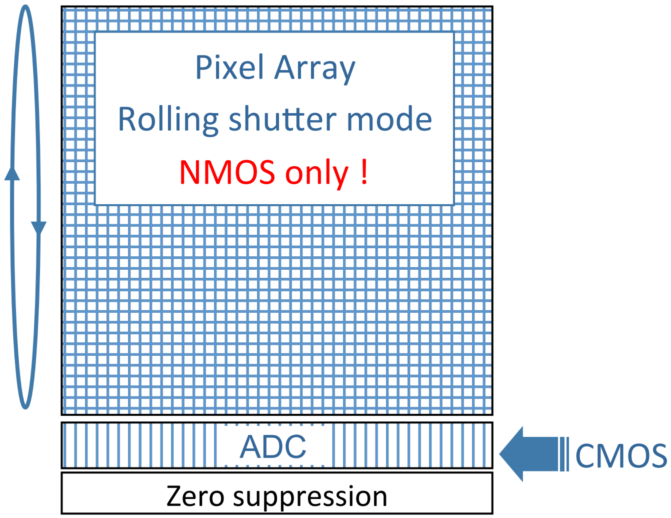
DCA Pointing resolution	$(12^{(*)} \oplus 24\ \mathrm{GeV}/p \cdot c)\ \mu m$
Layers	Layer 1 at 2.8 cm radius Layer 2 at 8 cm radius
Pixel size	20.7 μm X 20.7 μm
Hit resolution	3.7 $\mu m^{(*)}$ (6 μm geometric)
Position stability	6 μm rms (20 μm envelope)
Radiation length first layer	x/X_0 = 0.39% (Al conductor cable)
Number of pixels	356 M
Integration time (affects pileup)	185.6 μs
Radiation environment	20 to 90 kRad / year $2 \cdot 10^{11}$ to 10^{12} 1MeV n eq/cm^2
Rapid detector replacement	~ 1 day

356 M pixels on ~0.16 m^2 of Silicon

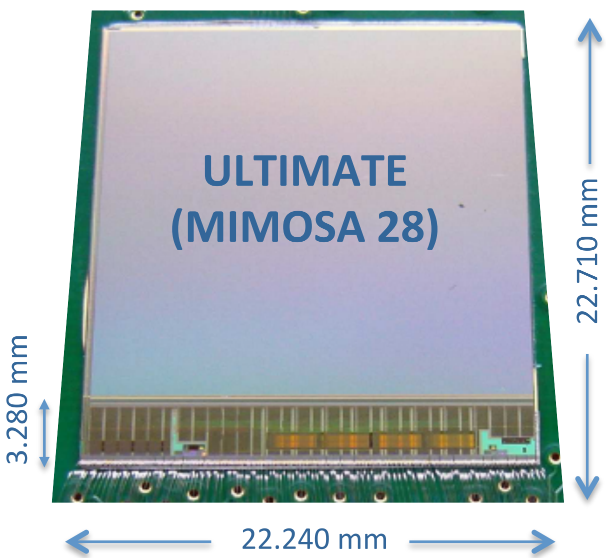
L. Greiner (LBL) / CPIX-2014

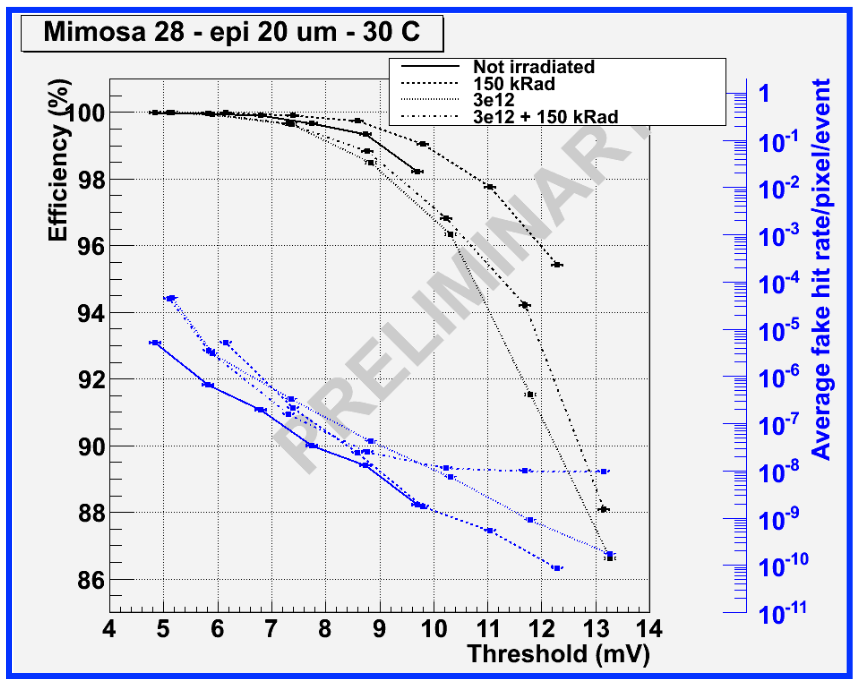
(*) Simple geometric component, cluster centriod fitting gives factor of ~1.7 better

STAR PXL – CMOS Sensor



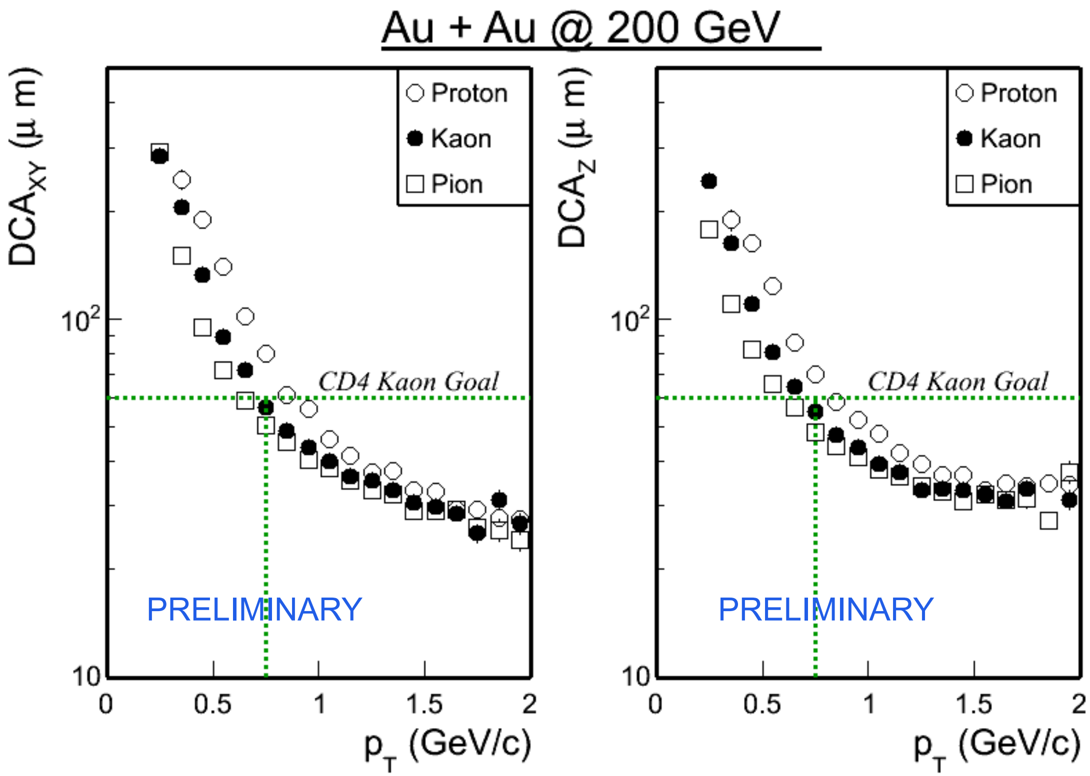
- Process: 0.35μm twin-well CMOS process
  - NMOS only in pixel array ➔ any additional N-well used to host PMOS would compete for charge collection with sensing N-well diode
- RO architecture: rolling shutter column parallel readout with integrated zero suppression logic



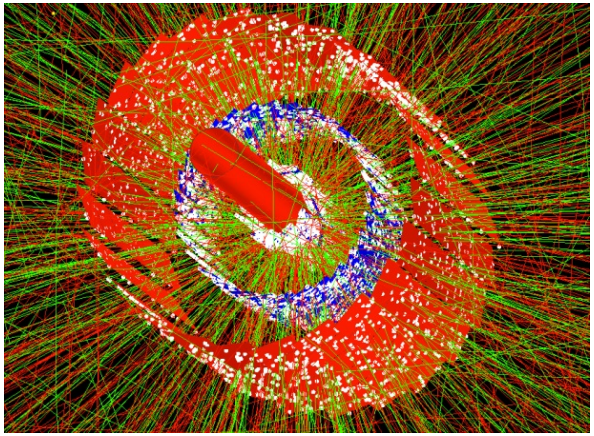


C. Hu (IPHC) / CPIX-2014

STAR HFT – pointing resolution (preliminary!)



TPC + IST + PXL



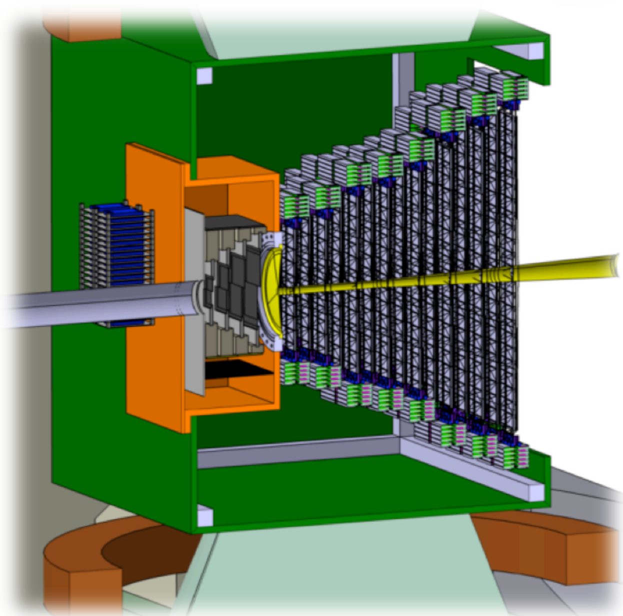
L. Greiner (LBL) / CPIX-2014

- DCA resolution for TPC tracks with 1 IST + 2 PXL hits ~ 30 µm at high p_T (better alignment still in progress will improve these results)
- Design goal for DCA resolution: 60 µm for kaons with p_T = 750 MeV/c

CBM Micro Vertex Detector (MVD)

J. Stroth (GSI and U. Frankfurt)

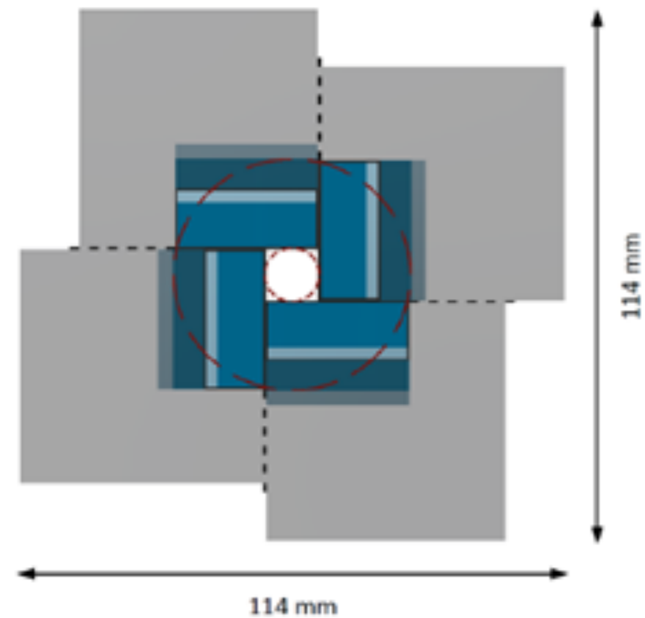
<u>MVD & STS</u>



146 M pixels

832 cm2

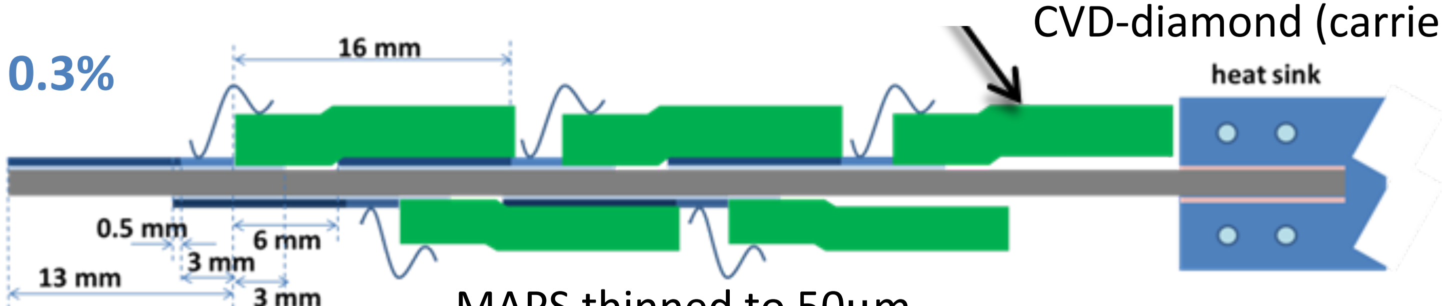
MVD Station 0



4 planar stations close to the target, vacuum operation

x/X_0 ~ 0.3%

CVD-diamond (carrier material)



MAPS thinned to 50μm

CBM MVD – Detector Design Characteristics

J. Stroth (GSI and U. Frankfurt)

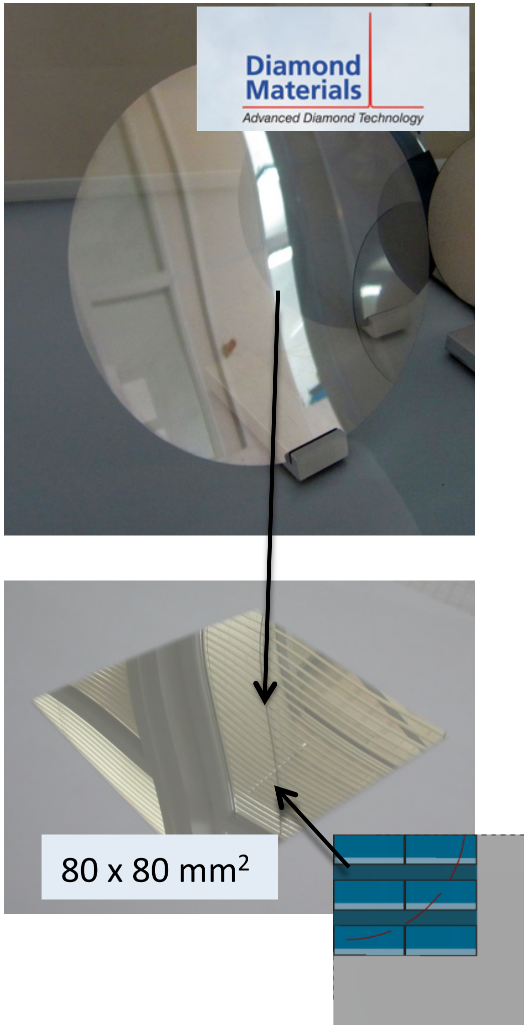
Pointing resolution	50 μm (along beam axis)
4 Planar Stations	First Station at 5cm Last station at 20cm
Pixel size	O (20 μm X 32 μm)
Hit resolution	< 10 μm
Radiation length first station	x/X_0 = 0.3% (Al conductor cable)
Number of pixels	146 M
Integration time	32 μs
Radiation environment	10^{13} 1MeV n_{eq}/cm^2 (SIS 100 lifetime)
Readout	continuous

146 M pixels on ~0.08 m^2 of silicon

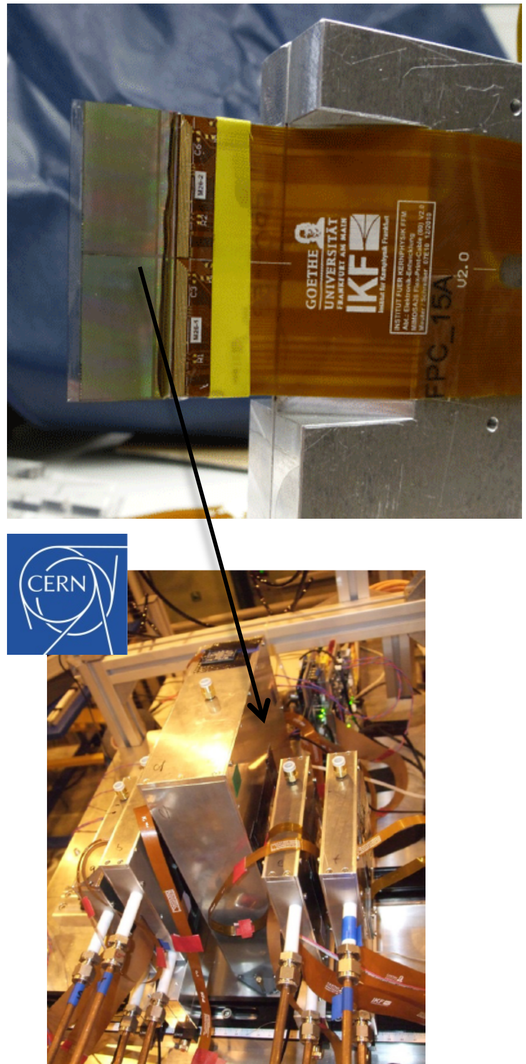
CBM MVD – R&D

J. Stroth (GSI and U. Frankfurt)

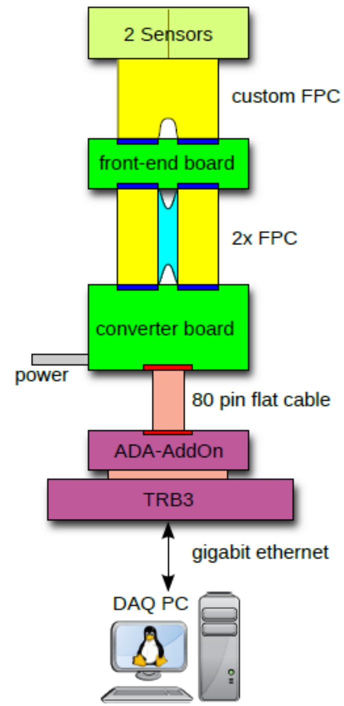
Large-area CVD-diamond carrier



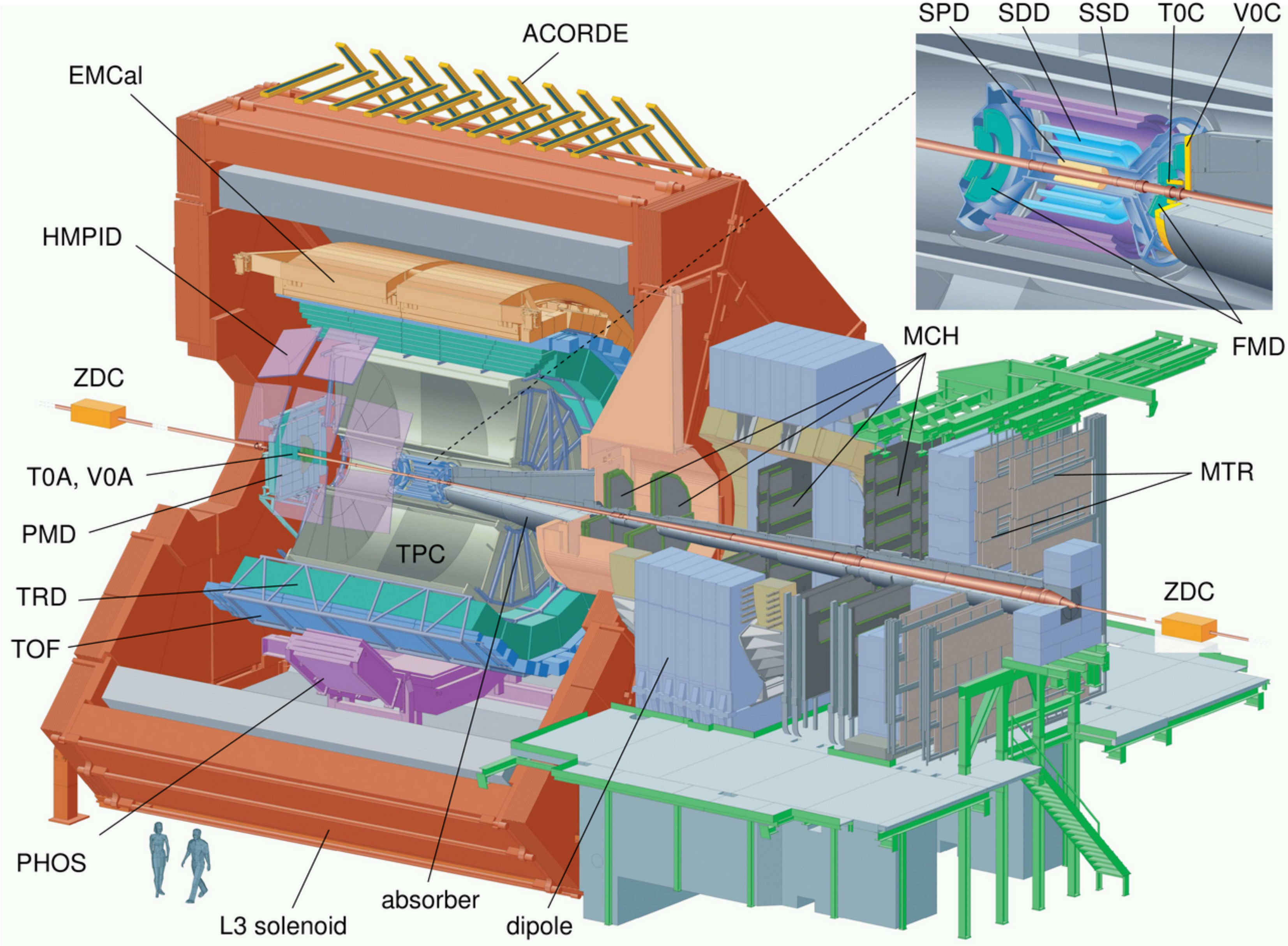
Prototype (double-sided with M26-AHR), validated in-beam



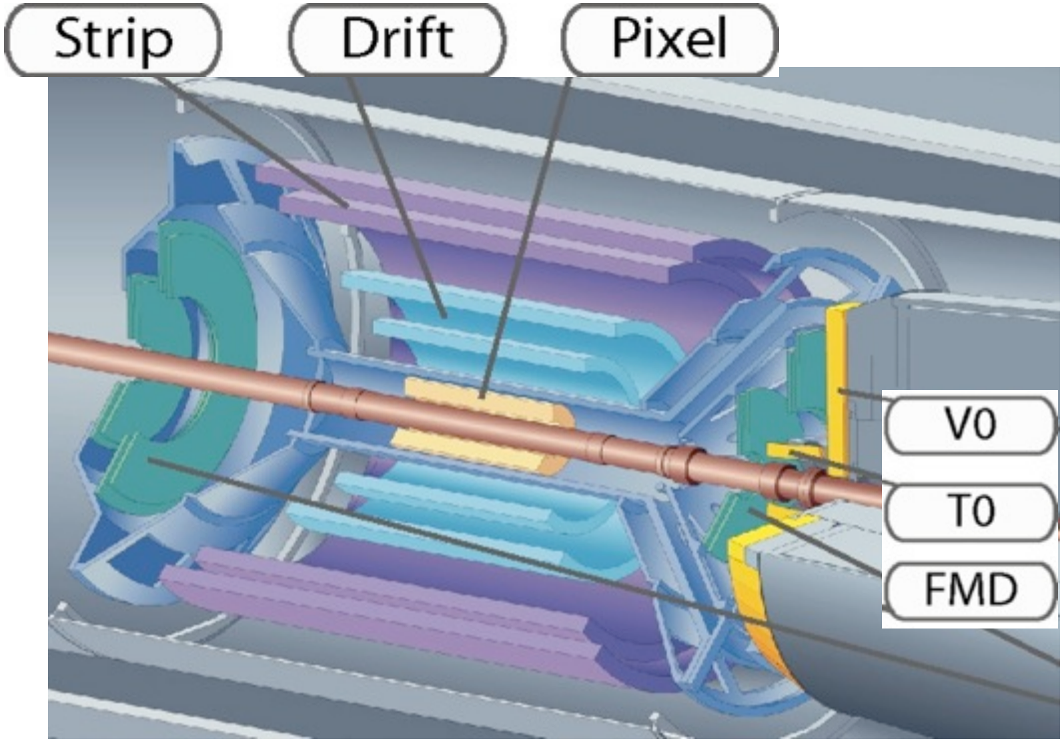
Customized FEE & DAQ, probe-testing of thin sensors

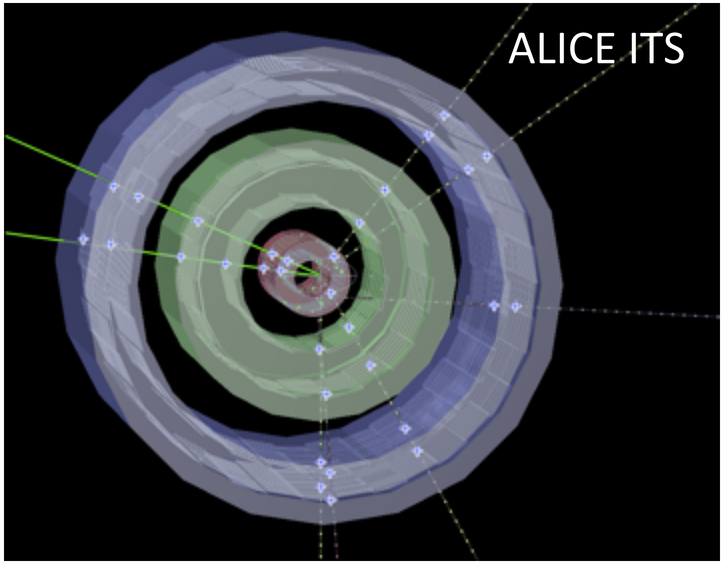


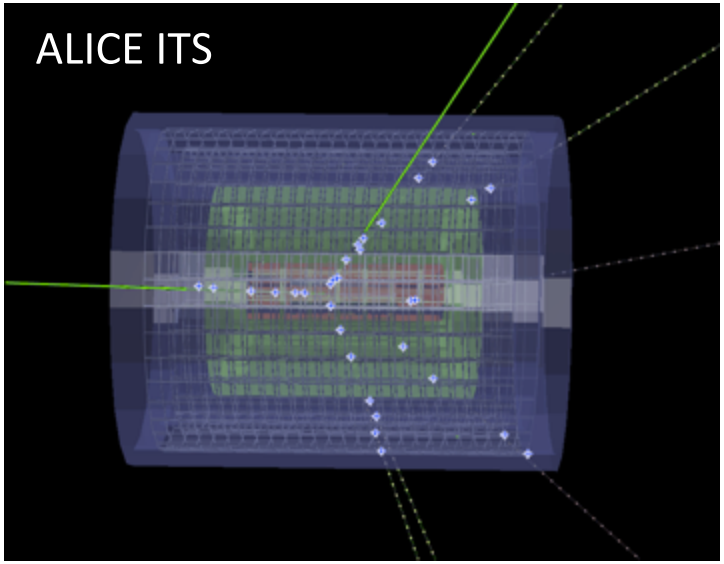
The Current ALICE Detector



The Current ALICE Inner Tracking System







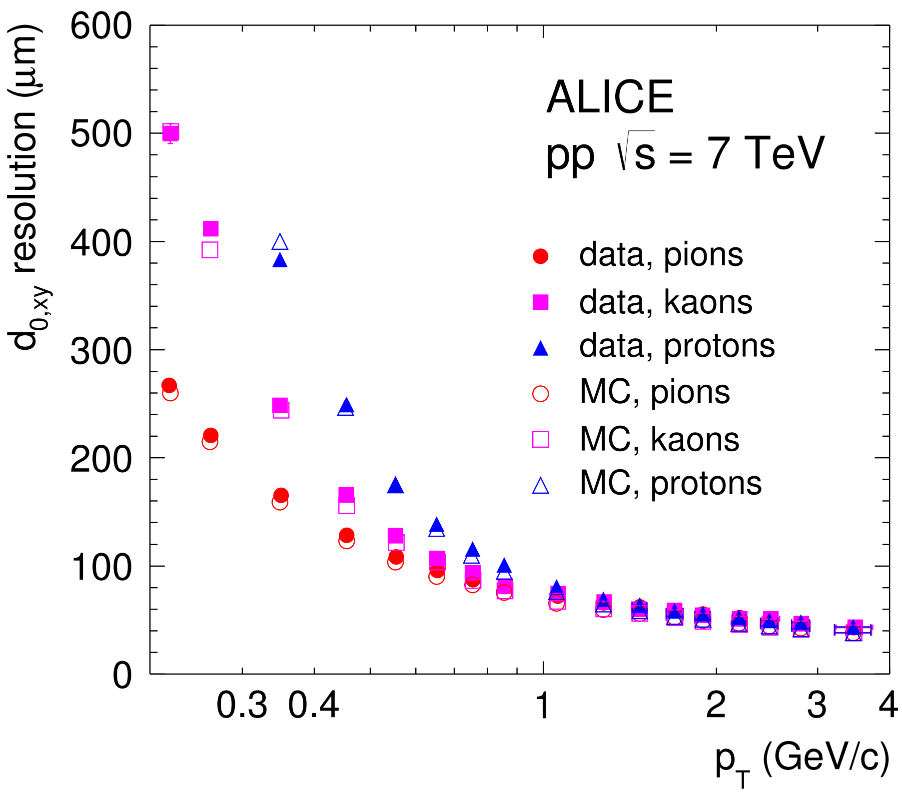
Current ITS

6 concentric barrels, 3 different technologies

- 2 layers of silicon pixel (SPD)
- 2 layers of silicon drift (SDD)
- 2 layers of silicon strips (SSD)

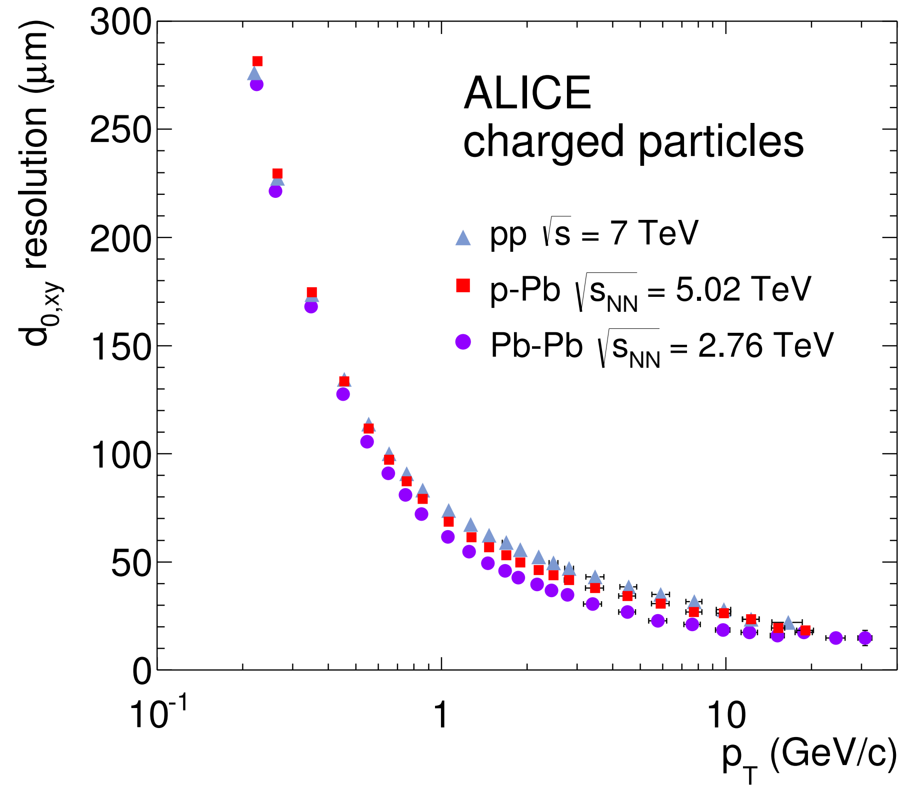
ALICE ITS Upgrade – Impact parameter resolution

Very good MC description



ALICE, Int. J. Mod. Phys. A29 (2014) 1430044

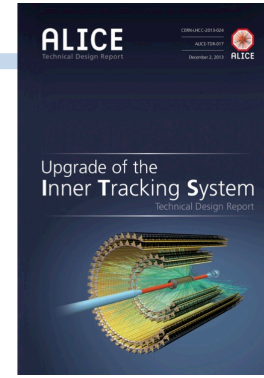
Very weak dependence on the colliding system



ALICE, Int. J. Mod. Phys. A29 (2014) 1430044

60-70 μm at p_T = 1GeV/c

Upgrade design objectives



CERN-LHCC-2013-24

1. Improve impact parameter resolution by a factor of ~3

- Get closer to IP (position of first layer): 39mm ➡ 22mm
- Reduce x/X_0 /layer: ~1.14% ➡ ~ 0.3% (for inner layers)
- Reduce pixel size: currently 50μm x 425μm ➡ O(30μm x 30μm)

2. Improve tracking efficiency and p_T resolution at low p_T

- Increase granularity:
  - 6 layers ➡ 7 layers
  - silicon drift and strips ➡ pixels

J. Phys. G (41) 087002

3. Fast readout

- readout Pb-Pb interactions at > 50 kHz and pp interactions at ~ several 10^5 Hz (currently limited at 1kHz with full ITS and ~3kHz without silicon drift)

4. Fast insertion/removal for yearly maintenance

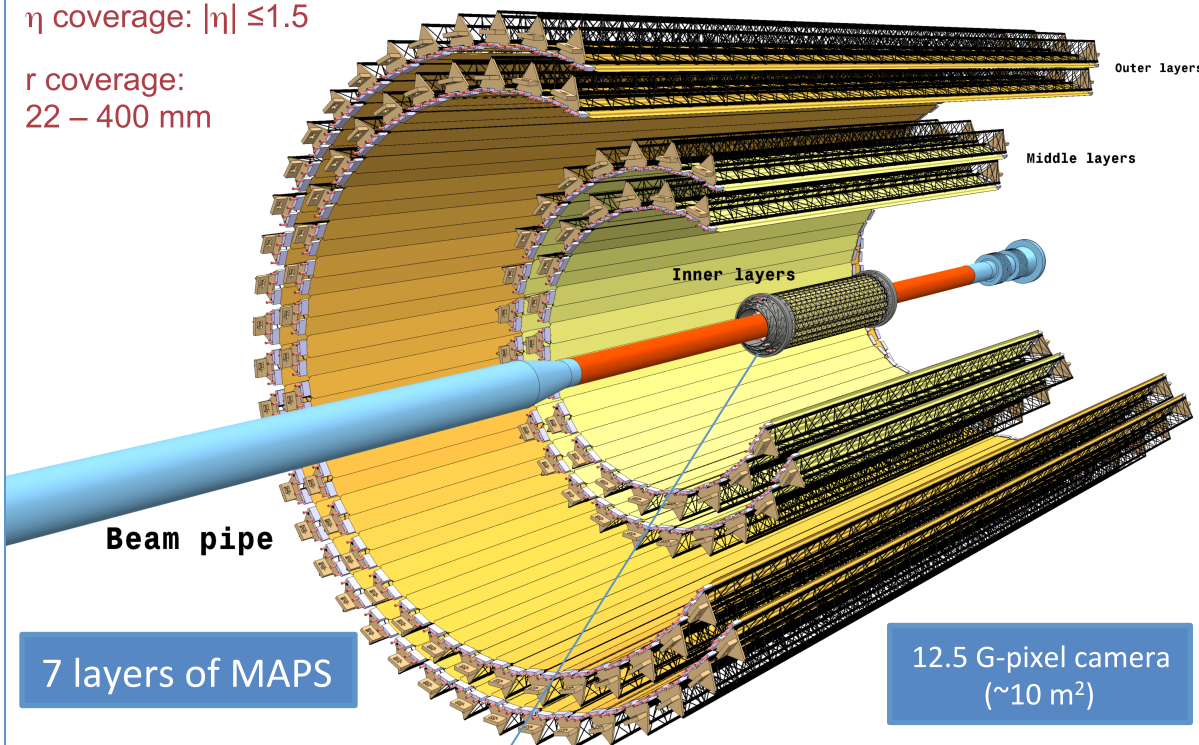
- possibility to replace non functioning detector modules during yearly shutdown

Install detector during LHCC LS2 (2018-19)

New ITS Layout

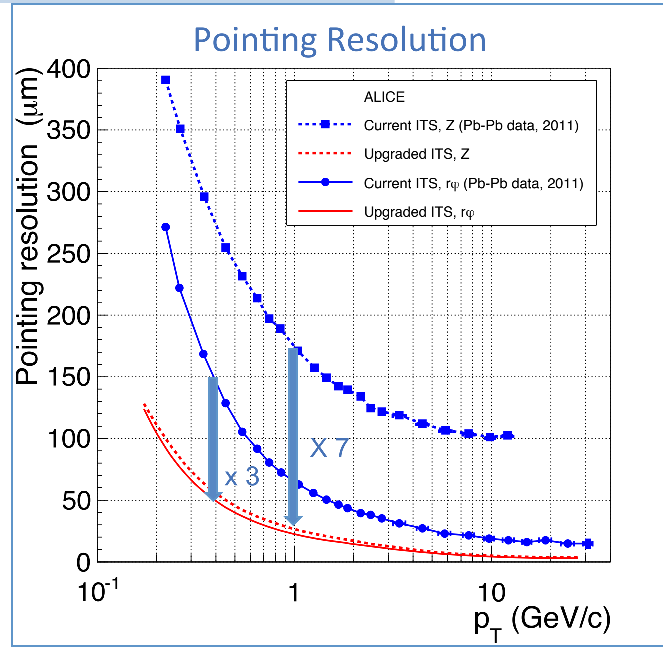
η coverage: |η| ≤1.5

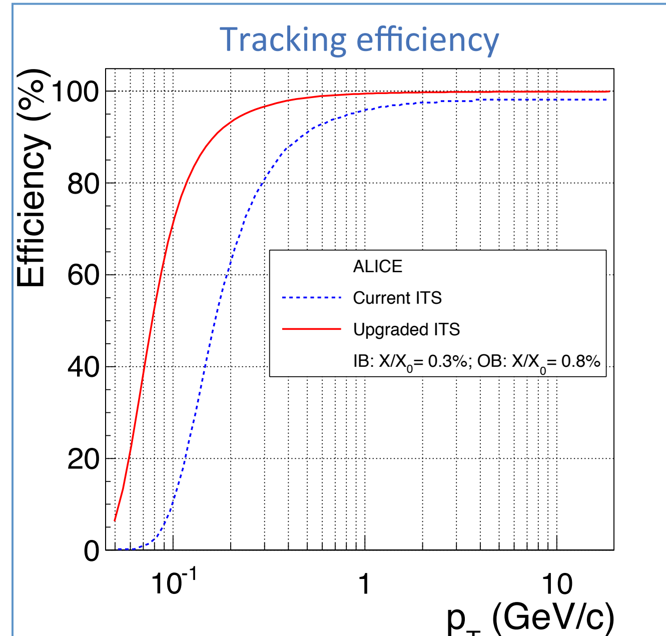
r coverage:
22 – 400 mm



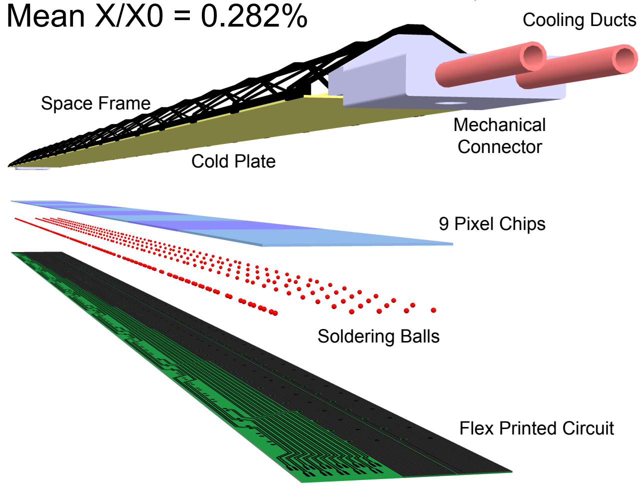
7 layers of MAPS

12.5 G-pixel camera (~10 m²)

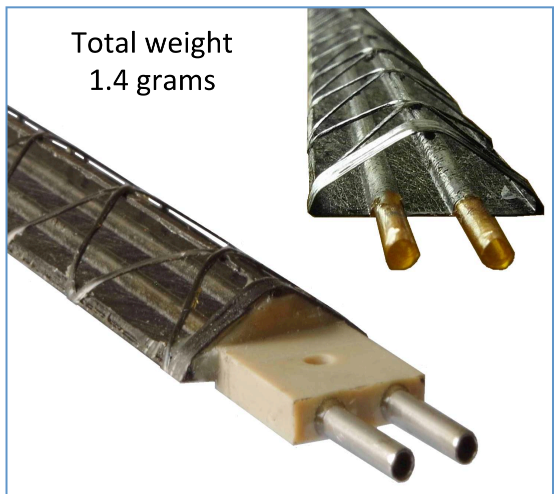




Mean X/X0 = 0.282%



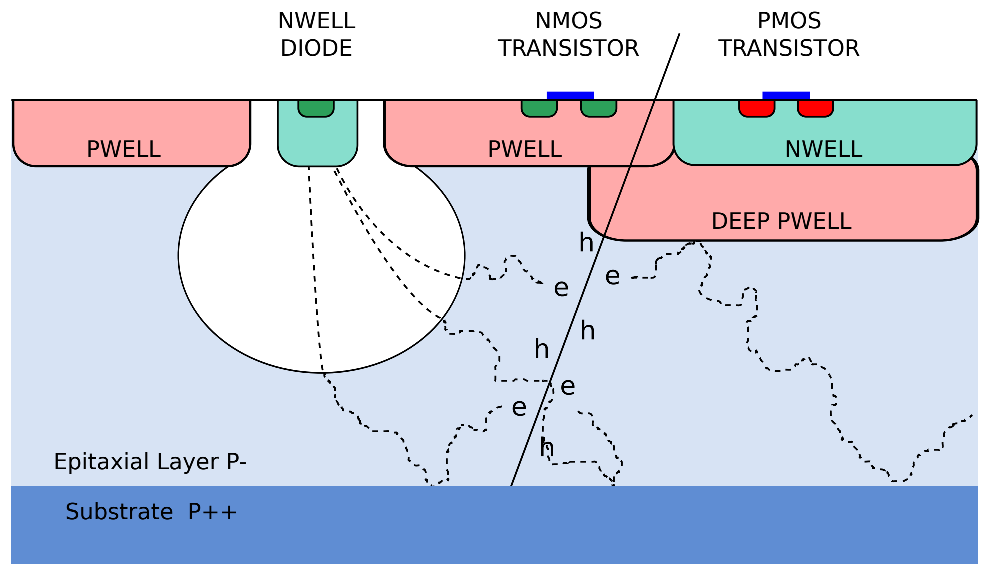
Total weight
1.4 grams



PIXEL Chip

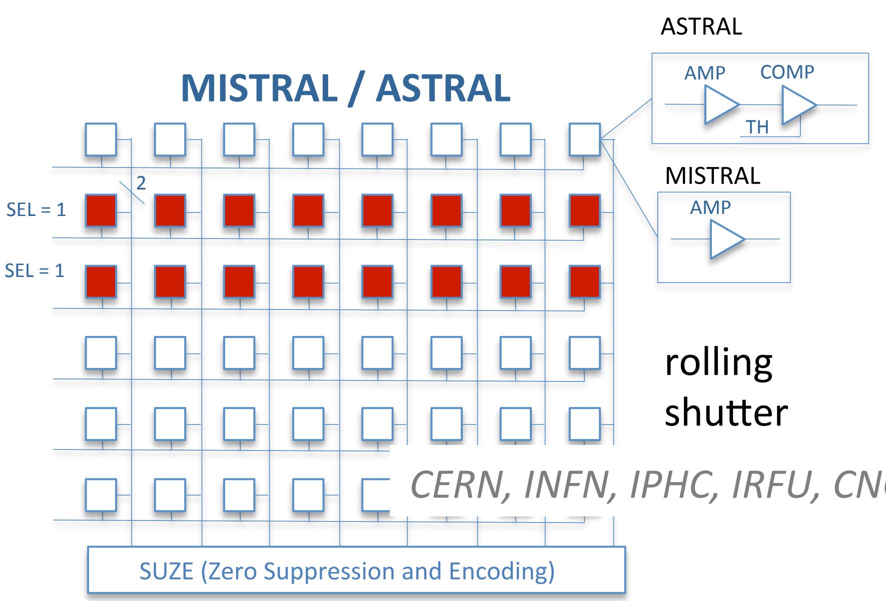
Monolithic PIXEL chip using Tower Jazz CMOS 0.18 μm

- Chip size: 15mm x 30mm
- Pixel pitch ~ 30 μm
- Spatial resolution ~ 5 μm
- Power density < 100 mW/cm^2
- Three architectures under study



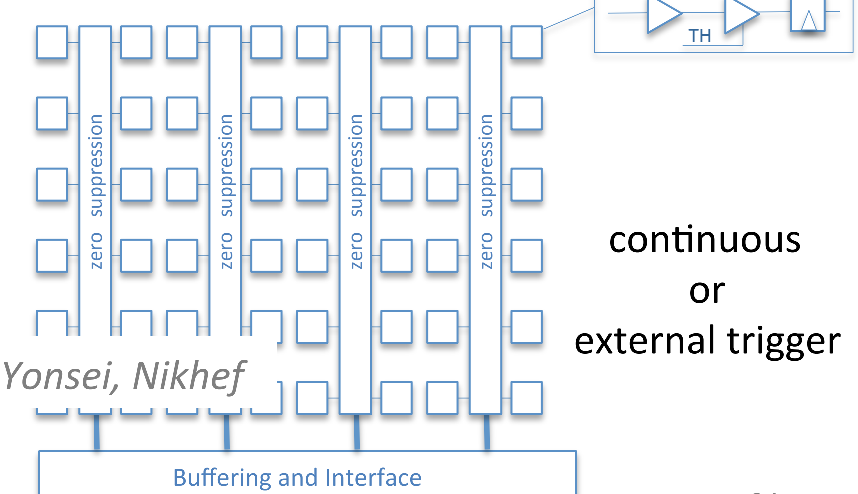
Deep p-well allows truly CMOS circuit inside pixel

MISTRAL / ASTRAL



rolling shutter

ALPIDE



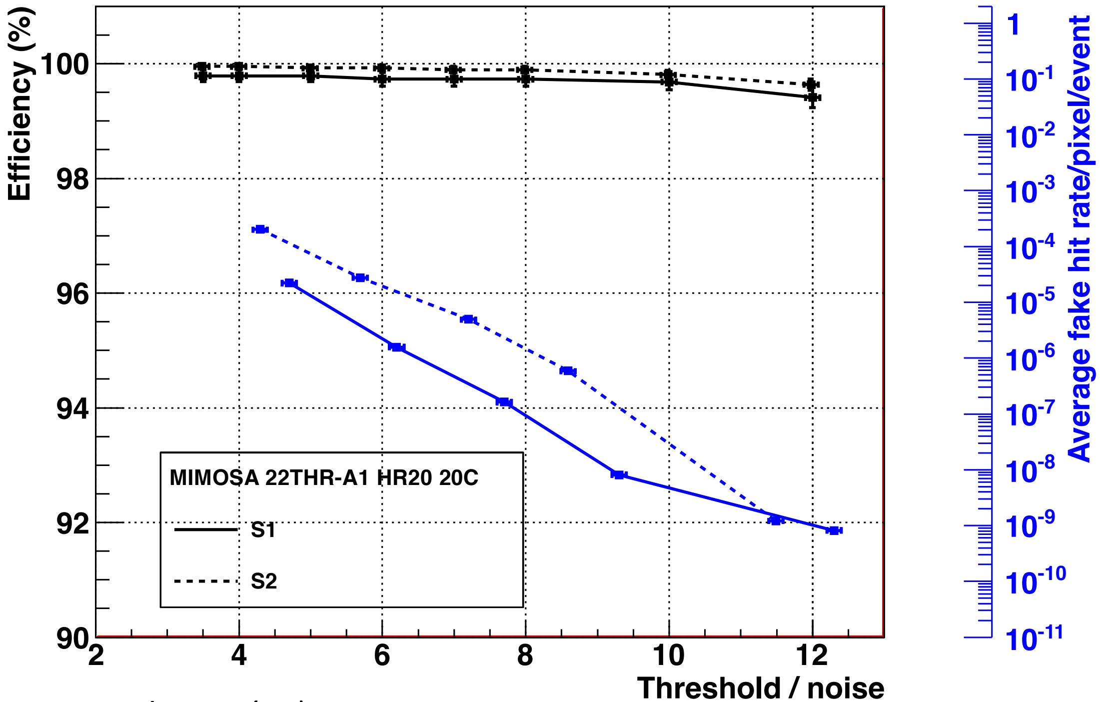
continuous or external trigger

CERN, INFN, IPHC, IRFU, CNCU, Yonsei, Nikhef

PIXEL Chip Prototypes – Experimental Results

(MISTRAL)

MIMOSA-22-THR-A1 (IPHC/IRFU), performance from digital output
pixel size (22 x 33 μm^2) and in-pixel circuitry as proposed for final chip (MISTRAL)



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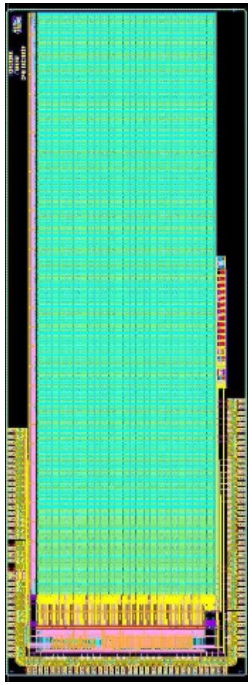
MIMOSA-22THRA

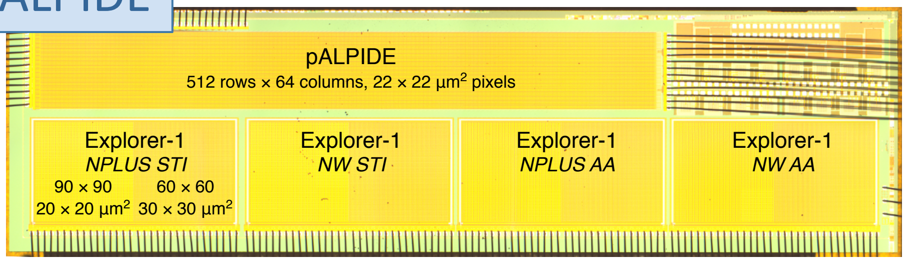


Detection efficiency and fake hit rate (DESY, e^- @ 4.4 GeV/c electron beam)

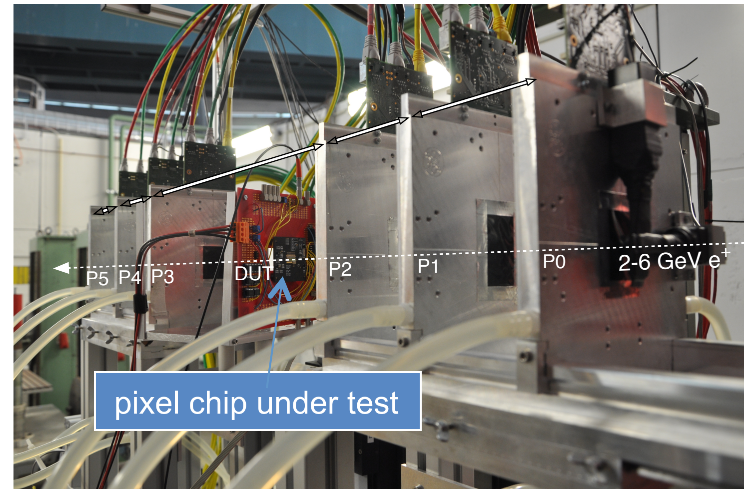
HR20 = epi-layer from different vendor: 6kΩcm, 20μm thick

PIXEL Chip Prototypes – Experimental Results

ALPIDE

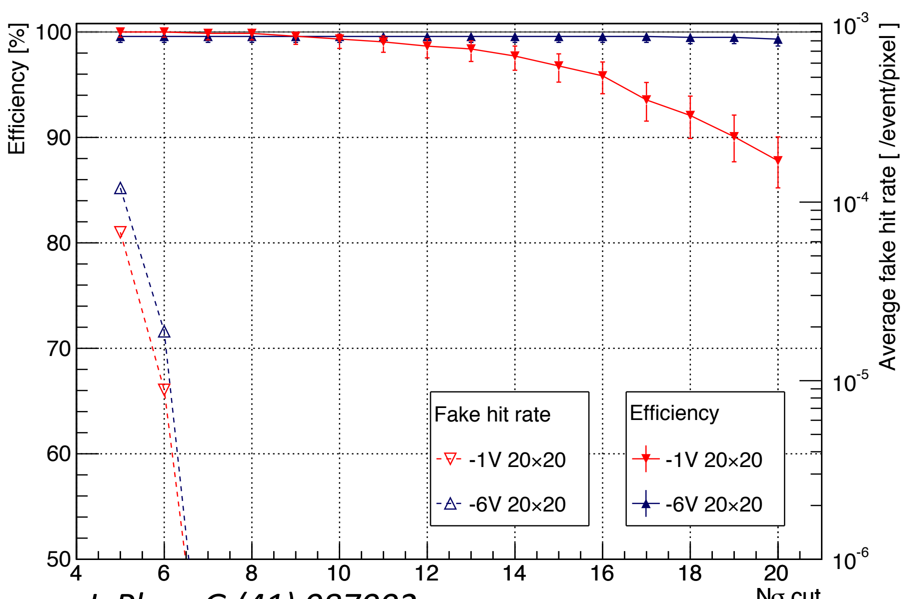


pALPIDE: sizeable prototype of final chip (digital output)
Explorer: prototype chip with analogue output



Measurements at DESY test beam (4.4 Gev electron beam) – Sep 2013

Explorer chip, performance of pixel chip from analogue output, pixel size: 20 x 20 μm^2



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pALPIDE chip, performance of pixel chip from digital output, pixel size: 22 x 22 μm^2

Threshold / Noise: 20

Detection efficiency: 99.7%

Fake hit rate < 10^{-8}

Spatial resolution ~ 5μm

FSBB-M0 – Full Scale Building Block of MISTRAL

FSBB-M0 (Full Scale Building Block Mistral 0)

- **About 1/3 of a complete sensor** (approx. **9mm x 17mm**)
- 416 x 416 pixels of 22μm x 33μm (final chip **36μm x 62μm**)
- 40μs integration time (final chip **~ 20μs**)
- Full chain working (front-end, discr., zero suppression)
- 25 sensors characterized showing similar noise performance

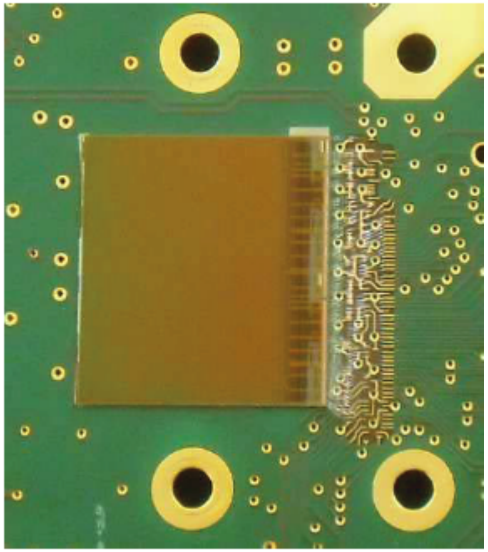


Figure: Two FSBB M0

- Dimensions: **30mm x 15 mm**
- About 0.5 M pixels 28μm x 28μm
- **40 nW front-end (4.7mW / cm^2)**
- ~40mW/cm^2 total
- Allows reverse substrates bias to increases depletion volume
- 4 sectors with different pixels

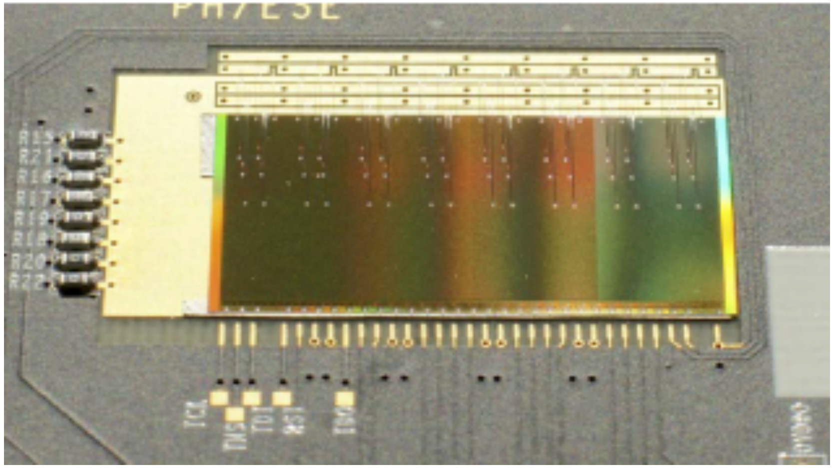


Figure: picture of pALPIDEfs

Chips under characterization at PS and SPS test beam
Results soon!

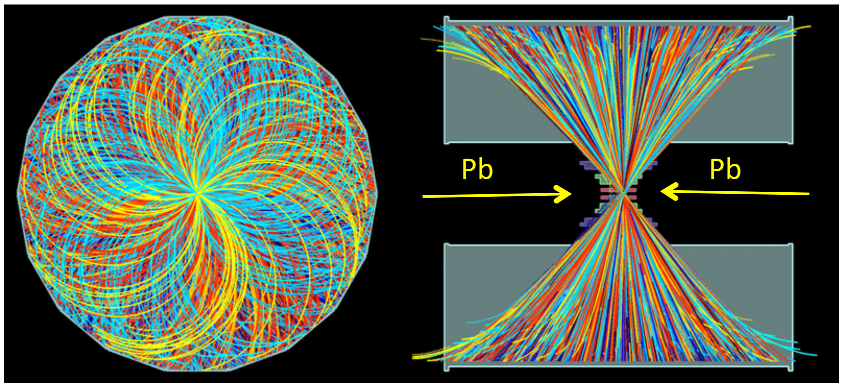
Conclusions

- Thin CMOS Pixel Sensors improve substantially the position resolution of vertex and tracking detectors
  - ✧ High granularity and position resolution, low material budget
- Large scale production available at low cost (relative to HPD)
- State-of-the-art CMOS Pixel sensors (partially depleted) can be used in applications with neutron fluency up to ~ 10^{13} cm^{-2}
- First vertex detector based on CMOS Pixel Sensor installed and successfully operated in the STAR experiment
- Intensive R&D with novel technology for the development of improved monolithic pixel detectors for CBM and ALICE
  - Reduce integration time: <10μs
  - Increase radiation hardness: ~10^{13} n cm^{-2}
  - Reduce power consumption: <50mW cm^{-2}

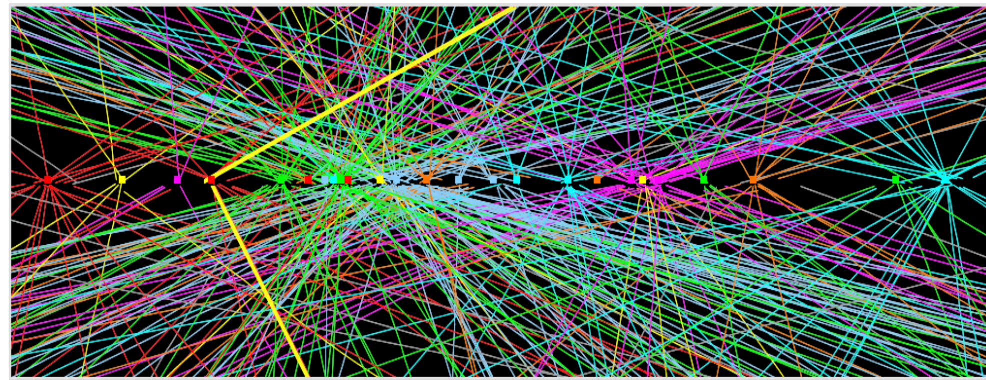
SPARES

Why use Silicon Pixels in HEP experiments

Silicon Pixel Detectors are high granularity detectors, which provide unambiguous and precise hit information in a harsh environment close to the interaction point



LHC Pb-Pb collision (ALICE, Sep 2011)



LHC pp collisions: a candidate Z boson event in the dimuon decay with 25 reconstructed vertices. (ATLAS, April 2012)

- Position resolution down to few microns
- Unambiguous hit information in high track density region
- High resolution for determination primary and secondary vertex
- Fast readout
- High level of radiation hardness

Pixel Detectors in HEP – Short historical excursus

First use in HEP Experiments: CCDs used early 1980s in SLD/SLAC and NA11/32 CERN

“The silicon micropattern detector: a dream?”

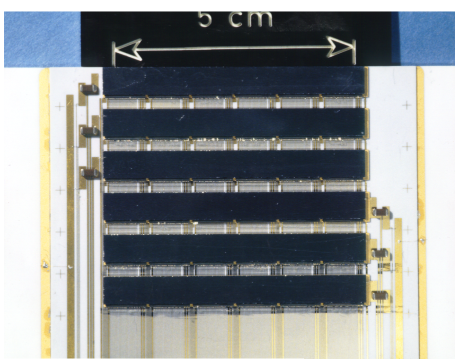
E.H.M Heijine, P. Jarron, A. Olsen and N. Redaelli , *Nucl. Instrum. Meth. A 273 (1988) 615*

“Development of silicon micropattern detectors”

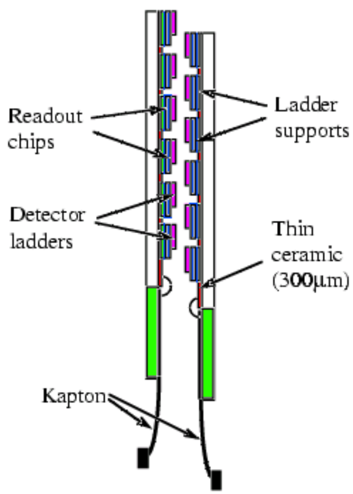
CERN RD19 collaboration, *Nucl. Instrum. Meth. A 348 (1994) 399*

1995 – First Hybrid Pixel detector installed in WA97 (CERN, Omega facility)

1996/97 – First Collider Hybrid Pixel Detector installed in DELPHI (CERN, LEP)

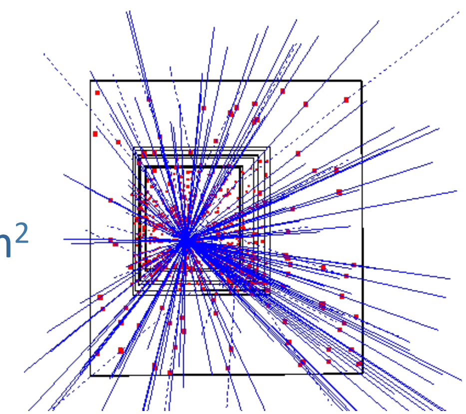


E. Heijine, E. Chesi



CERN – WA97 Experiment (1995)

- 5×5 cm^2 area
- 7 detector planes
- ~0.5 M pixels
- Pixel size 75×500 μm^2
- 1 kHz trigger rate
- Omega2 chip

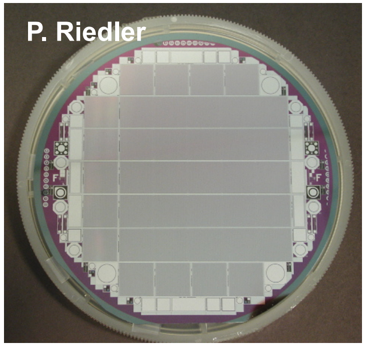


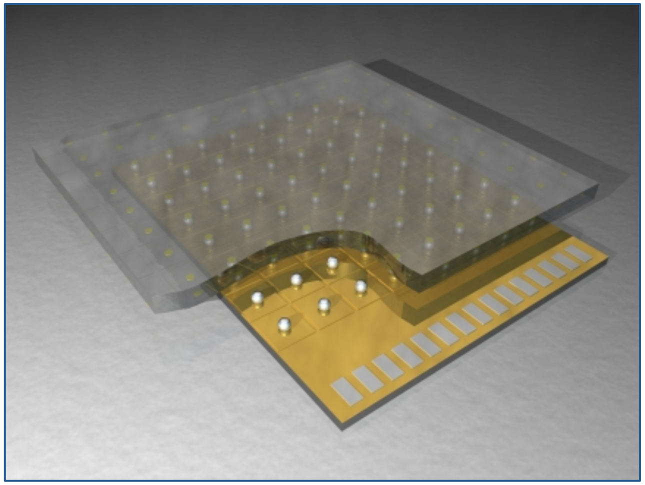
Work carried out by RD19 for WA97 and NA57/CERN

No-field, Pb-Pb, 153 reconstructed tracks

Beyond Hybrid Pixel Detectors …

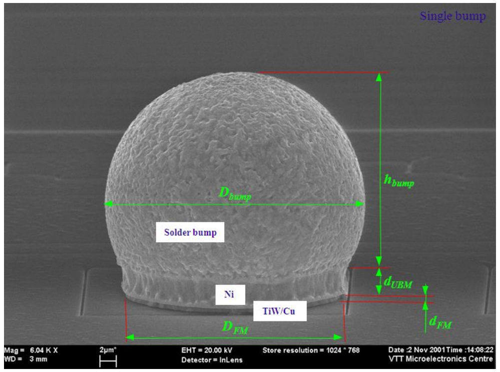
- Limited number of sensors producers (~10 world-wide)
- no industrial scale production ➔ high cost



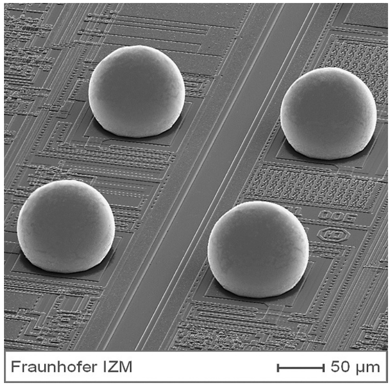


Azom.com

- Complex and costly interconnection between sensors and ASIC
- Interconnection technology (micro-bump bonding) limits:
  - pitch (currently ~30μm)
  - input capacitance ➔ power



VTT Microelectronics Centre



Fraunhofer IZM

Lower production cost

Higher integration (pitch, x/X_0)

Lower power (x/X_0, cost)

Pixel Detectors in HEP – Inner Tracking Region

	Inter. Rate (Hz)	Particle Rate [kHz/mm^2]	Fluence [n_{eq}/cm^2 per lifetime]	Ionization dose [Mrad per year]
LHC (10^{34} cm^{-2}s^{-1})	10^9	10^3	2×10^{15}	79
HL-LHC (10^{35} cm^{-2}s^{-1})	6×10^{10}	10^4	2×10^{15}	> 500
LHC HL-HI (6 x 10^{27} cm^{-2}s^{-1})	10^5	10	< 10^{13}	0.1
RHIC (8 x 10^{27} cm^{-2}s^{-1})	10^5	3.8	few 10^{12}	0.2
FAIR CBM	10^6		10^{13}	0.1
SuperKEKB (8 x 10^{35} cm^{-2}s^{-1})		400	3×10^{12}	10
ILC (10^{34} cm^{-2}s^{-1})		250	10^{12}	0.4

Monolithic Pixels
- Lower rates
- Lower radiation
- Smaller Pixels
- Less material

Examples: STAR HFT, BELLE II, CBM, ALICE Upgrade

Hybrid Pixels
- High rates
- High radiation

Examples: ATLAS, CMS, NA62

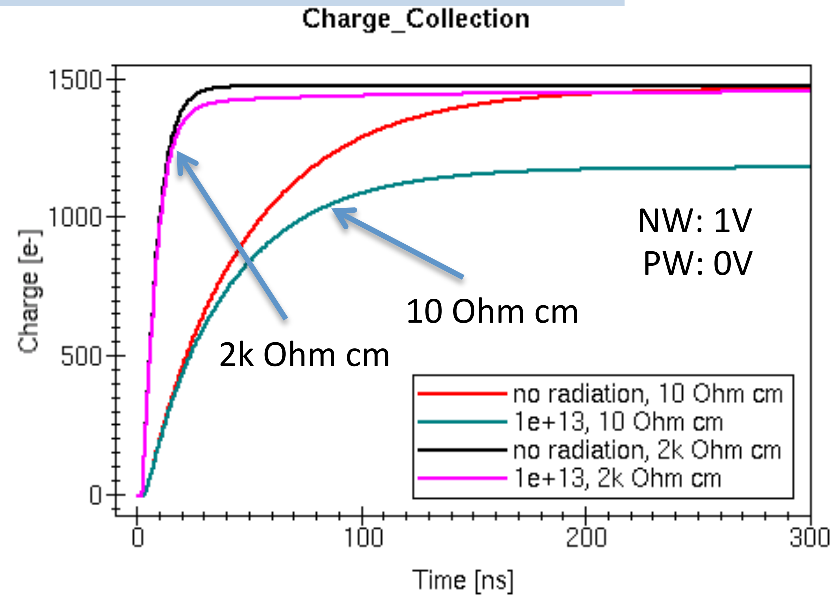
CMOS Pixel Sensors – Radiation tolerance

Transistor radiation tolerance comes for free for deep sub-micron CMOS and improved design layout

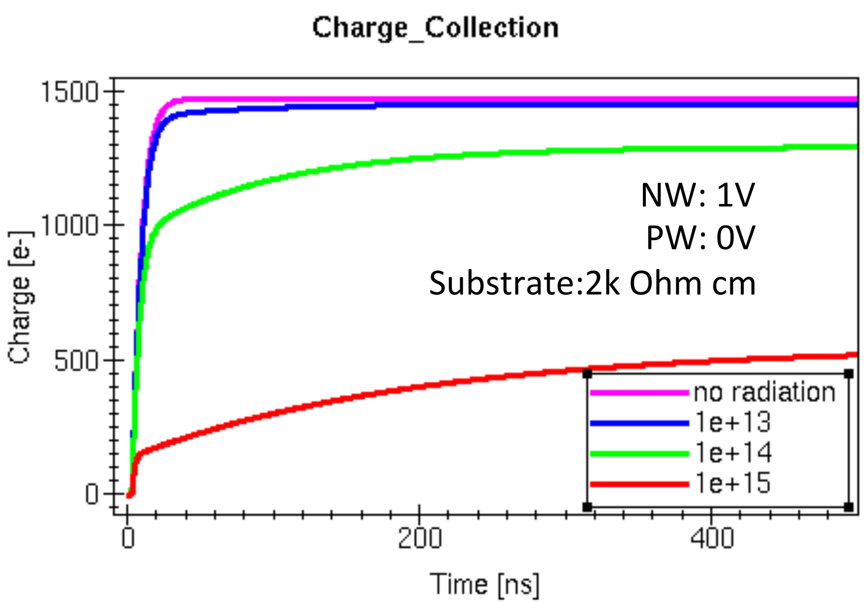
Charge collection by diffusion suffers from radiation damage beyond 10^{13} n cm^{-2}

High Resistivity epi layer

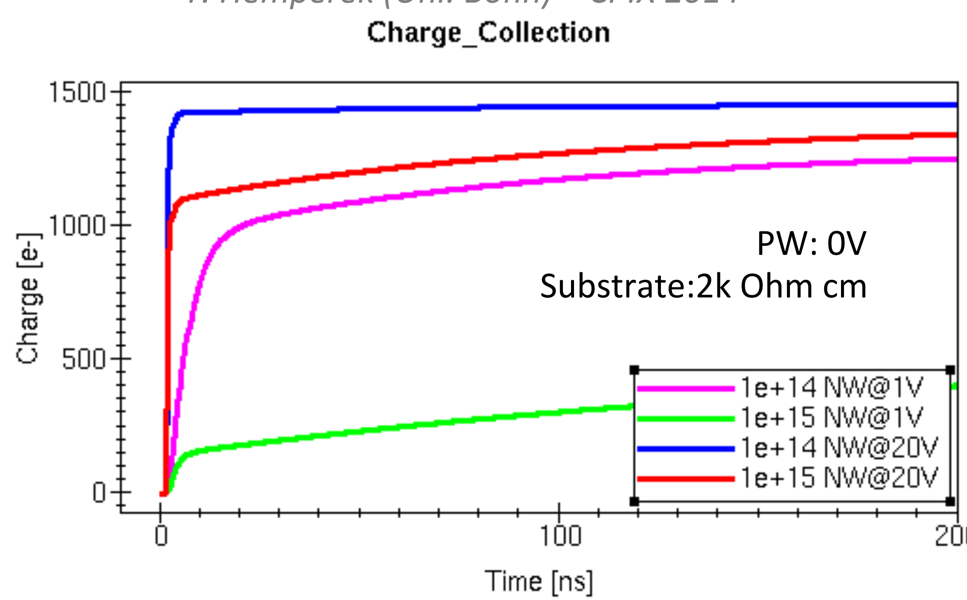
Deplete epi-layer to collect charge by drift



T. Hemperek (Uni. Bonn) – CPIX 2014



T. Hemperek (Uni. Bonn) – CPIX 2014

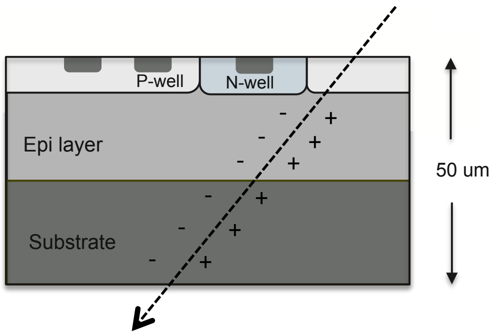


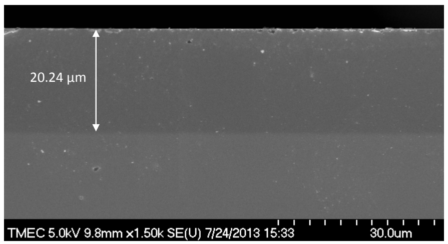
T. Hemperek (Uni. Bonn) – CPIX 2014

Monolithic Pixel Detector

Low Power – Low Mass

The actual silicon thickness is only part of the detector material thickness and can be of the order of 50 μm (e.g. STAR PXL, CBM MVD, ALICE ITS Upgrade)





ALICE, J. Phys. G (41) 087002

The power consumption will impact material budget trough cables and cooling

W. Snoeys, NIMA 731 (2013) 125-130

Analogue power depends on charge collected (Q) over the electrode capacitance (C)

$$P \sim \left(\frac{S/N}{Q/C}\right)^{m} \Rightarrow P \sim \left(\frac{Q}{C}\right)^{-m}$$

For constant S/N at a certain bandwidth

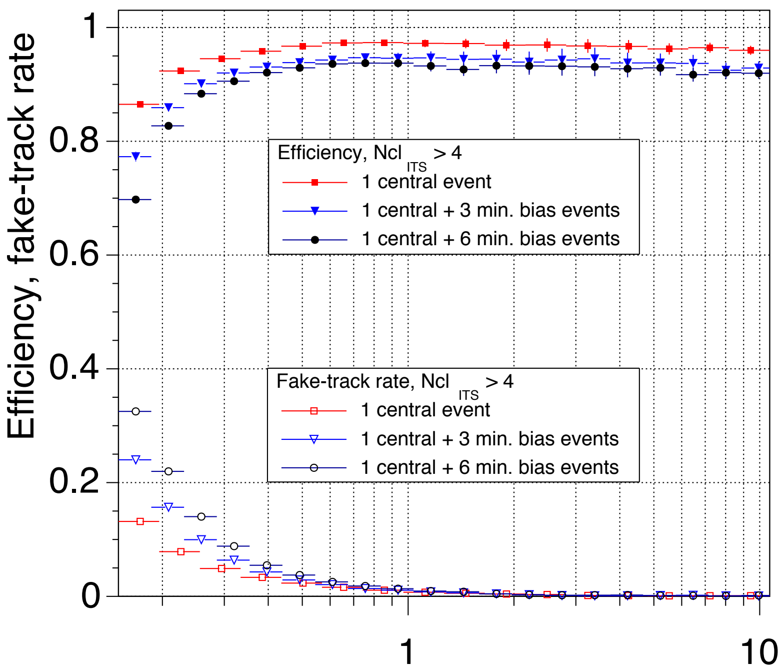
$$2 \le m \le 4$$

ATLAS SPD (50x425μm^2): C_{det}~100 fF

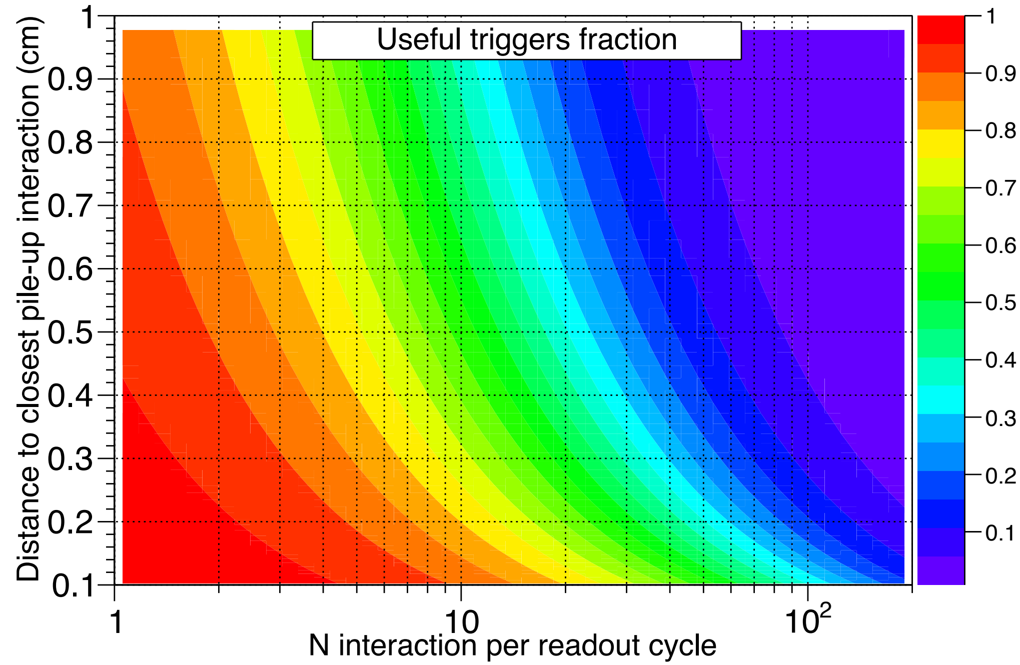
ALICE ITS upgrade (30x30μm^2): C_{det} ~ 5 fF

How integration time and pile-up affect performance

ALICE ITS Upgrade



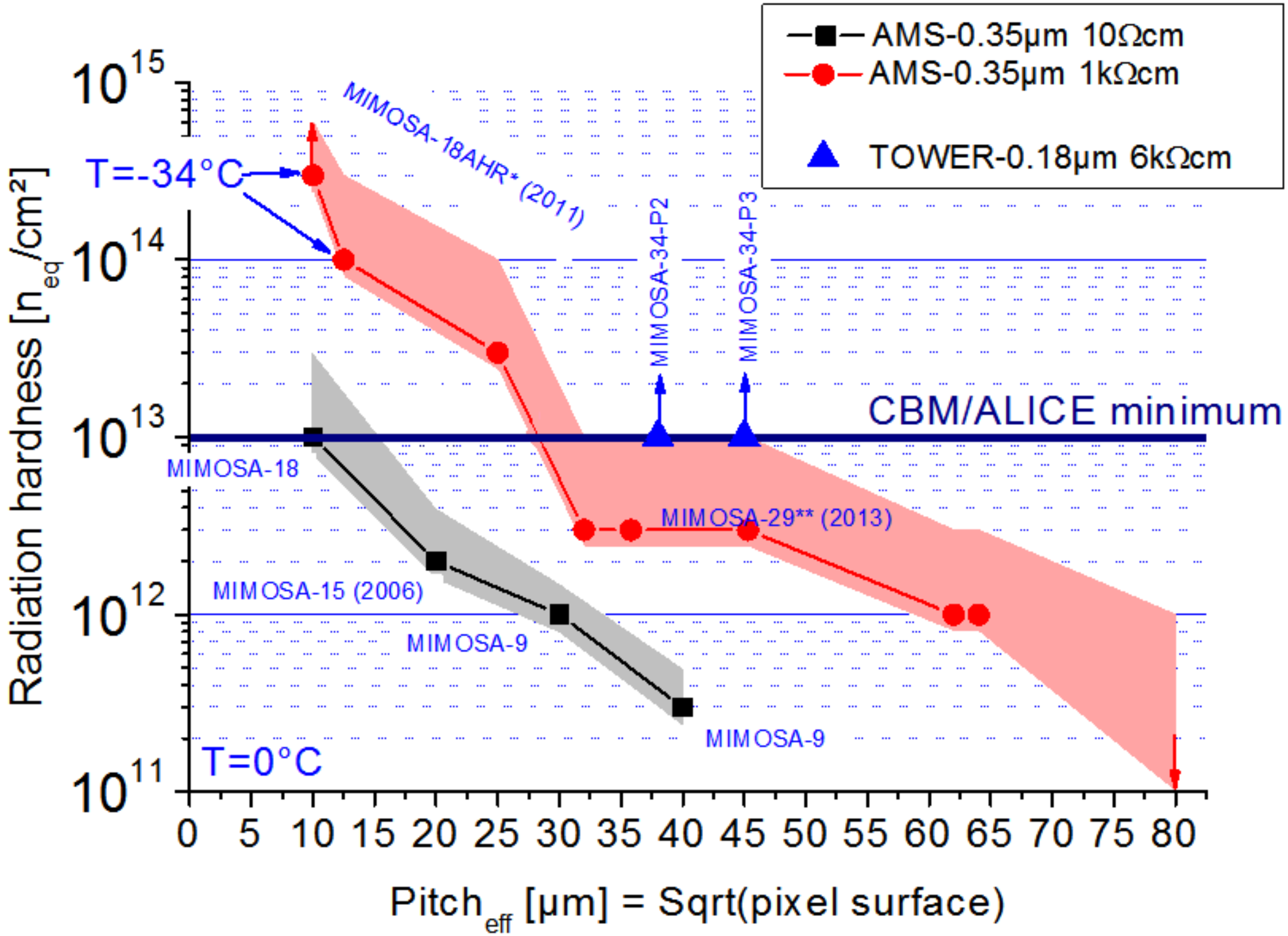
ALICE, J. Phys. G (41) 087002



At 50 kHz Pb-Pb interaction rate
<pile-up> @ 20 μs integration time: 1 central + 1 minimum bias

At 200 kHz pp interaction rate
<pile-up> @ 20 μs integration time: 5 interaction

Sensor radiation tolerance



Sensors: IPHC Strasbourg
M. Deveaux, D. Doering, S. Strohauer, CBM/IKF Frankfurt

*MIMOSA-34: EPI = 20µm, 1-6kΩ cm (not controlled), wafer from external provider

FSBB-M0 – Full Scale Building Block of MISTRAL

FSBB-M0 (Full Scale Building Block Mistral 0)

- About 1/3 of a complete sensor (approx. 9mm x 17mm)
- 416 x 416 pixels of 22μm x 33μm (final chip 36μm x 62μm)
- 40μs integration time
- Full chain working (front-end, discr., zero suppression)
- 25 sensors characterized showing similar noise performance
- Test beam measurements at SPS in October

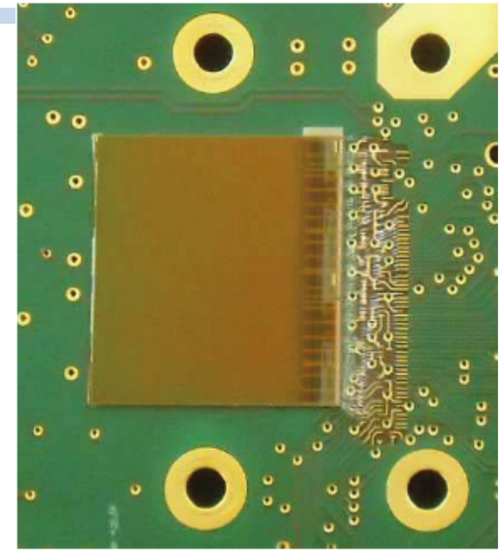
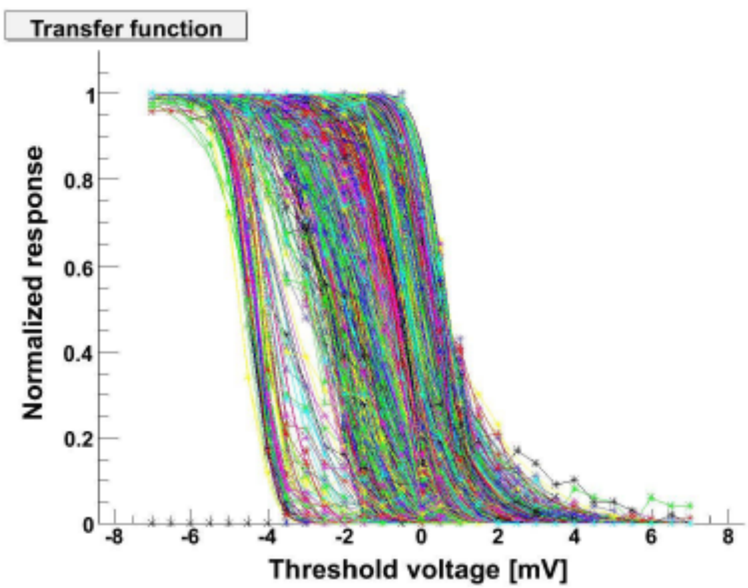
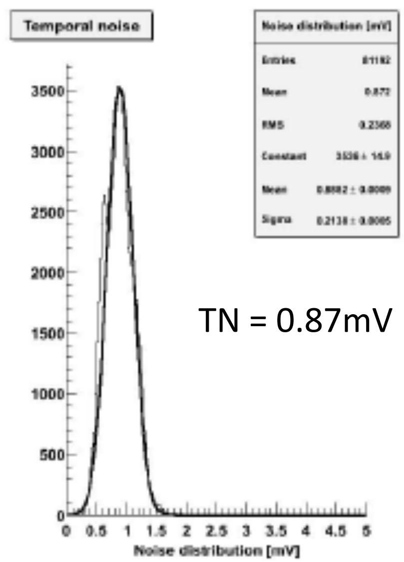


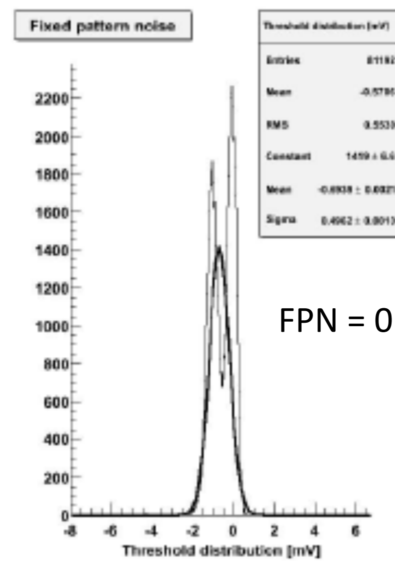
Figure: Two FSBB M0

M. Winter (IPHC) – CPIX2014





Temporal Noise



Fixed Pattern Noise

pALPIDEfs – A full-scale prototype of ALPIDE

- Dimensions: 30mm x 15 mm
- About 0.5 M pixels 28μm x 28μm
- 40 nW front-end (4.7mW / cm^2)
- ~40mW/cm^2 total
- Allows reverse substrates bias to increases depletion volume
- 4 sectors with different pixels

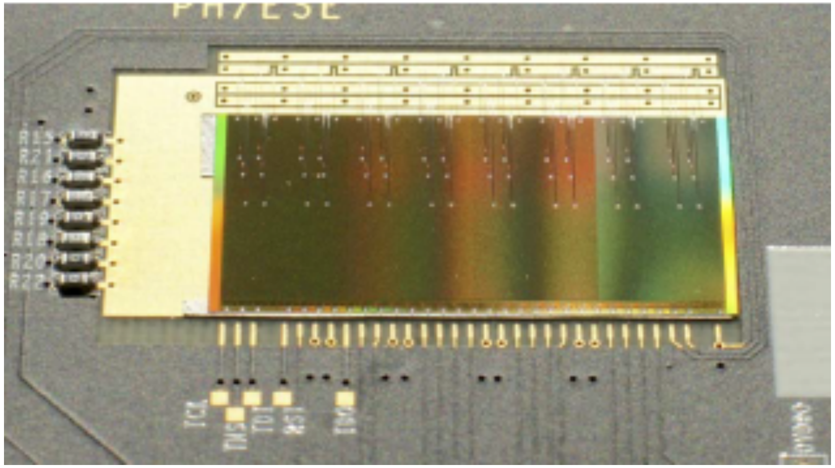
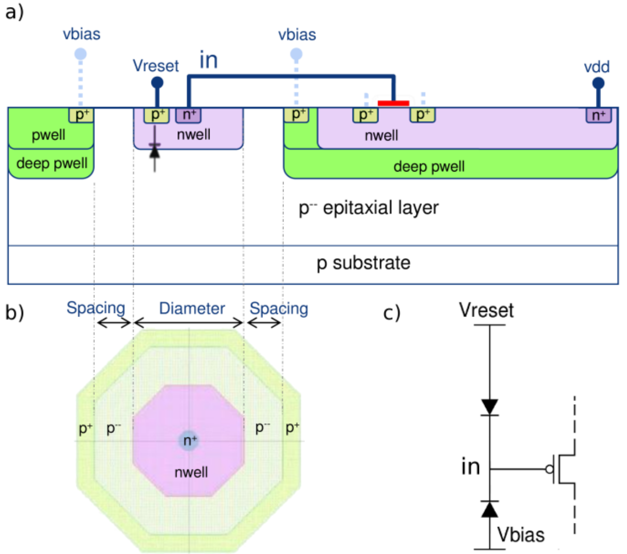


Figure: picture of pALPIDEfs

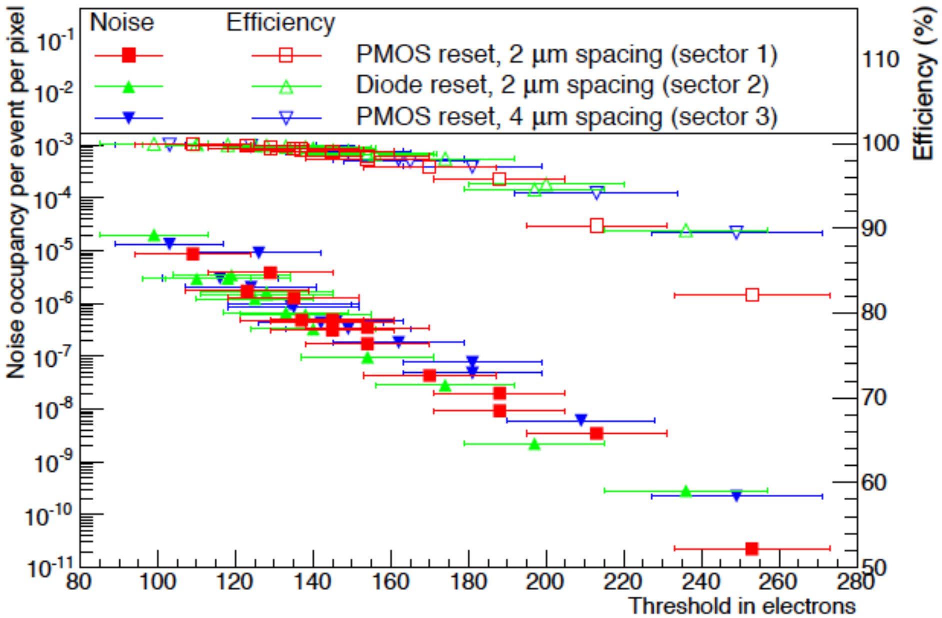
Sector	nwell diameter	Spacing	pwell opening	Reset
0	2 μm	1 μm	4 μm	PMOS
1	2 μm	2 μm	6 μm	PMOS
2	2 μm	2 μm	6 μm	Diode
3	2 μm	4 μm	10 μm	PMOS

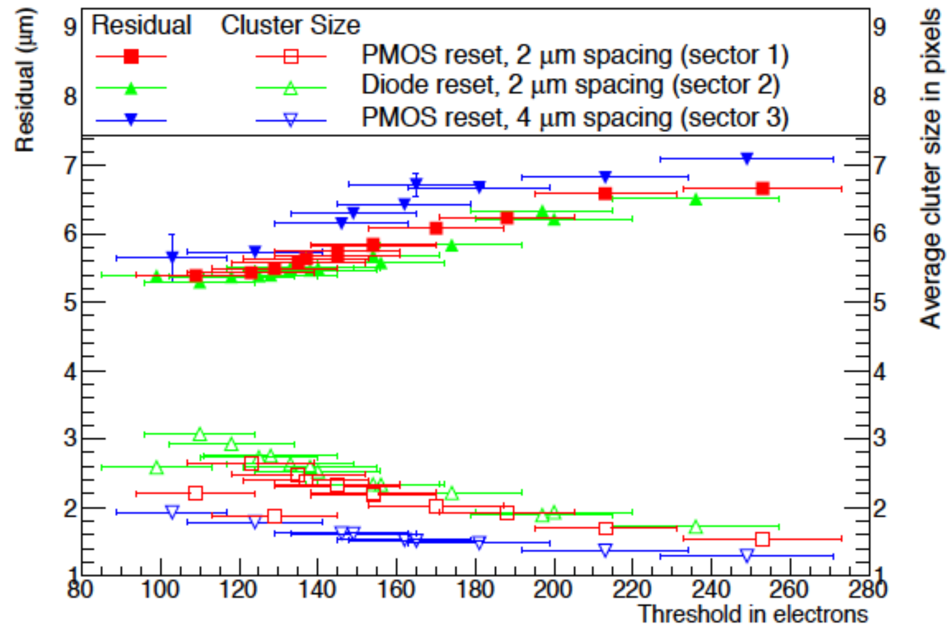
P. Yang (CERN & CCNU) – PIXEL2014

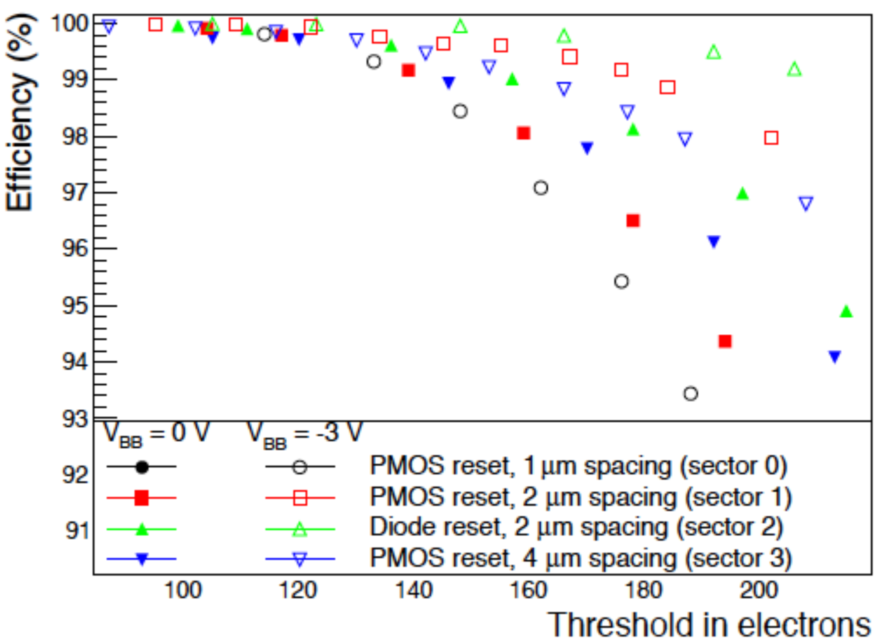


- In-matrix sparsification using priority-encoder logic
- No high-speed output link in this version

pALPIDEfs – measurements at PS test beam







- 99% efficiency at fake hit rate of 10^{-5} achievable (only 20 pixels masked) at 0V
- Reverse substrate bias (V_{BB}) provides additional margin
- Telescope based on a Stack-up of 6 or 7 layers of pALPIDEfs
- Spatial resolution (including tracking error of ~3μm): 5.5 μm