

# Readout of straws for PANDA

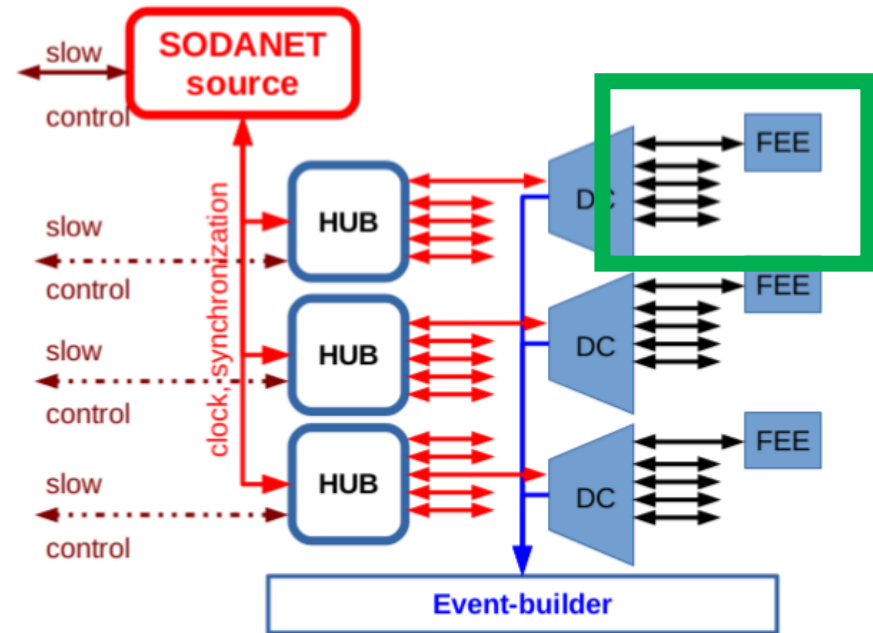
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16 January 2020, Kraków

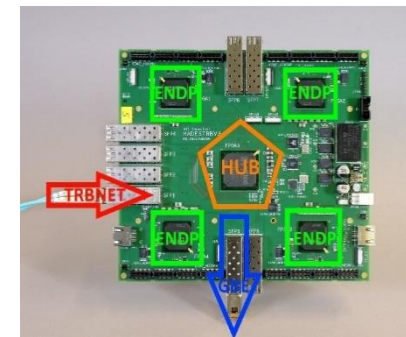
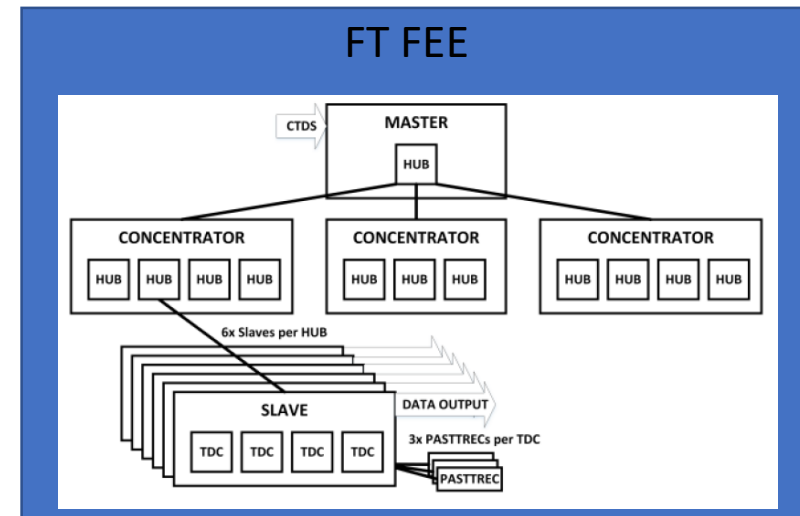
# PANDA readout concept

- Subsystems (7) have specific FEE
- All FEEs from a subsystem are connected to unified Data Concentrators
- DCs are gateways for:
  - Slow control
  - Readout data to storage
  - Time synchronisation



# Forward Tracker subsystem

- Complete system based on PASTTRECs and TRBv3
- Tested and verified under multiple experiments
- Recent deployment for HADES
- System suitable for PANDA Phase One (1/10 luminosity)



Traxler, M.; Korcyl, G.; Bayer, E.; Maier, L.; Michel, J.; Palka, M. „A compact system for high precision time measurements (<14 ps RMS) and integrated acquisition for a large number of channels“, JINST 10.1088/1748-0221/6/12/C12004

**Table 3.3:** Estimated data rates per tracking station in High Resolution mode.

Tracking station	Number of channels	Average hit rate	Maximum hit rate	Number of TRBv3s	Bandwidth	Total bandwidth
FT 1,2	2304	35 kHits/s	140 kHits/s	12	81 MB/s	972 MB/s
FT 3,4	3328	31 kHits/s	90 kHits/s	18	69 MB/s	1242 MB/s
FT 5,6	6592	9 kHits/s	39 kHits/s	35	20 MB/s	700 MB/s

# Forward Tracker subsystem

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- TRBv3 – 10 years old
- TDC implementation – 5 years old
- PANDA is supposed to be operational in 2025
- => refreshment would be welcome

# TRB platform upgrade

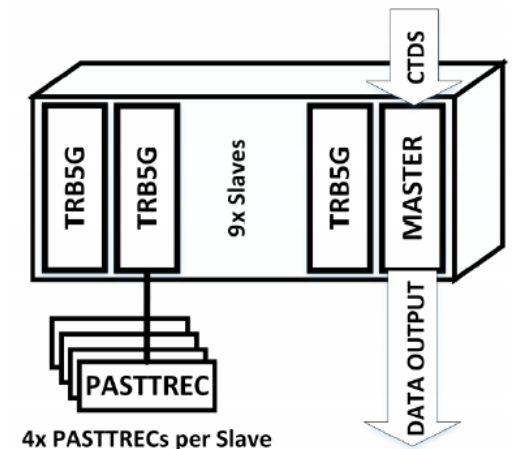
- Upgraded hardware
  - New form factor
  - Custom crate system
  - Lattice ECP5
  - Addon connector



Trb.gsi.de

**Table 3.4:** Estimated data rates per tracking station in High Luminosity mode.

Tracking station	Number of channels	Average hit rate	Maximum hit rate	Number of TRB5Gs	Bandwidth	Total bandwidth
FT 1,2	2304	350 kHits/s	1400 kHits/s	36	90 MB/s	3240 MB/s
FT 3,4	3328	310 kHits/s	900 kHits/s	52	79 MB/s	4108 MB/s
FT 5,6	6592	90 kHits/s	390 kHits/s	103	23 MB/s	2369 MB/s



4x PASTTREC per Slave

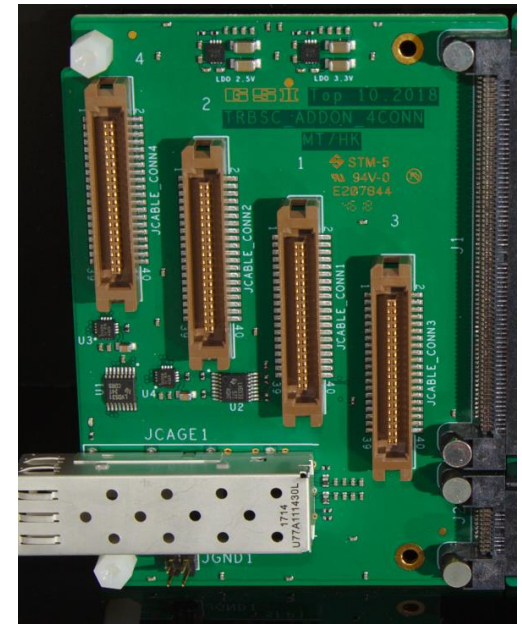
# TRB firmware development

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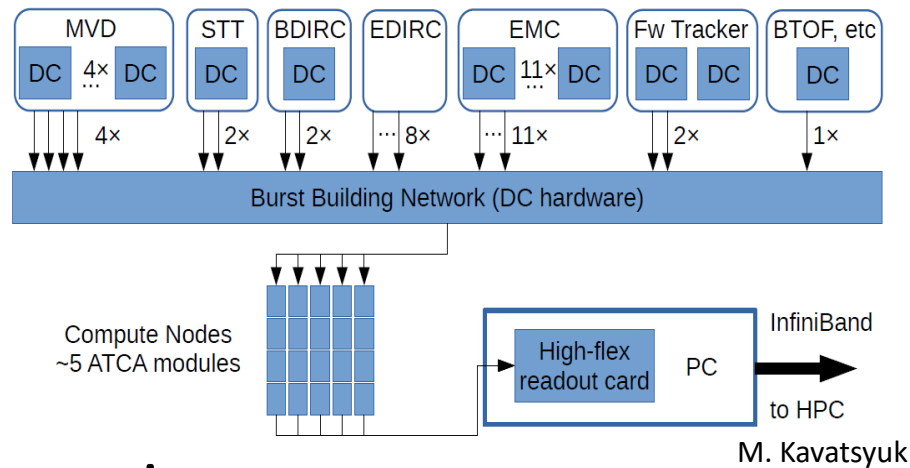
- New FPGA -> possibility for a new TDC
  - Lower resolution
  - No delay chain – oversampling with phase-shifted clocks
  - Higher channel count – 4x PASTTREC boards per FPGA
  - New data format with lower overhead
  - Time sorted hits
  - Work in progress – cooperation with PK - M. Michałek
- Communication features
  - Most TrbNet components to be migrated
  - Gigabit Ethernet requires fixes
  - SodaNet to be migrated
  - Connection to Data Concentrator to be developed

# Hardware development

- TRB5 – PASTTREC Addon
  - Fix pseudo-SPI interface
  
- Crate controller
  - Local data concentrator via backplane
  - SodaNet receiver and hub
  - Data Concentrator output
  - Xilinx FPGA



# PANDA complete readout



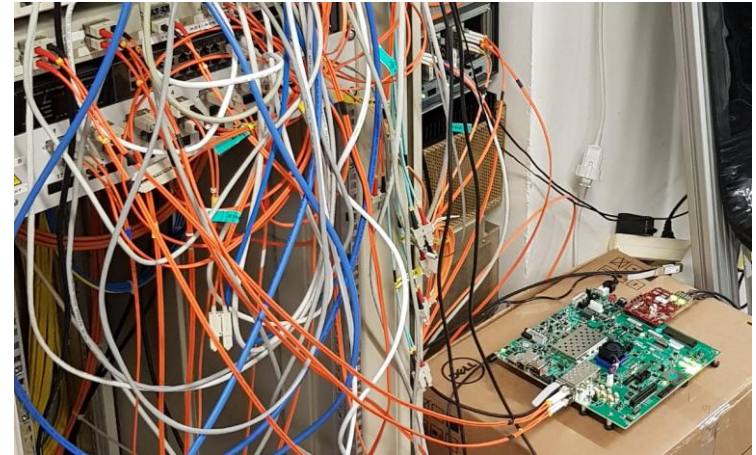
- Minimum requirement
  - Deliver raw data to the Data Concentrators
- Additional module for preprocessing and online tracking
  - Between TRB crates and Data Concentrator



# Intermediate module

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- Performs:
  - Data aggregation
  - Hit sorting
  - Clustering
  - Filtering
  - Tracking
  
- Prototype developed on ZCU102 platform
  - 2x inputs, GbE data streams from TRBv3
  - 2x output, GbE and to the Compute Node
  
  - Tested during 2019 Juelich beamtime
  - Filtering only, data to be analyzed
  
- Firmware to be developed
- Possibility to develop the hardware as well



# Work Packages

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## 1. TRB5 readout board

- Firmware:
  - New TDC implementation
  - PASTTREC controller
  - Communication infrastructure
- Hardware:
  - PASTTREC Addon

## 2. Crate controller

- Firmware:
  - Data aggregation
  - Hit sorting
  - SodaNet
  - Data Concentrator link
- Hardware:
  - Entire board

## 3. Intermediate board

- Firmware:
  - Full online tracking pipeline
- Hardware:
  - Design or commercial

## 4. Support and maintenance

