SMX2.1, a 128 Channel, Event-Driven Tracking Chip for Silicon and Gaseous Detectors

Krzysztof Kasinski, Robert Szczygiel, Weronika Zubrzycka, Rafal Kleczek, Piotr Otfinowski[1]
Ralf Kapell, Piotr Koczon, Joerg Lehnert, Anton Lymanets, Osnan Maragoto-Rodriguez,
Adrian Rodriguez-Rodriguez, Christian J. Schmidt, Carmen Simons[2]
Wojciech Zabolotny, Marek Guminski, Adrian Byszuk[3]

for the CBM Collaboration

[1]AGH University of Science and Technology, Cracow, Poland
[2]GSI Helmholtzzentrum fuer Schwerionenforschung GmbH, Darmstadt, Germany
[3]Warsaw University of Technology,Warsaw, Poland

Facility for Antiproton & Ion Research

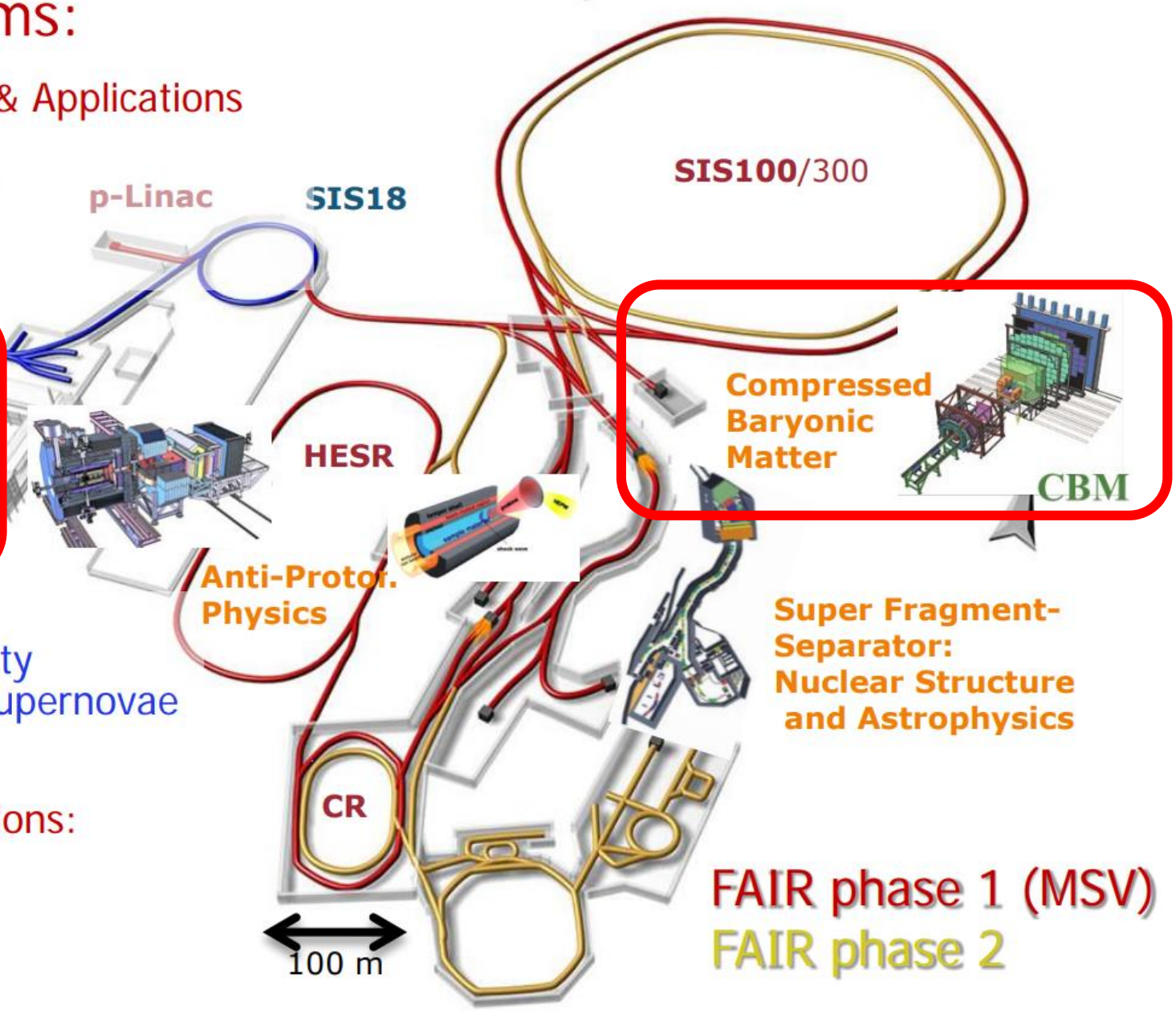
Experimental programs:

APPA: Atomic & Plasma Physics & Applications
- Highly charged atoms
- Plasma physics
- Radiobiology
- Material science

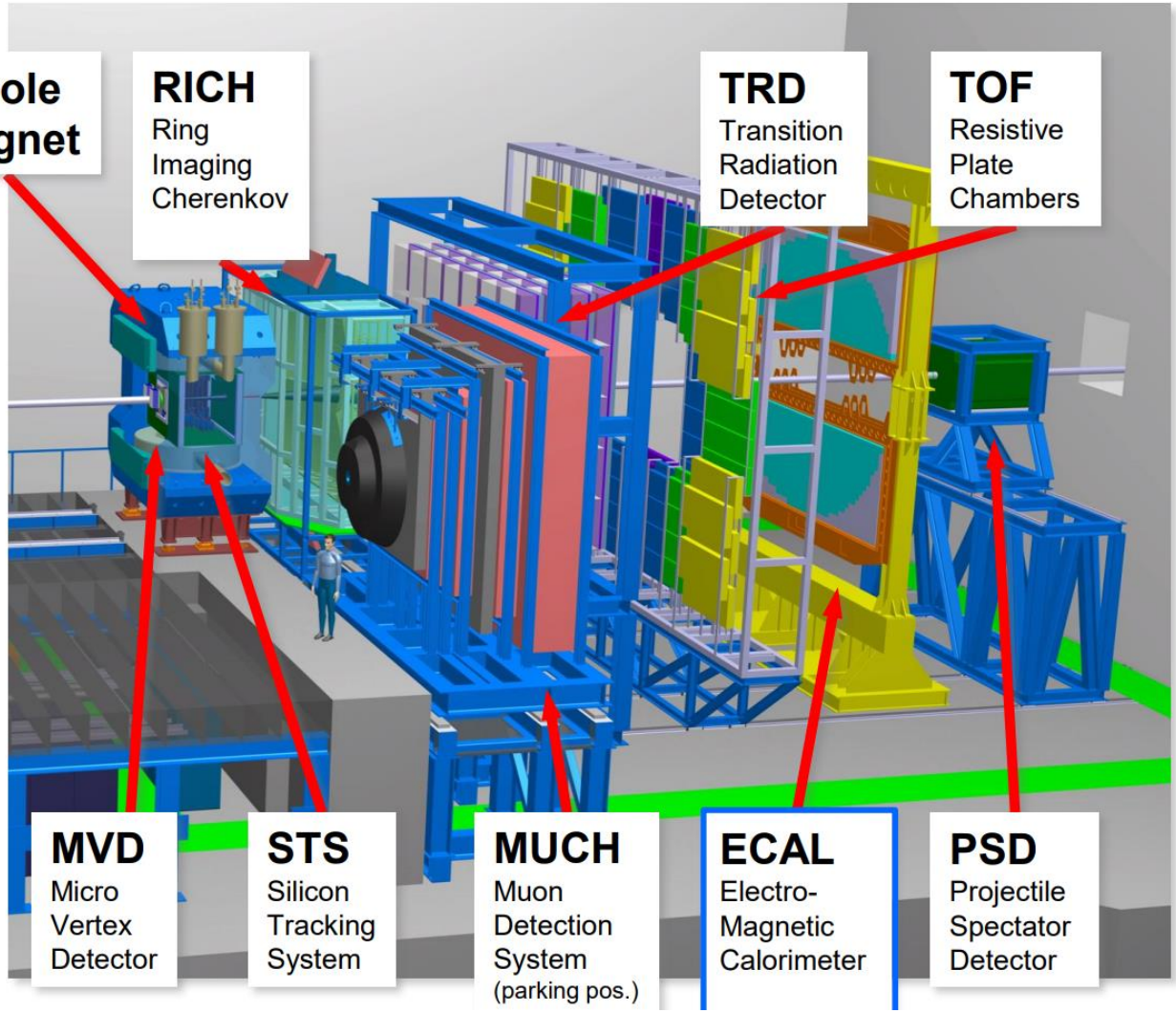
CBM: Nucleus-nucleus collisions
- Nuclear matter at neutron star core densities
- Phase transitions from hadrons to quarks

NUSTAR: Rare Isotope beams
- Nuclear structure far off stability
- Nucleosynthesis in stars and supernovae

PANDA: Antiproton-proton collisions:
- Charmed hadrons (XYZ)
- Gluonic matter and hybrids
- Hadron structure
- Double Lambda hypernuclei



CBM Detector Structure

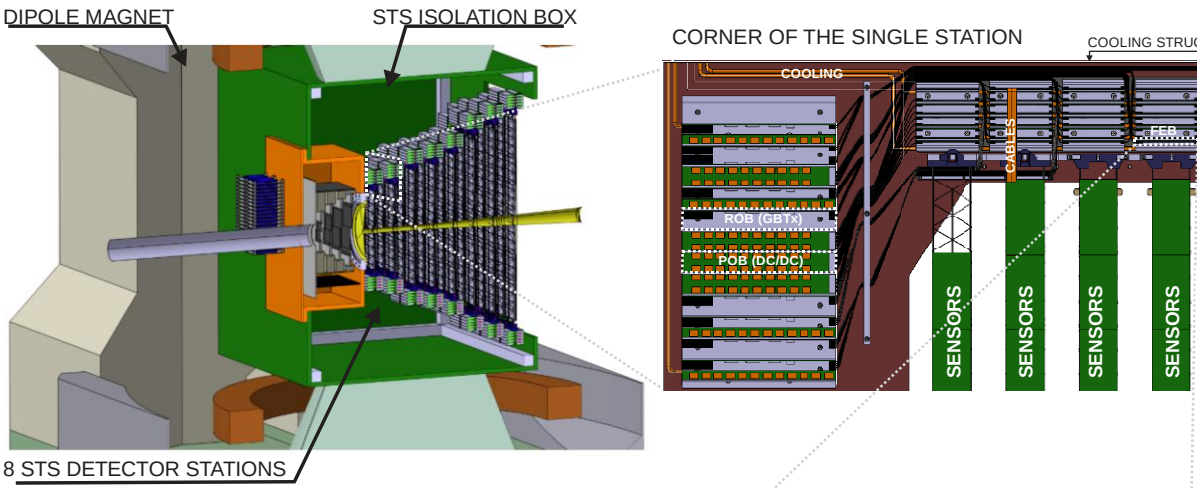


- Tracking acceptance: $2° < \theta_{lab} < 25°$
- Free streaming DAQ
- R_{int} = 10 MHz (Au+Au)

  $R_{int} \approx 0.5$ MHz
  full bandwith:
  Det. – Entry nodes
  reduced bandwidth
  Entry nodes – Comp. farm

  with
  R_{int} (MVD)=0.1 MHz
- Software based event selection

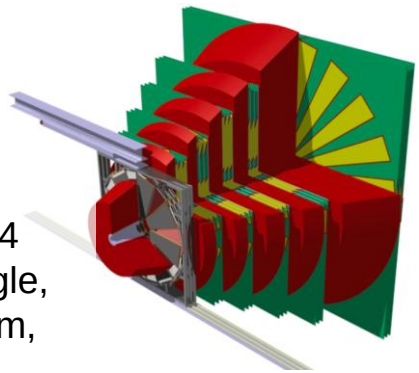
STS



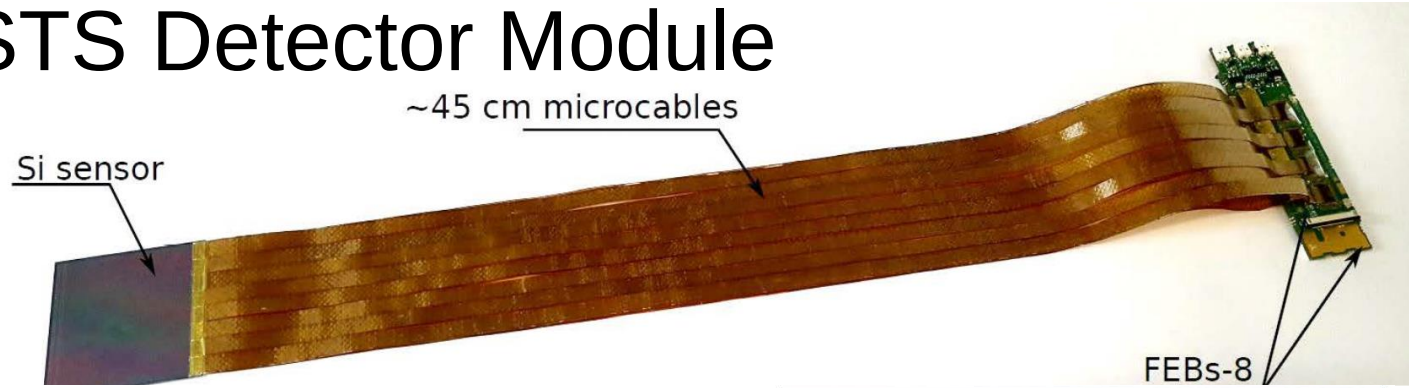
STS metrics:
>1 790 000 channels
>14 000 ASICs
1752 FEBs
600 ROBs, 78 DPB s

double–sided, micro-strip, 1024 channels per side, 7.5°stereo angle, **58 *μ*m pitch**, lengths 20 - 120 mm, 300 *μ*m thickness,

MUCH



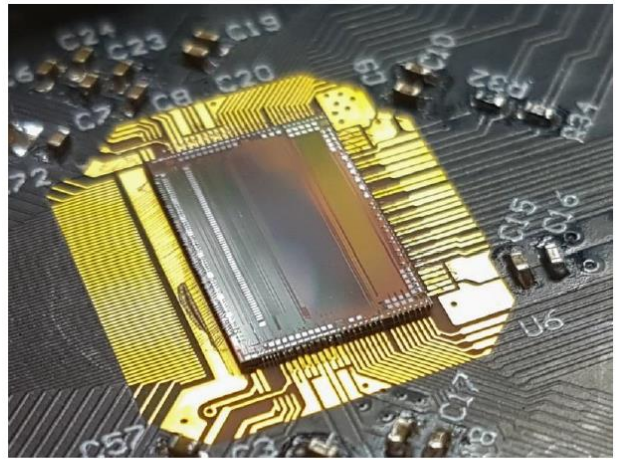
STS Detector Module

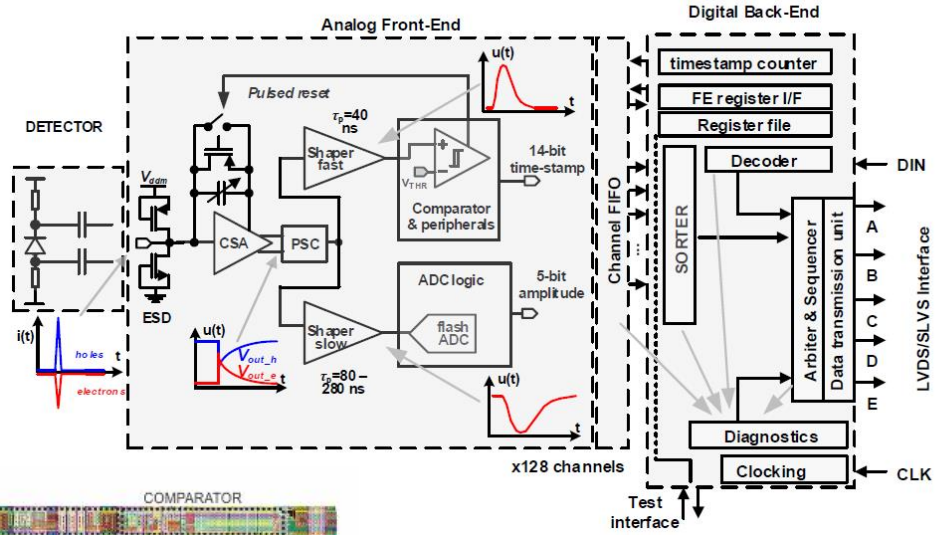


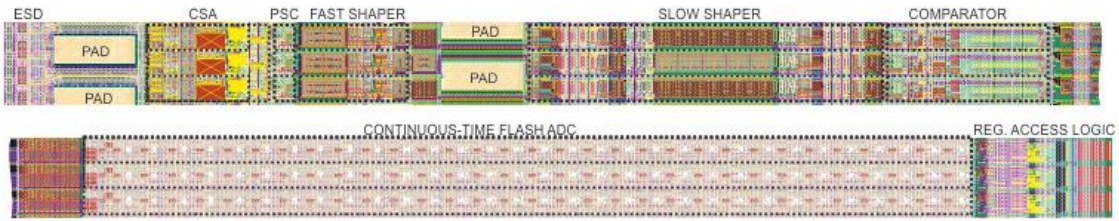
SMX chip

Features:

- Low power, self-triggering ASIC
- 128 channels + 2 test channels
- Time resolution ~ 5 ns
- Provides digitized hits with:
  - 5 bit Energy Resolution.
  - 14 bit Time stamp.
- Linearity range up to 15 fC
- Radiation hard layout





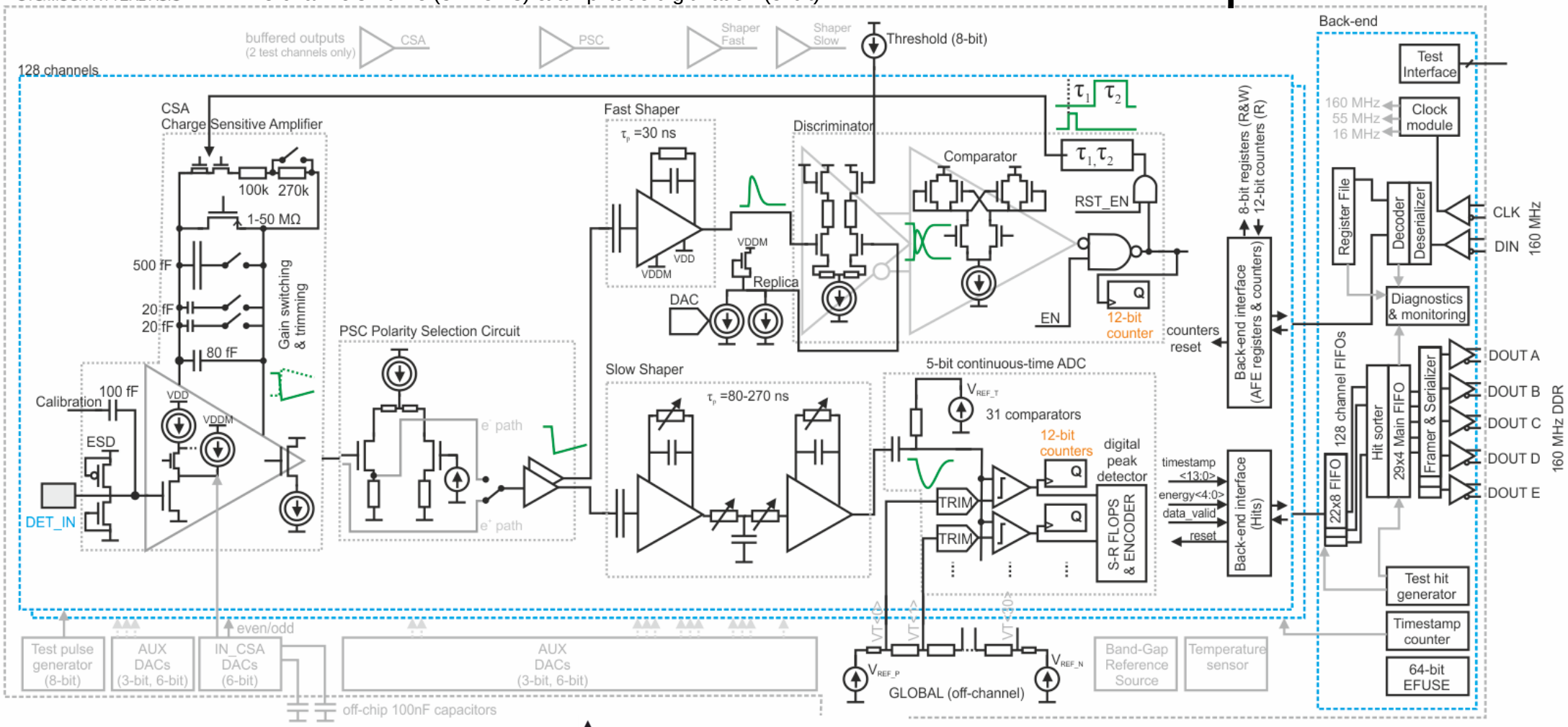


Parameter	Value
Process	180 nm CMOS MM/RF
Chip area	10.0 mm × 6.75 mm
Channel number	128 + 2 test
ADC bits	5
Input charge frequency	max. 500 kHz
Power Consumption: Uninitialized Initialized	 0.6 – 1.2 W/chip 1.023 W/chip @ I_d=2 mA 8 mW/channel
Offset spread of fast channel	1.12 mV rms / 0.015 fC rms (after correction)
Offset spread of ADC [fC]	0.09 (before correction) [39] 0.02 (after correction)
Gain Fast shaper (STS) Slow shaper (STS)	 73 mV/fC 32.7 mV/fC
Gain spread: Fast shaper Slow shaper	 0.8 % 0.5 % (after calibration)
Slow shaper peaking time [ns]	90 / 180 / 262 / 332
Yield	>91% (146 ASICs tested on PCBs)

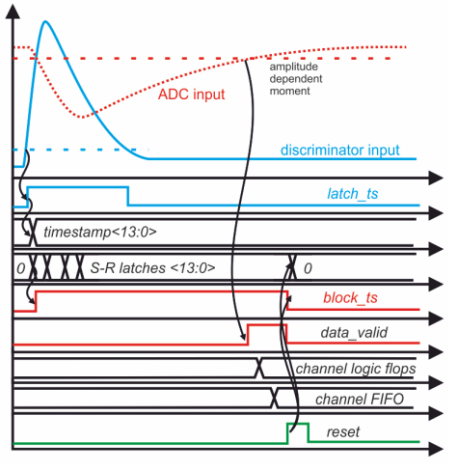
SMX 2.1 Chip architecture

STS/MUCH-XYTER2 ASIC

128 channels - time (3.125 ns) & amplitude digitization (5-bit)

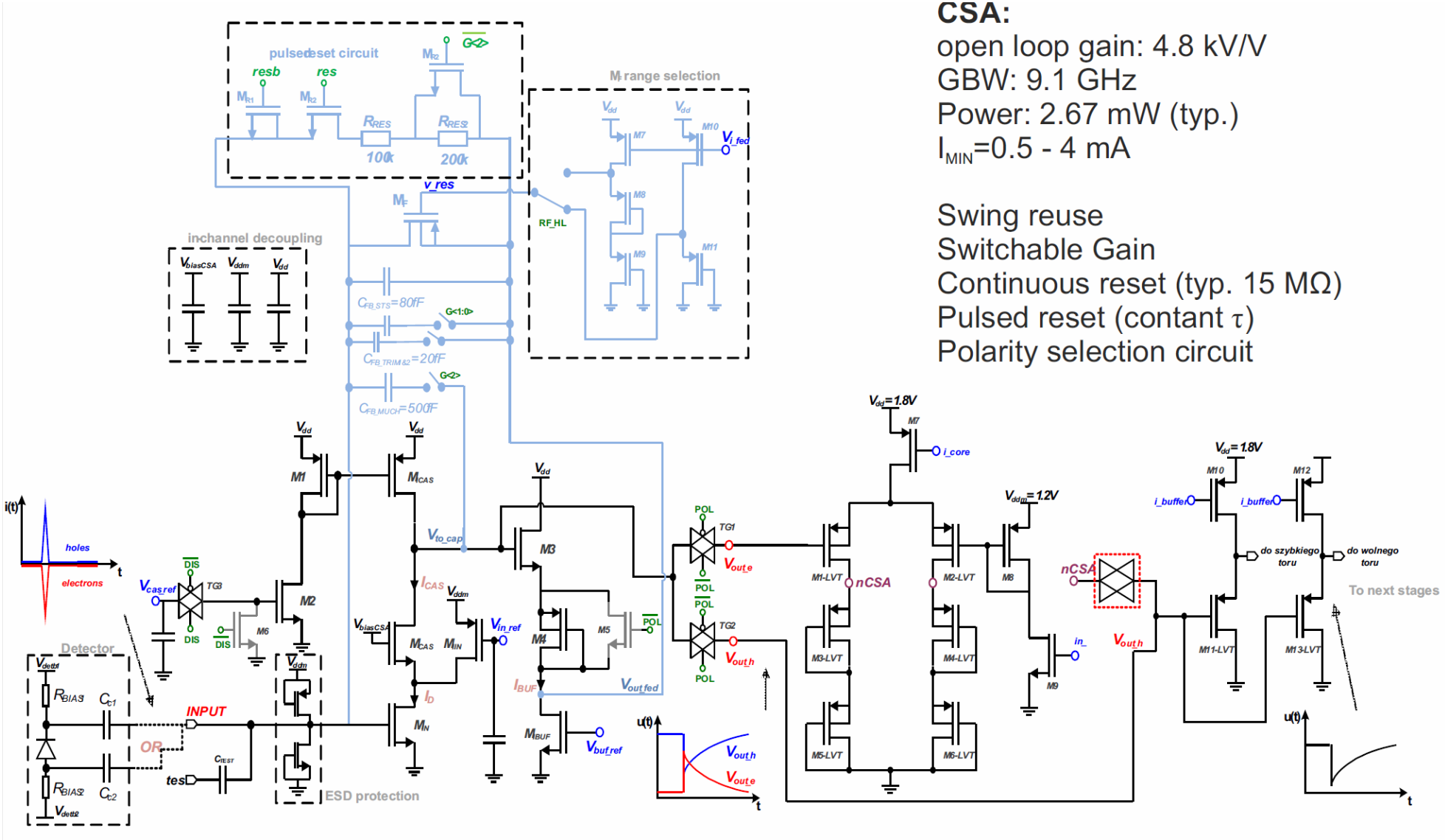


0-12 fC electrons & holes (STS)
gain switching & trimming
250 khit/s rate (pulsed reset)
80-280 ns shaping time (slow path)
time-walk corrected offline
continuous-time ADC + peak det.
P=8.5-10 mW/channel (incl. logic)



Back-end:
- control via synthesized reg & AFE DICE cells
- 9.41 – 47 Mhit/s/ASIC data BW
- dedicated protocol
- throttling, diagnostic features
- link loopback (multi-level)
- 64-bit e-fuse for traceability

Schematic of the CSA amplifier and PSC circuit



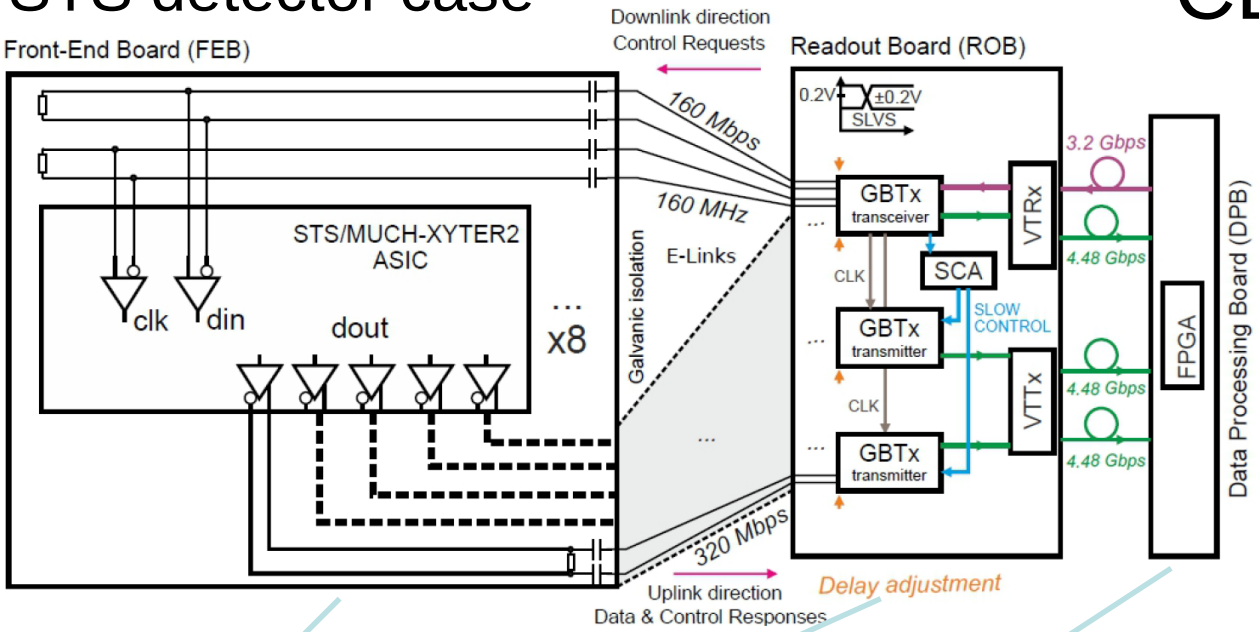
CSA:

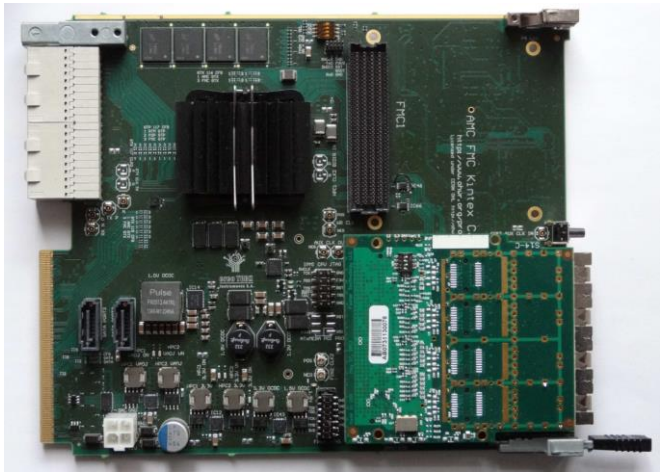
open loop gain: 4.8 kV/V
GBW: 9.1 GHz
Power: 2.67 mW (typ.)
I_{MIN}=0.5 - 4 mA

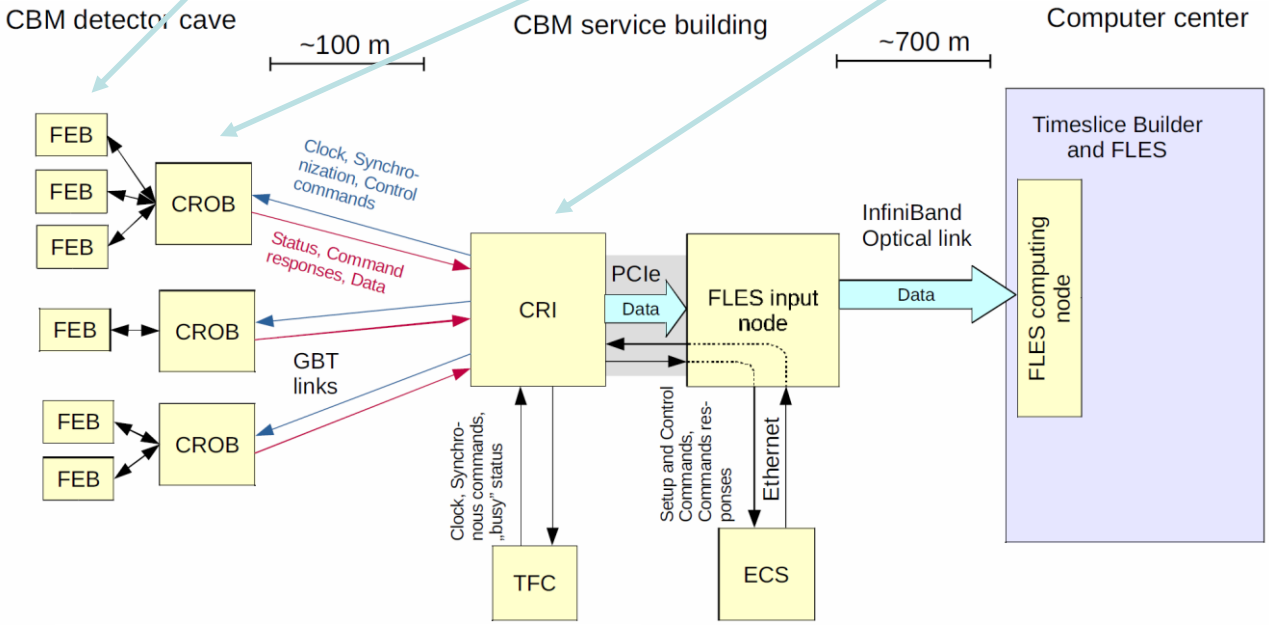
Swing reuse
Switchable Gain
Continuous reset (typ. 15 MΩ)
Pulsed reset (contant τ)
Polarity selection circuit

CBM DAQ system

STS detector case







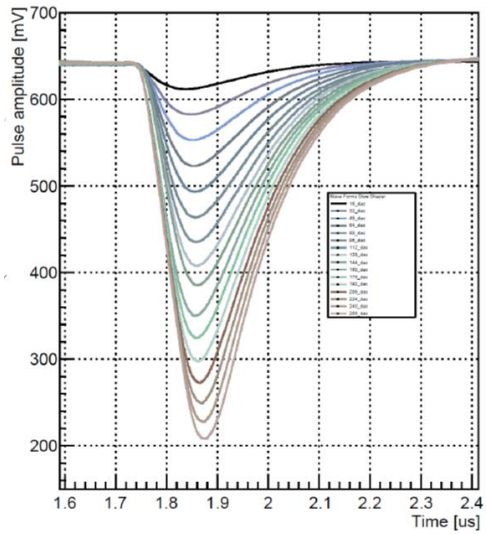
General CBM DAQ structure

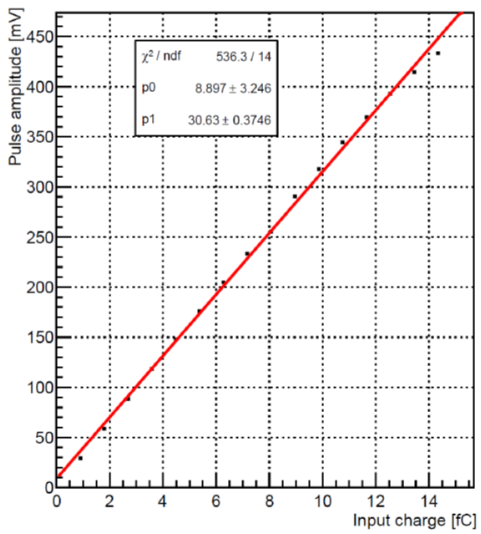
The DPB/CRI boards are responsible for:

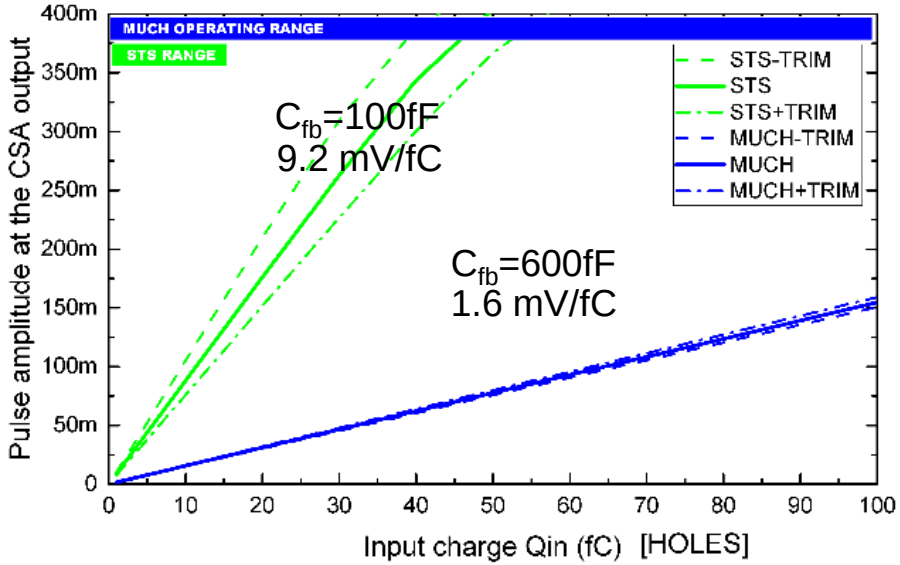
* communication with GBTx ASICs via 4.8 Gb/s optical link
* reference clock receive and its delivery to the FEE
* providing communication with Experiment Control System
* control command and responses to and from FEE
* time-deterministic fast control commands to the FEE
* concentration or aggregation of data delivered by the FEE ASICs (SMX2.1 in case of STS, or MUCH, Spadic in case of TRD)
* transmission of the aggregated data to DAQ via 10 Gb/s optical link (DPB) or PCIe (CRI).

Measurements: Analog waveforms

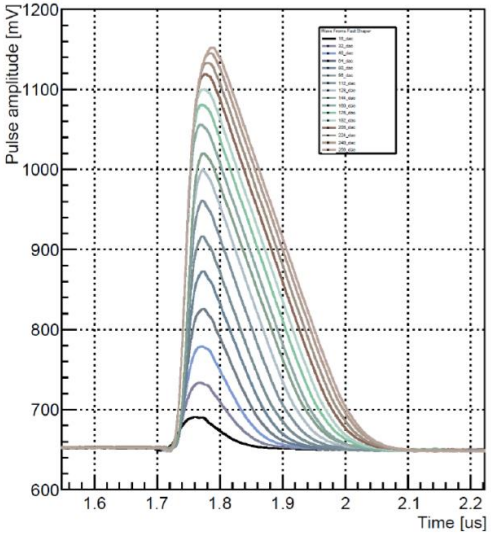
Slow shaper (STS mode)

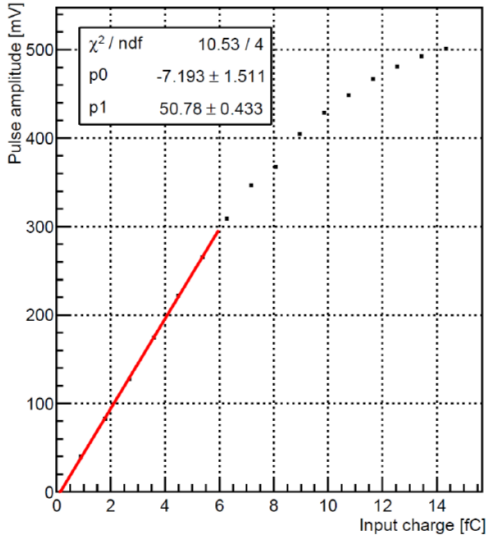


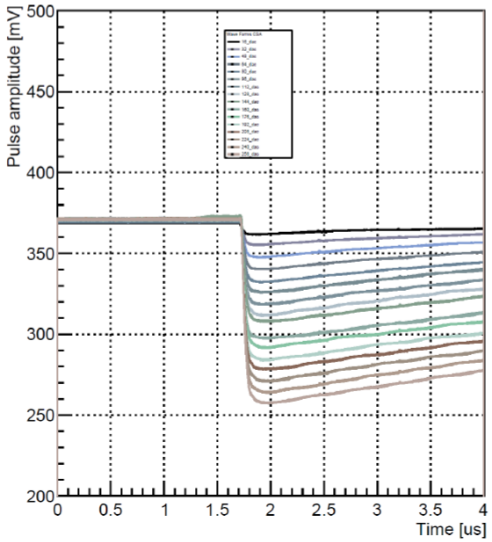




Fast shaper (STS mode)







Charge-sensitive amplifier

Electrons

IFED 7	τ = 0,33µs
IFED 16	τ = 0,61µs
IFED 32	τ = 1,08µs
IFED 48	τ = 1,44µs
IFED 63	τ = 1,50µs

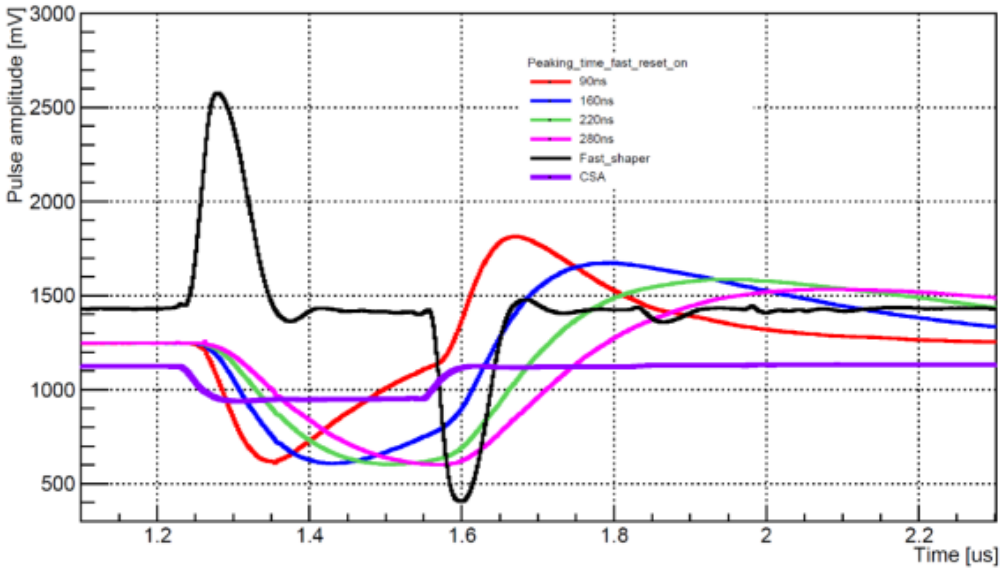
Holes

IFED 7	τ = 0,73µs
IFED 16	τ = 3,17µs
IFED 32	τ = 5,81µs
IFED 48	τ = 29,24µs
IFED 63	τ = 59,01µs

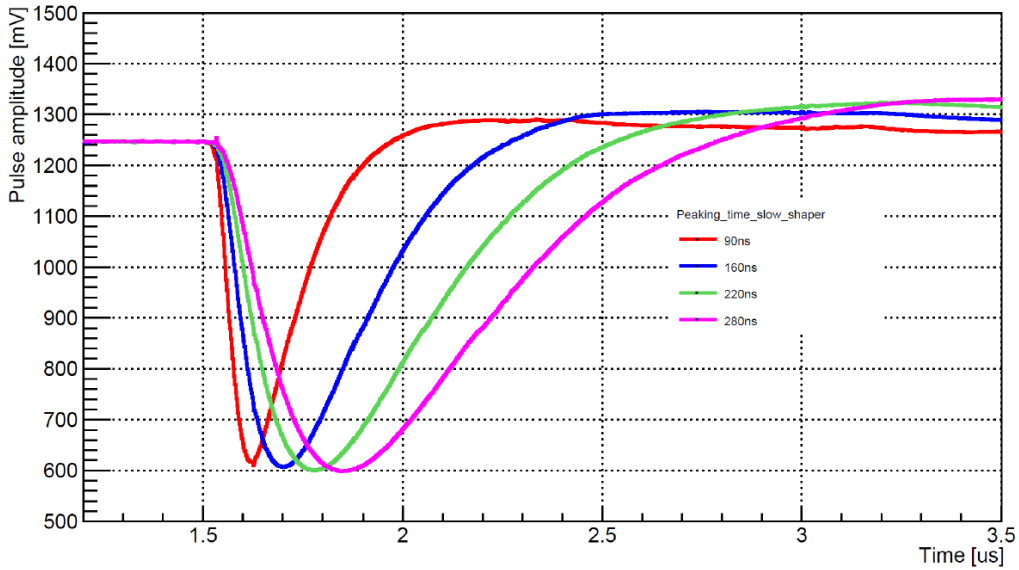
Measurements: selectable peaking times and fast reset

WF @ 10fC for different peaking times & fast reset On

Holes



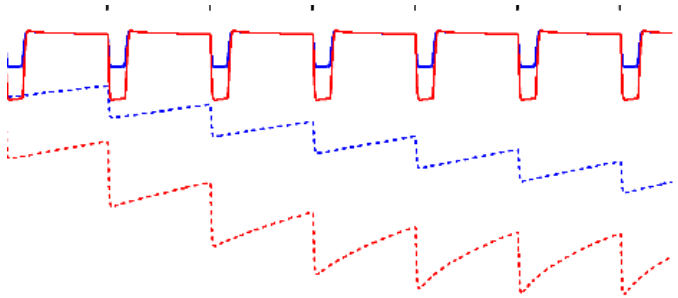
Selectable peaking time



Optimization towards varying dominant noise contributors.

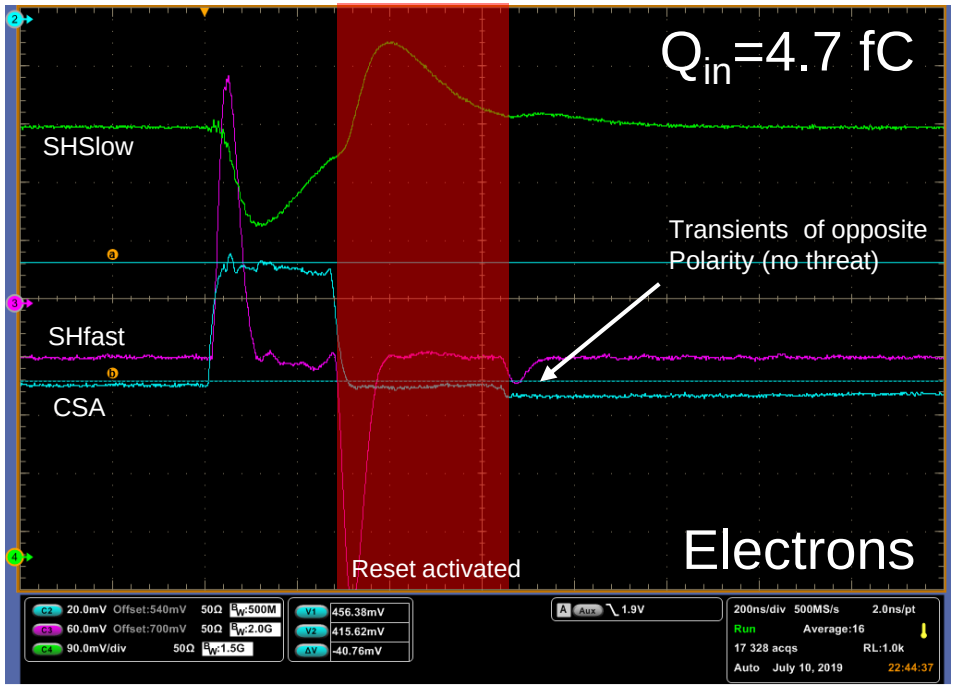
• CSA fast reset (baseline recovery). Reset procedure takes some time (150ns + 250ns)

• Reset itself causes dead time for shortest peaking times (e.g. pulses, which would be injected in this time frame will be lost).

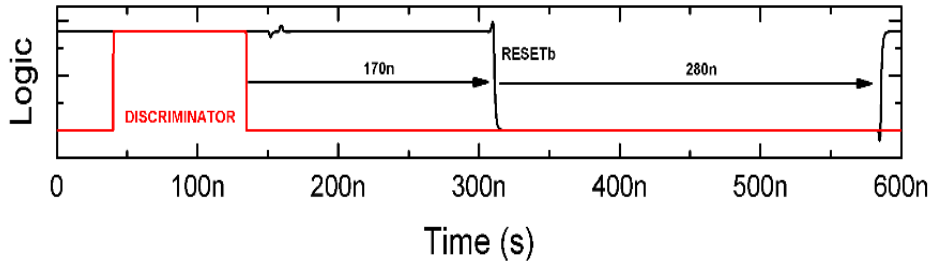


Optimization towards varying dominant noise contributors.

CSA reset for baseline recovery

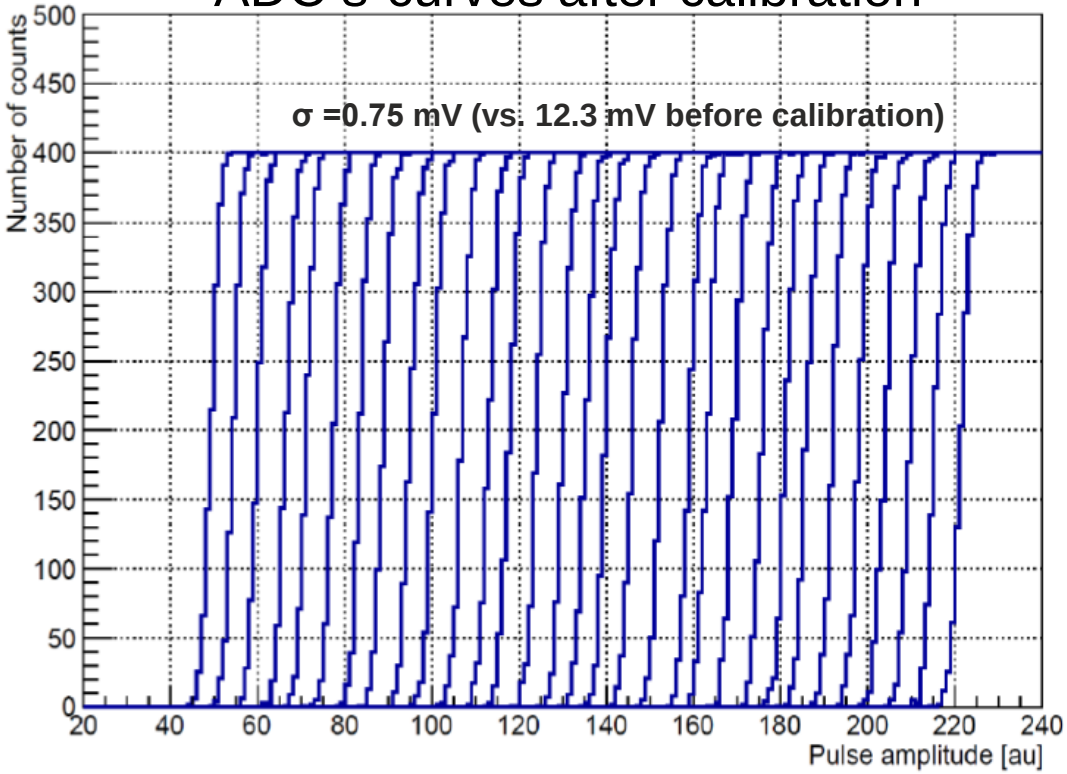


- Fast reset does not always help
- Intrinsic dead time decreases double pulse performance but helps withstanding long pulse trains (with the same AFE conditions)
- Modification for final ASIC: shortening both trigger time and reset time

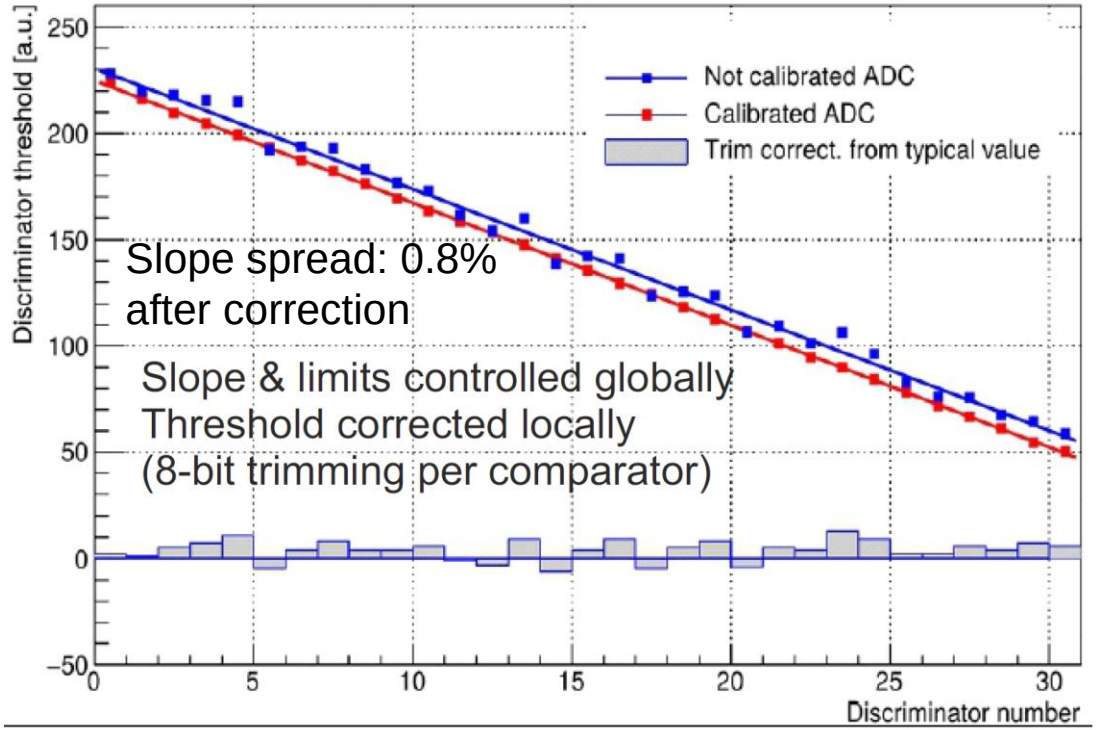


Measurements – in-channel 5-bit ADC

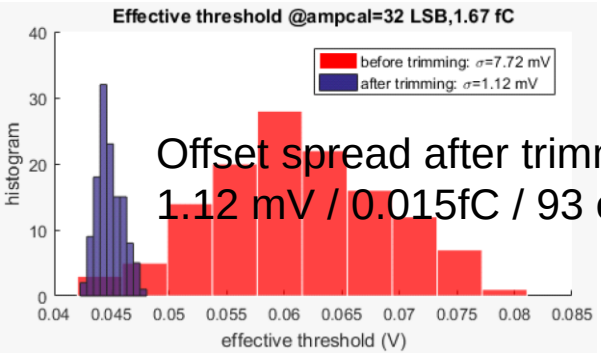
ADC s-curves after calibration



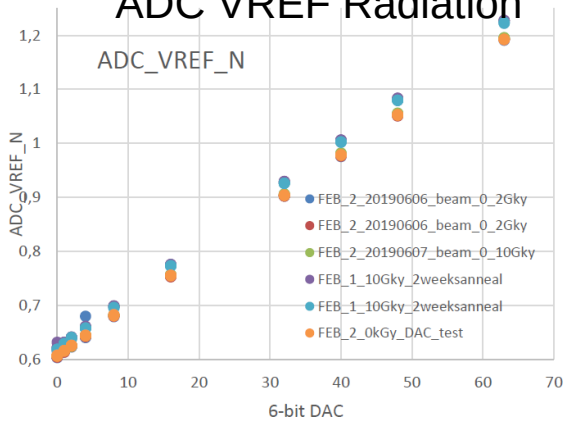
ADC Linearity



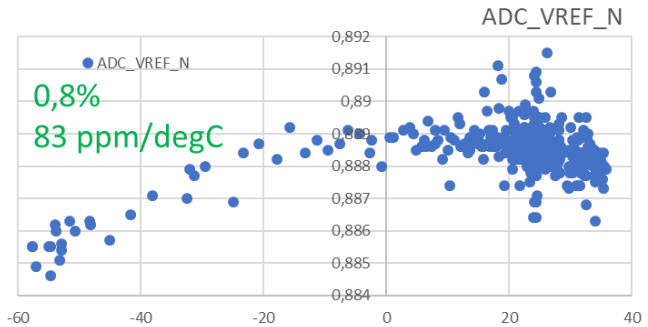
Fast comparator offset calibration



ADC VREF Radiation

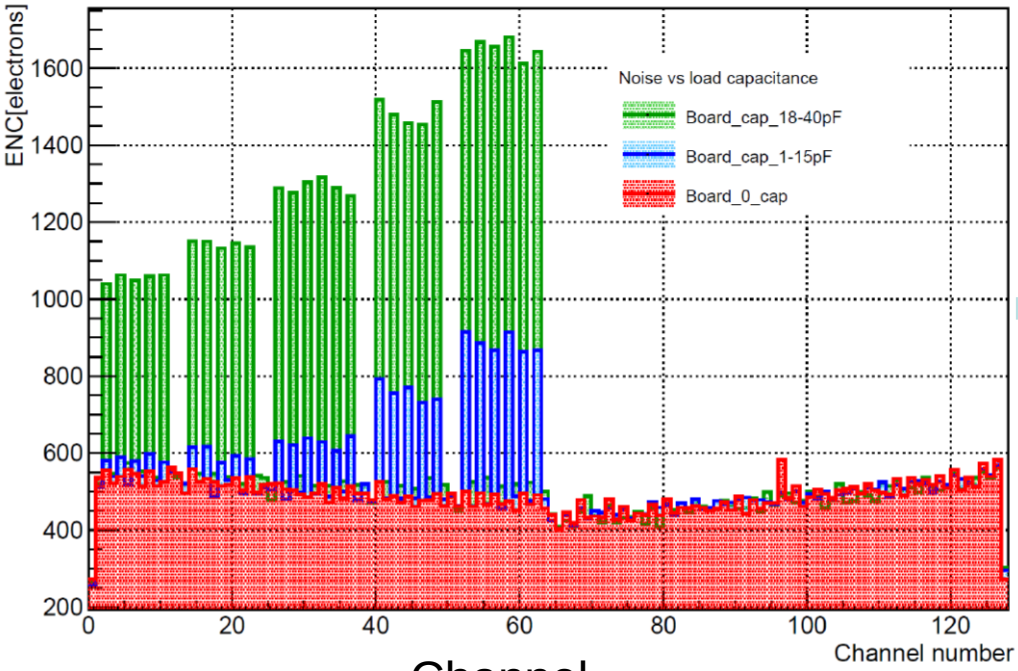


ADC VREF Tempco

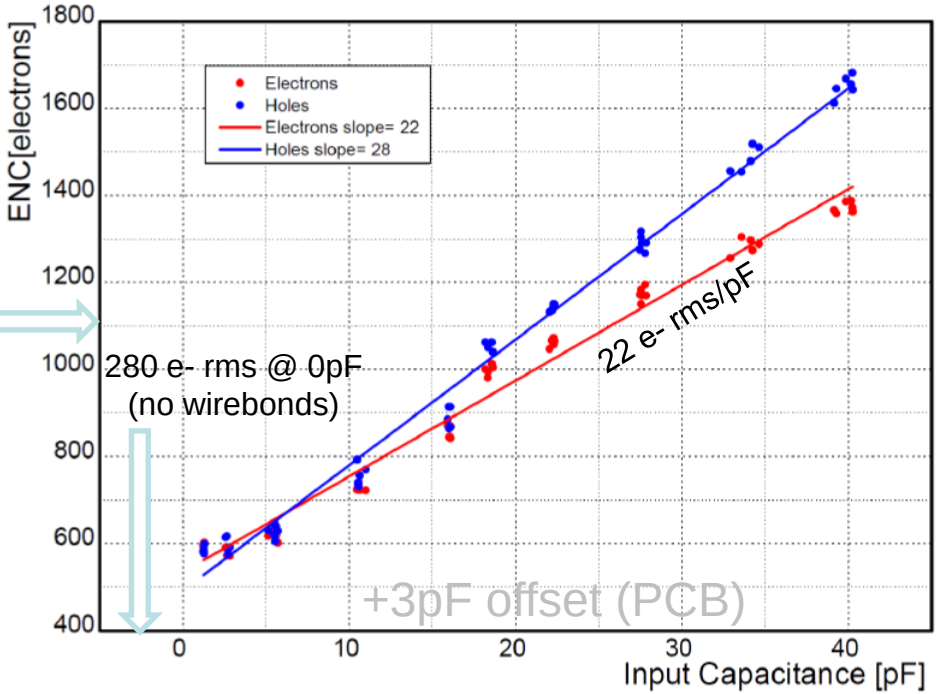


Measurements – noise performance

External C0G capacitors

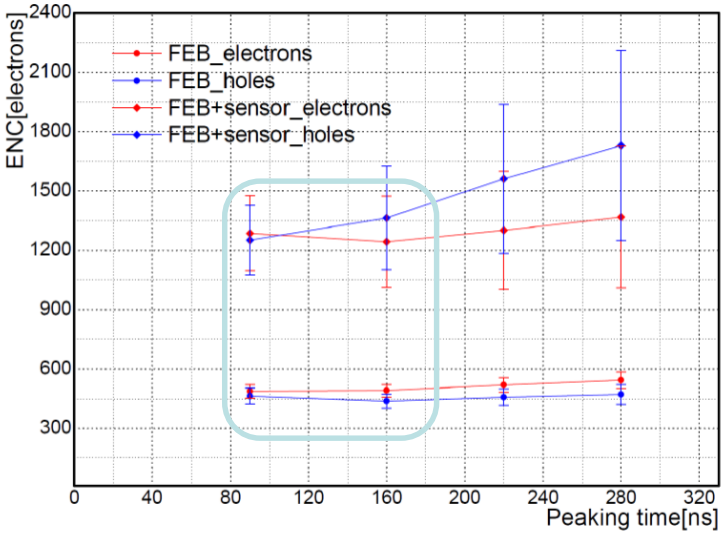


Channel



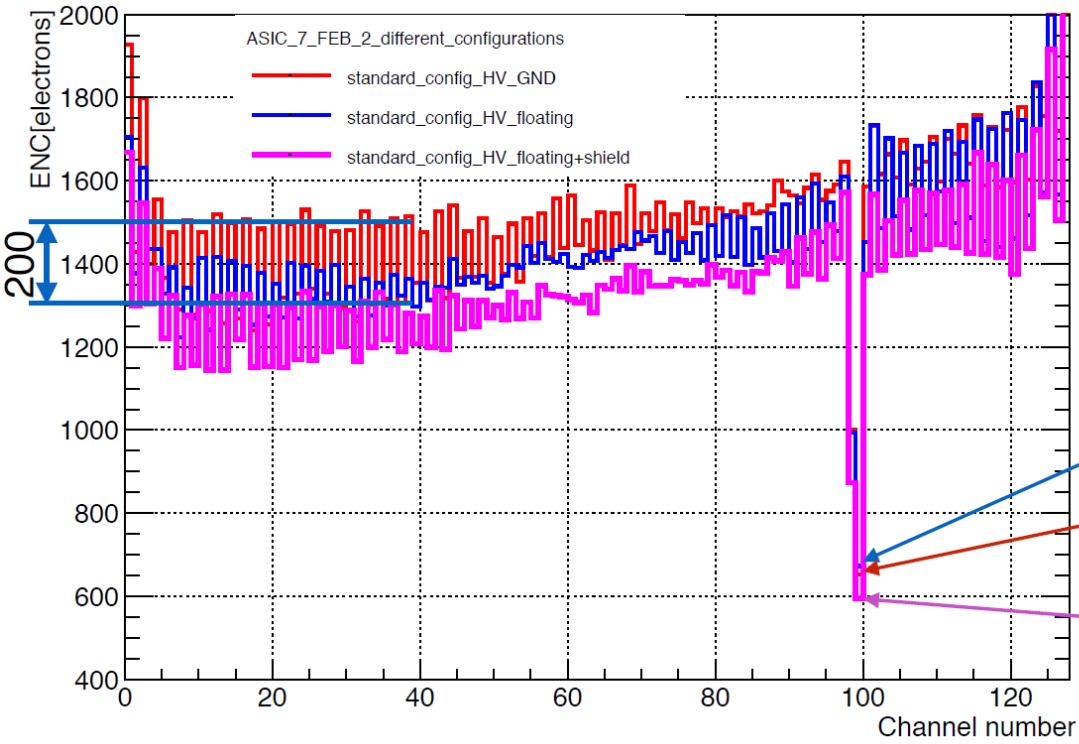
ASICv2.1 Setup with sensor

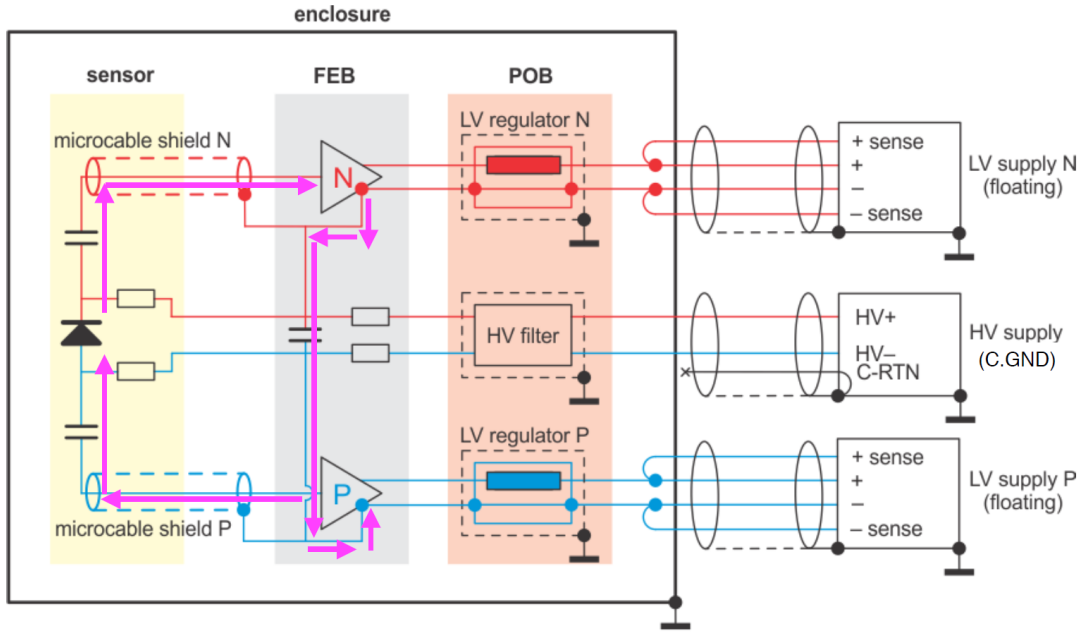
Best noise for two shortest peaking times



System Noise Studies

- Standard configuration:
  - ISEG MPOD HV
  - Wiener LV
- Tested configurations:
  - STD with mSTS box grounded
  - STD without box GND
  - Keithley 2410 as HV
  - Battery as LV + MPOD as HV
  - Battery as LV + Keithley 2410 as HV



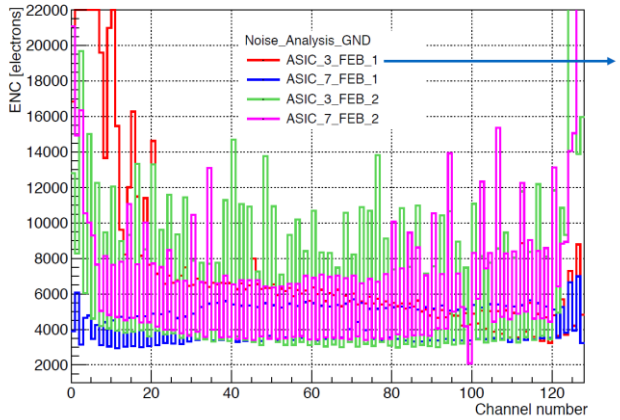


HV FLT: 670 e

HV GND: 655 e

HV FLT+ SHLD_GND: 590 e

Standard configuration + GND box



Best performance: floating HV power supply + grounded HV cable shield

- The difference between the best and the worst case is ca. 200 e.
- Noise performance of 1200 e is achievable.

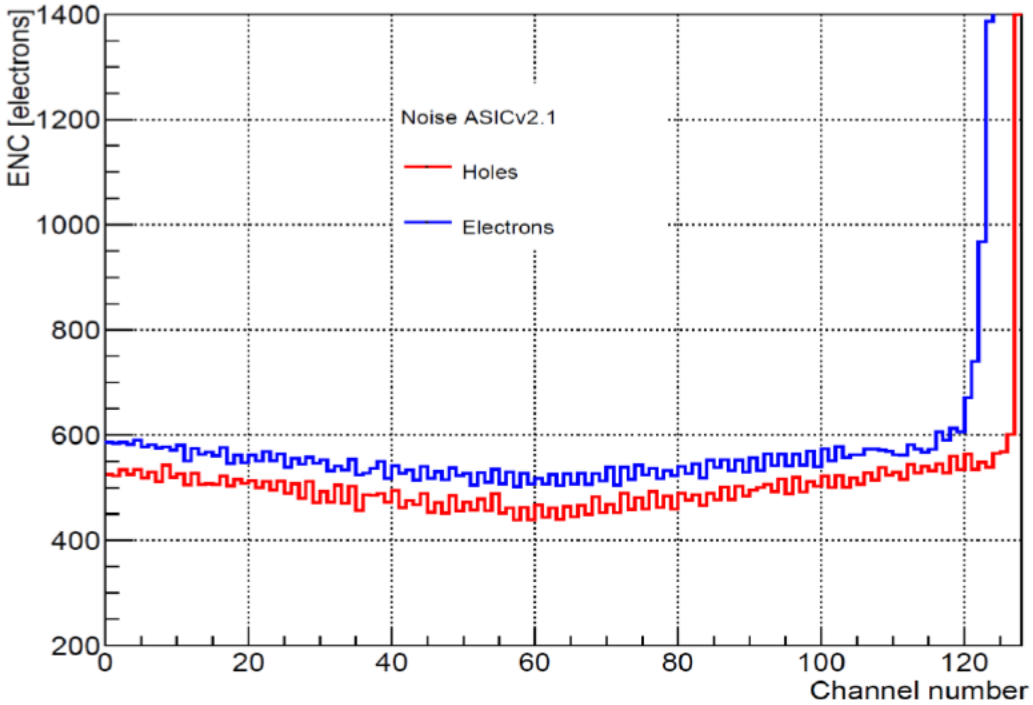
Courtesy: Anton Lymanets

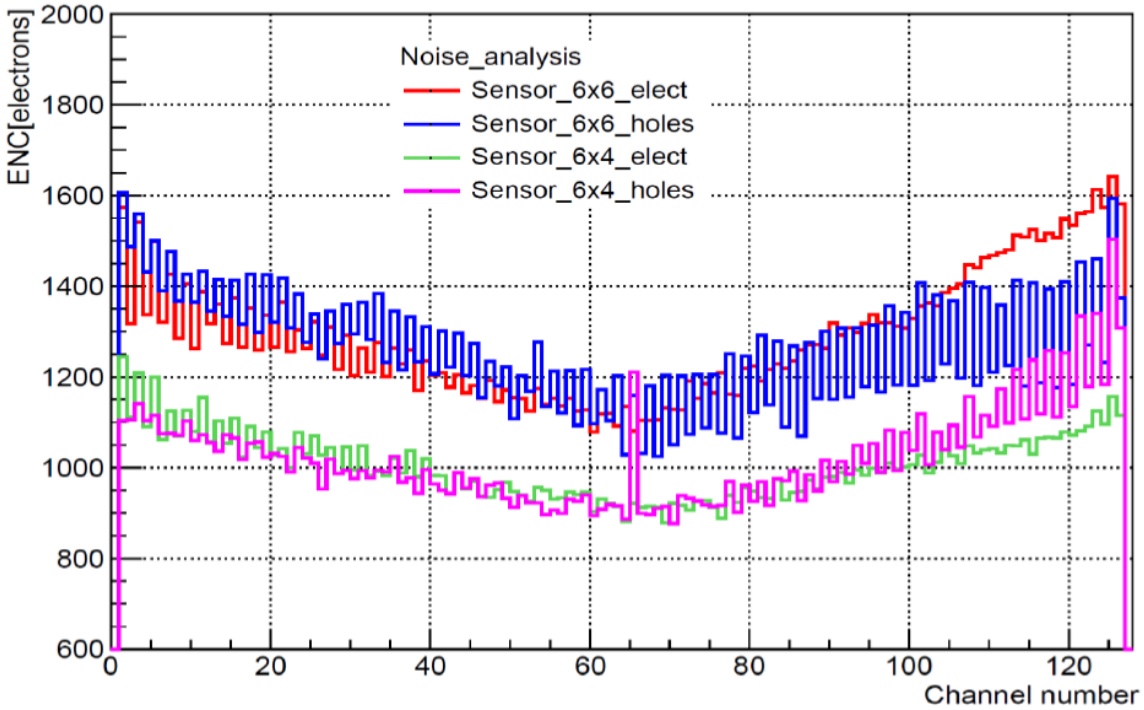
Measurements – noise performance with sensor

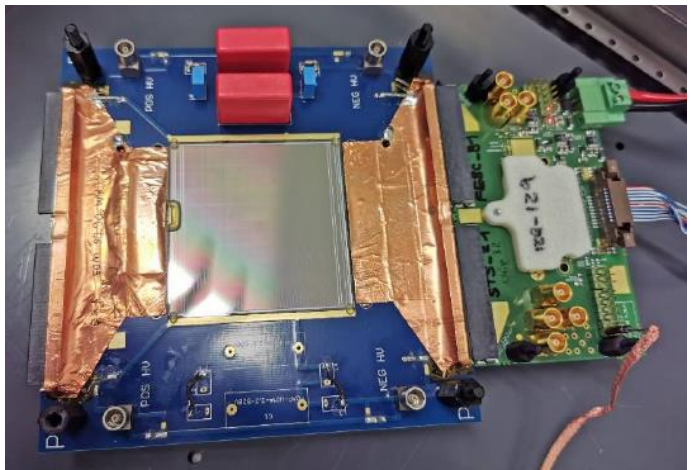
Single ASIC+FEB-C

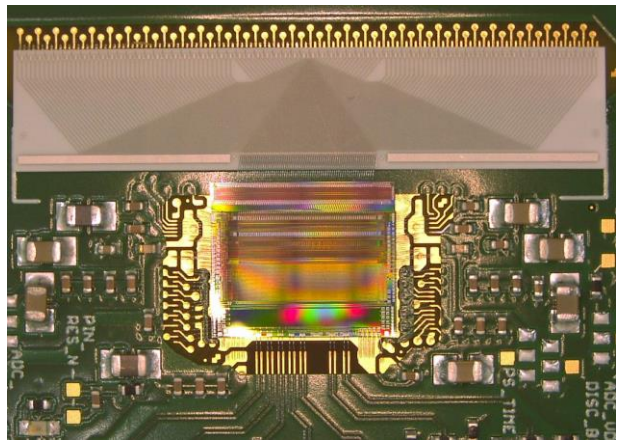
ASICv2.1

Hamamatsu Sensor (6x6cm^2 & 6x4cm^2) in PCB + FEB-C+ASICv2.1



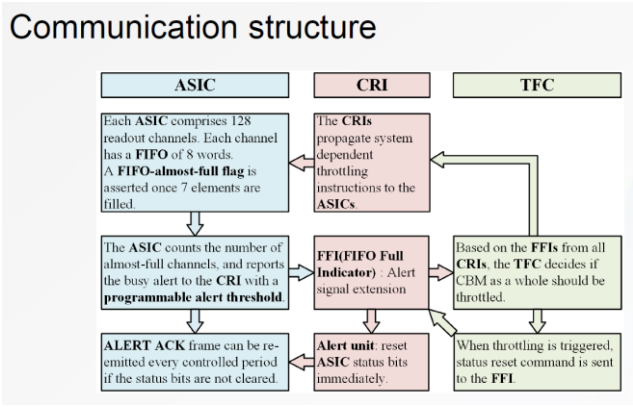


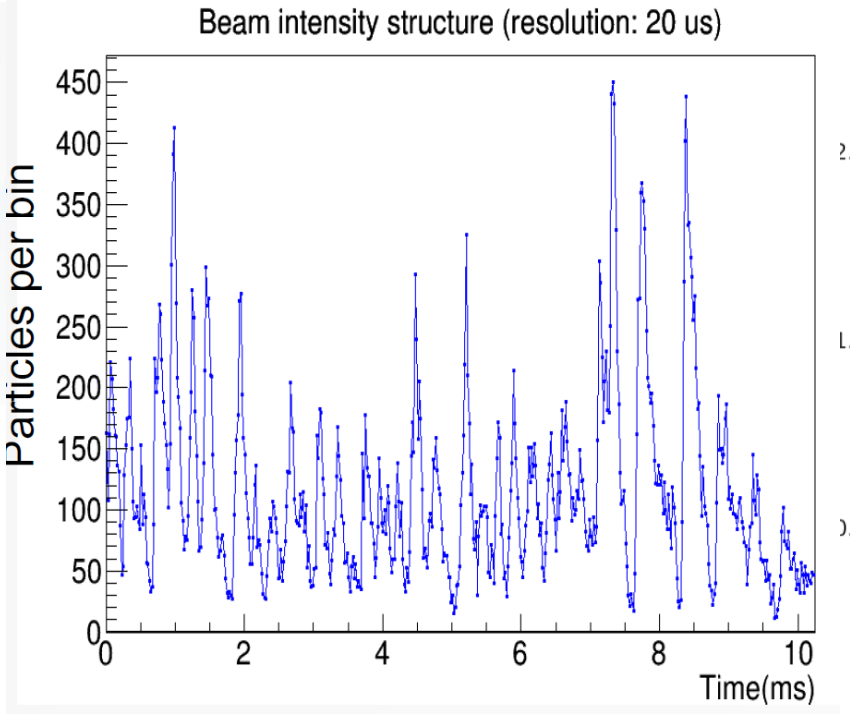


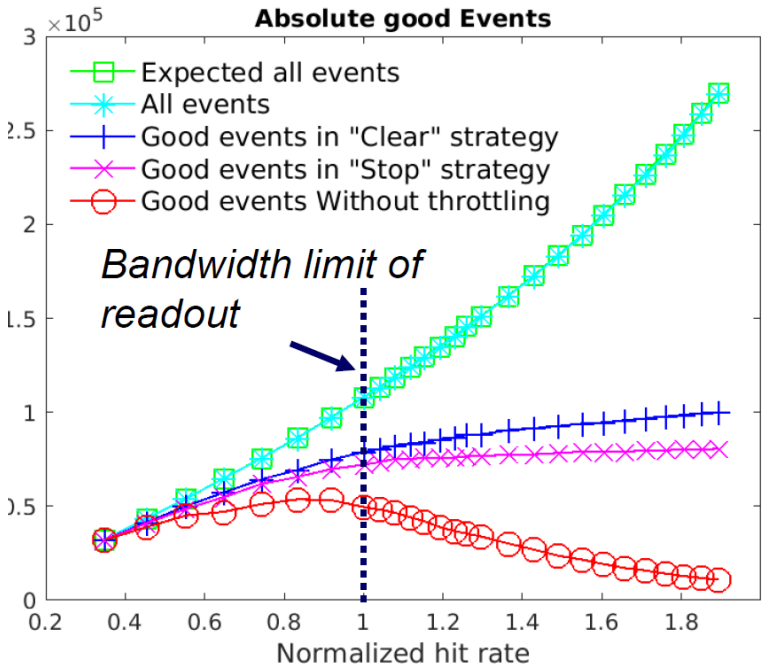


Throttling

Simulation with realistic beam intensity fluctuation. The average event rate ∝beam intensity; Beam intensity resolution is 20us. The event rates obey Poisson process during each 20us.



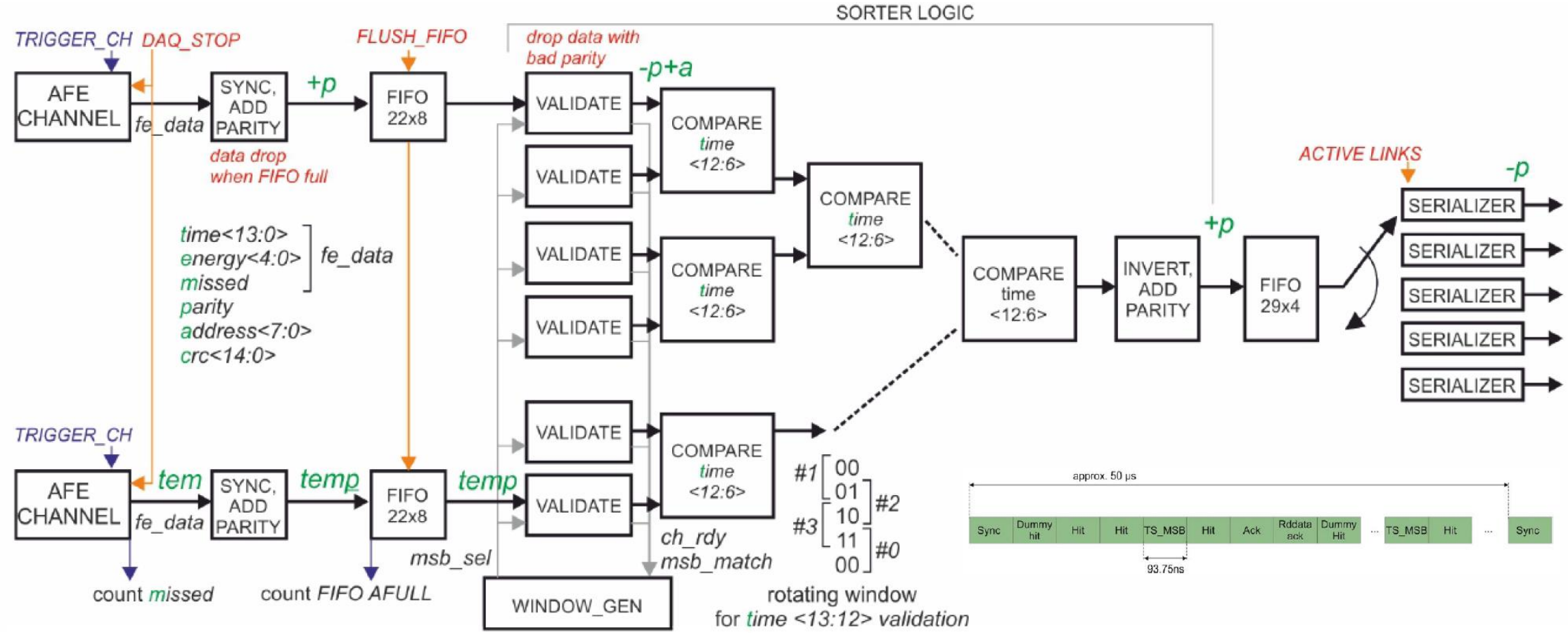




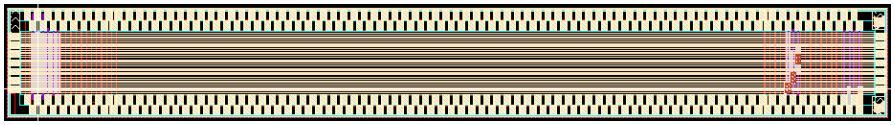
"Stop" strategy: stop accepting new hits, drain the ASIC channel FIFOs, then restart accepting hits.
"Clear" strategy : clear the ASIC channel FIFOs, then re-enable data taking as soon as possible.

Courtesy: Xin Gao, FAIR

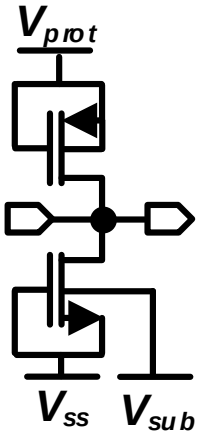
Back-end, data path



ESD protection - temperature

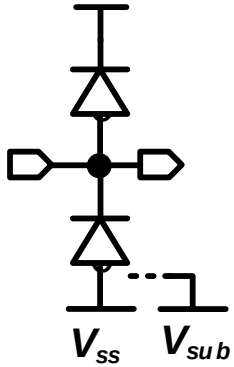


64*



ESD-CHIP

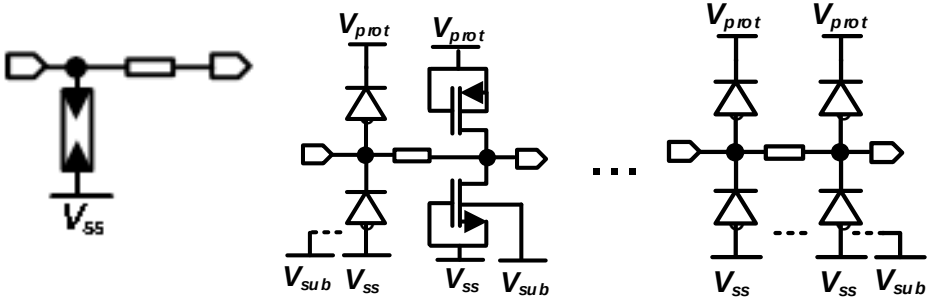
64*

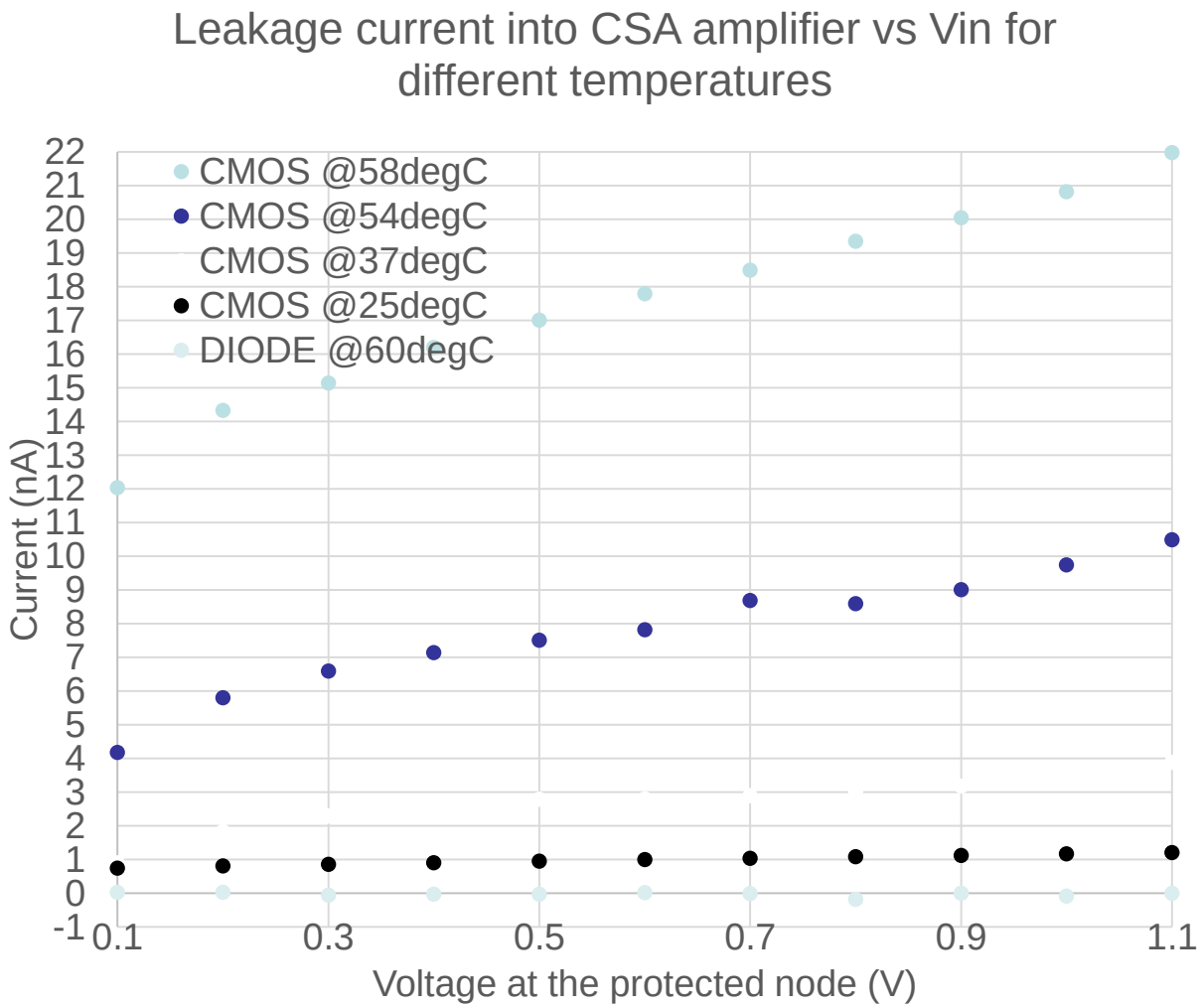


(PMOS: W=264µm L=280 nm,
NMOS: W=216 µm L=280 nm)

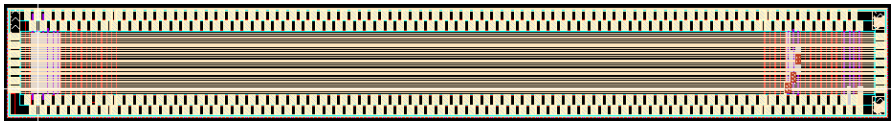
(DIOP: 200 µm x 9 µm
DION: 200 µm x 15 µm)

28 test structures

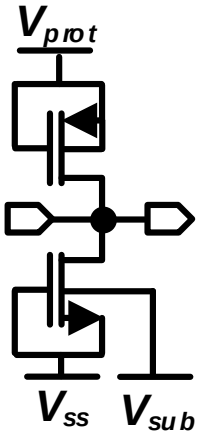




ESD protection - radiation

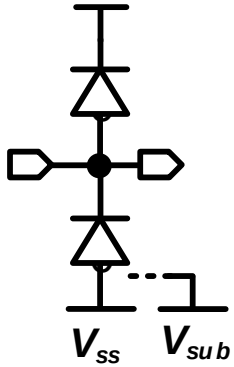


64*



ESD-CHIP

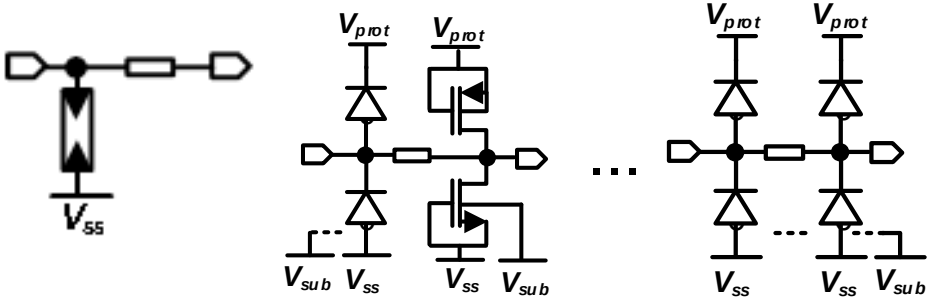
64*



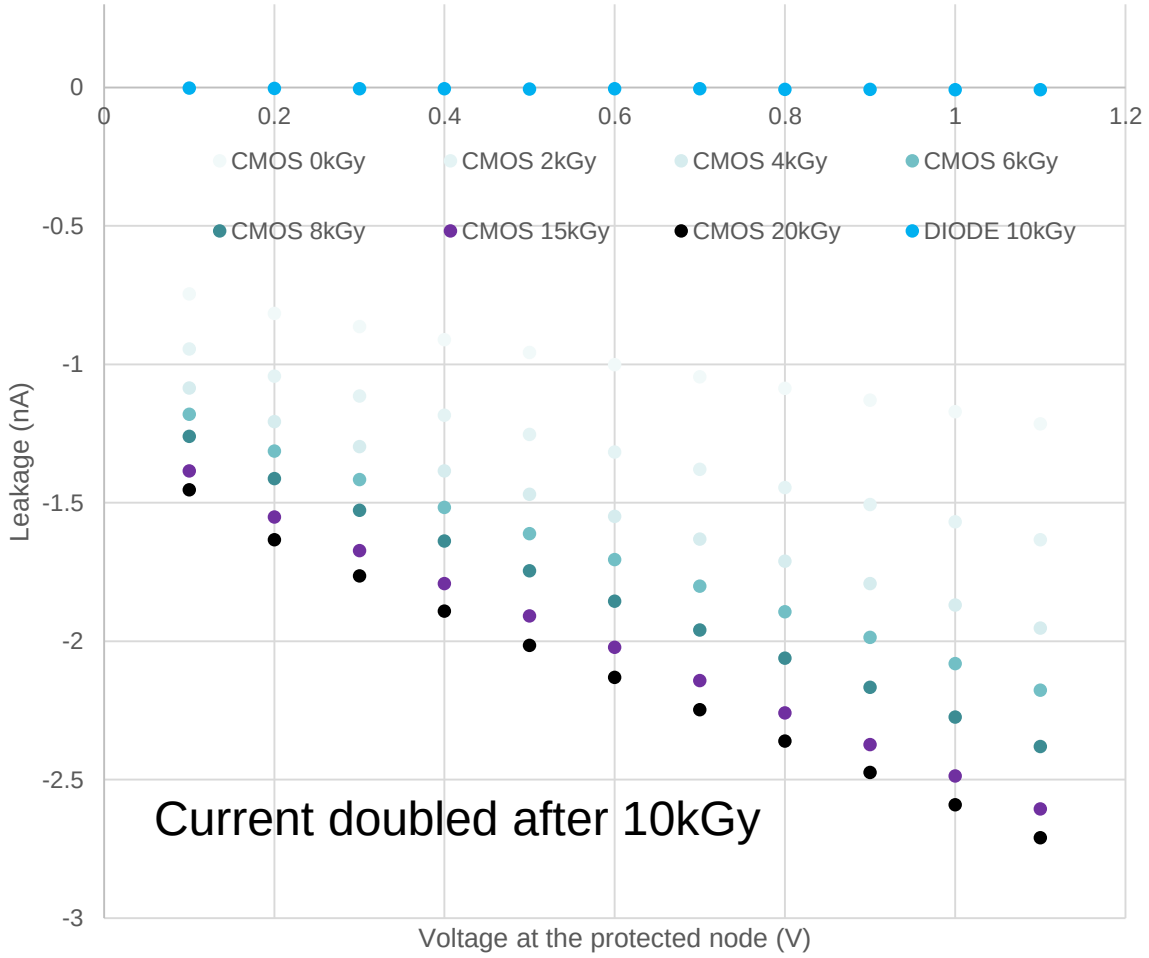
(PMOS: W=264µm L=280 nm,
NMOS: W=216 µm L=280 nm)

(DIOP: 200 µm x 9 µm
DION: 200 µm x 15 µm)

28 test structures



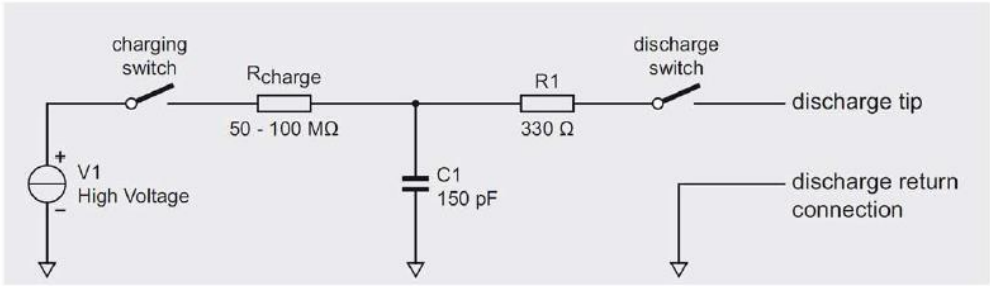
Leakage current into CSA amplifier vs Vin for different irradiation doses @24degC



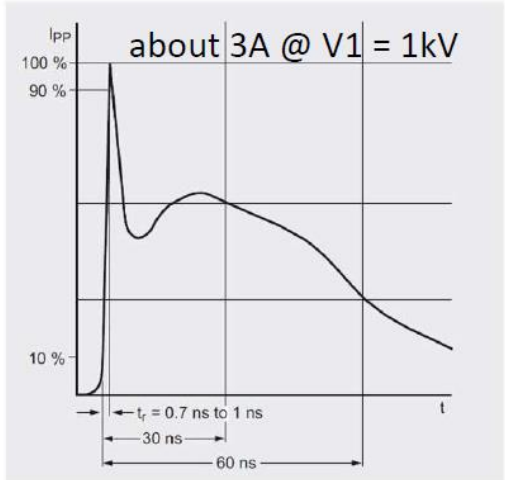
Testing of XYTER2.1 ESD protection level with "ESD gun" from emtest :

Used ESD generator:

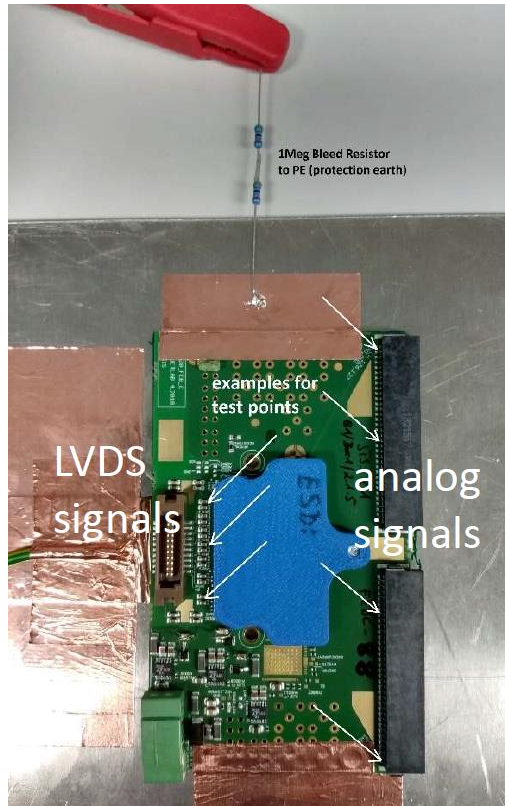
Internal circuit:



Typical waveform of ESD generator output current:



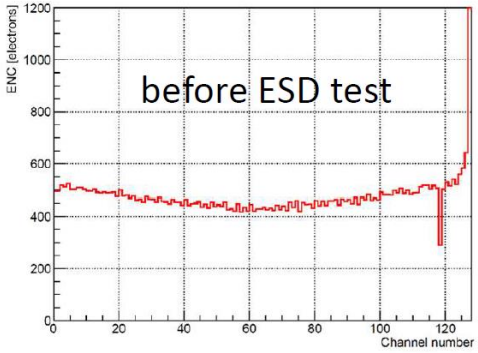
- An ESD pulse of up to 1kV on an analog signal line will damage the appropriate channel, but not other channels or the whole ASIC.
- With 1.2kV on analog signal lines there were CSA register read/write errors, so the whole ASIC was affected.



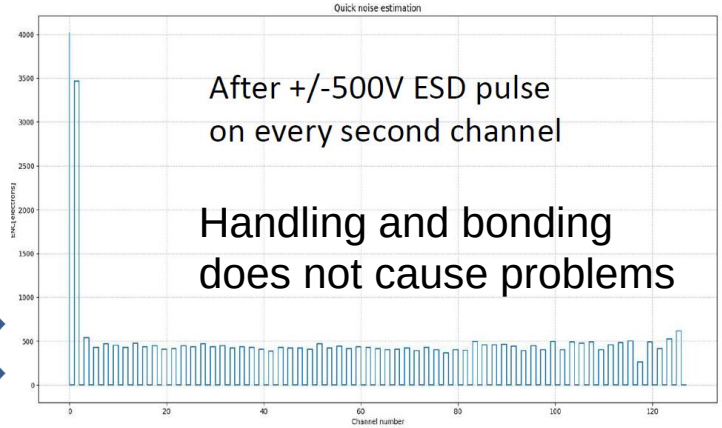
LVDS:

+/- 1500V @ LVDS signals: Sync and Communication OK
+/- 1700V @ LVDS signals: Sync and Communication OK
+/- 2000V @ LVDS signals: Sync error, no SOS received

Analog channels failure

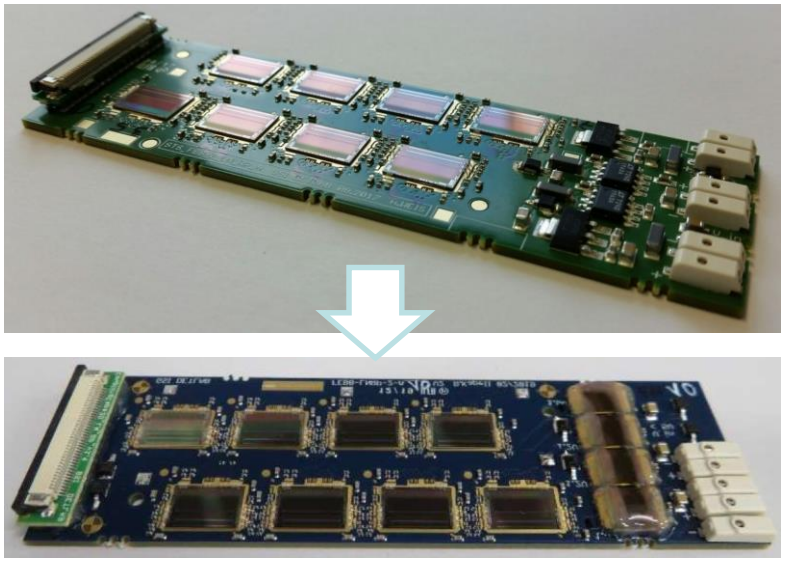


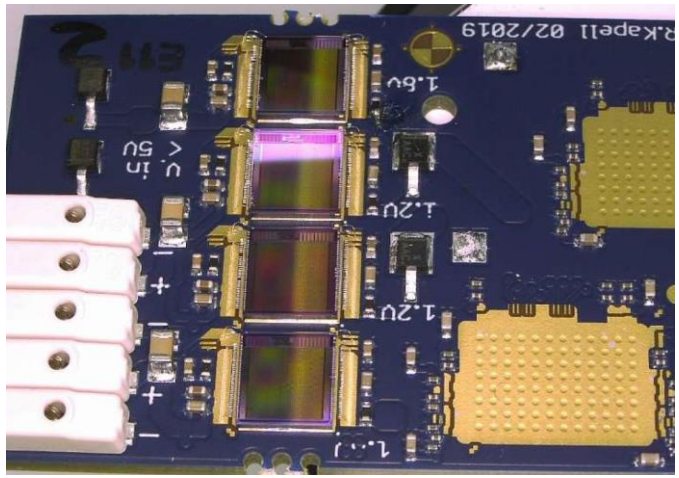
good channels
damaged channels

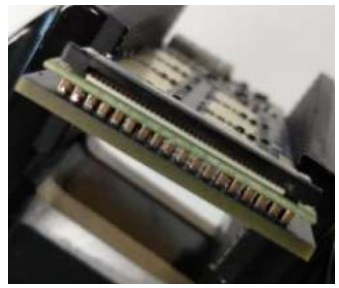


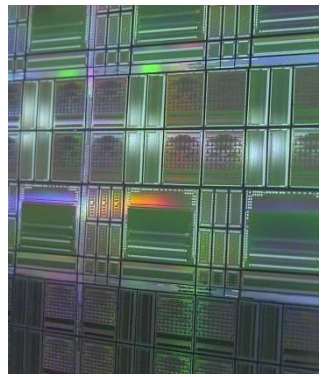
Courtesy: Ralf Kapell

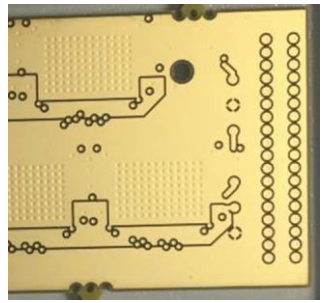
FEB-8 architecture

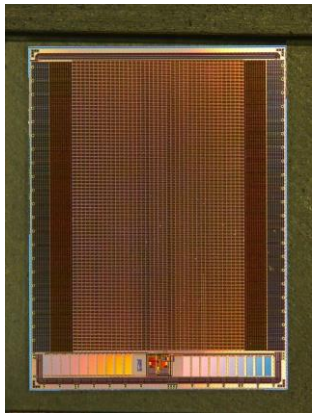












LDOs development at SCL Chandigarh

Output noise (100kHz to 100MHz) < **70µV RMS**

Final size: 5.7mm x 6.2mm

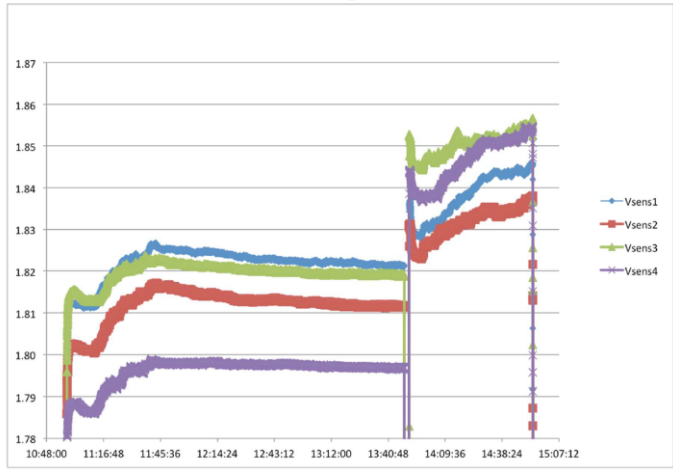
Two versions: 1.8V/1.6A and 1.2V/1.6A

4 external parts (2 Rs, 2 Caps)

Proton irradiation campaign successful

after 10kGy change Vout < 15 mV even at 20kGy.

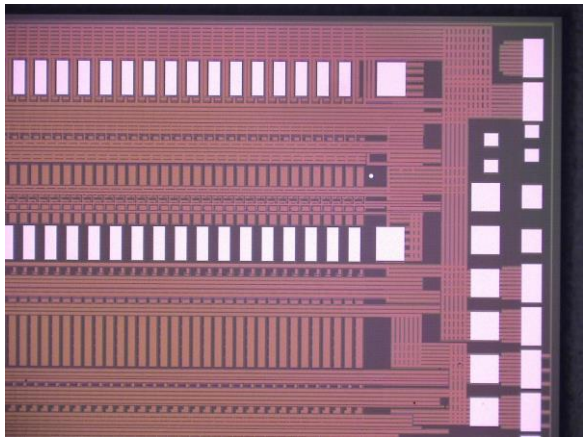
LDO Vout during irradiation

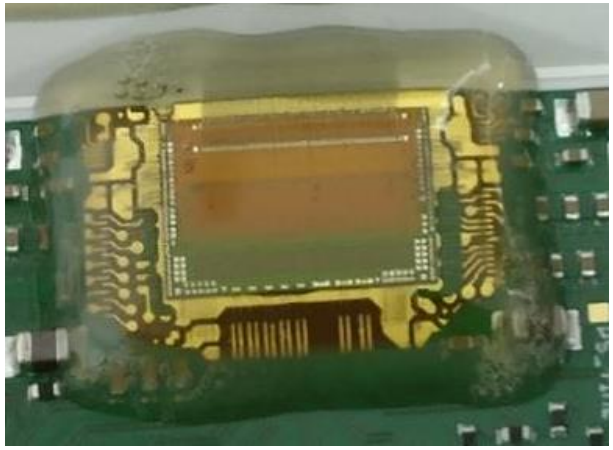


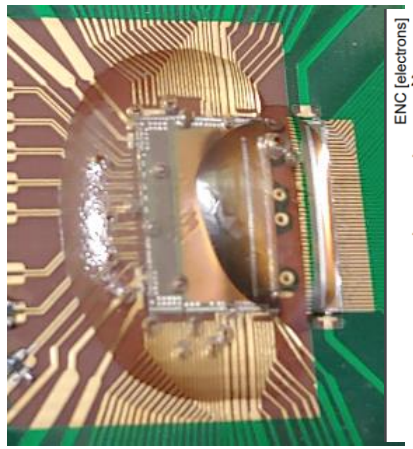
Manufacturing / Yield

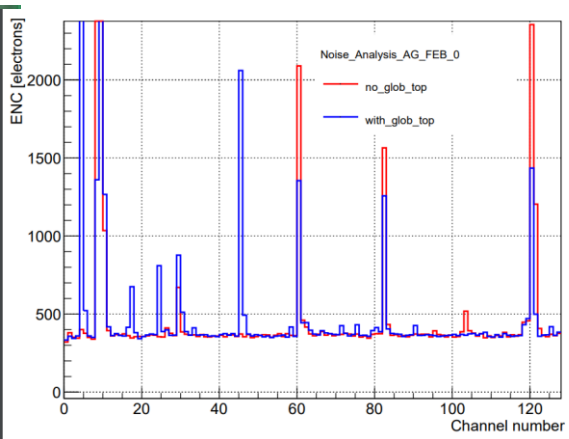
- Encapsulant issue:
  - SMX2.1 with existing dam&fill solution cannot withstand +40°C.

  (Polytec UV DC 2257, hardness 73)
  - SMX2.1 with Dymax 9001-E-v3.1 (hardness D43) is still operational at 83°C+.
  - Irradiation tests of new encapsulant are in progress.



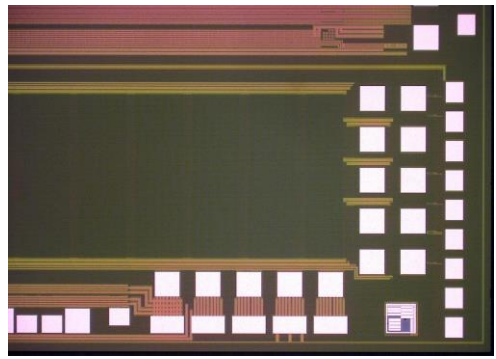


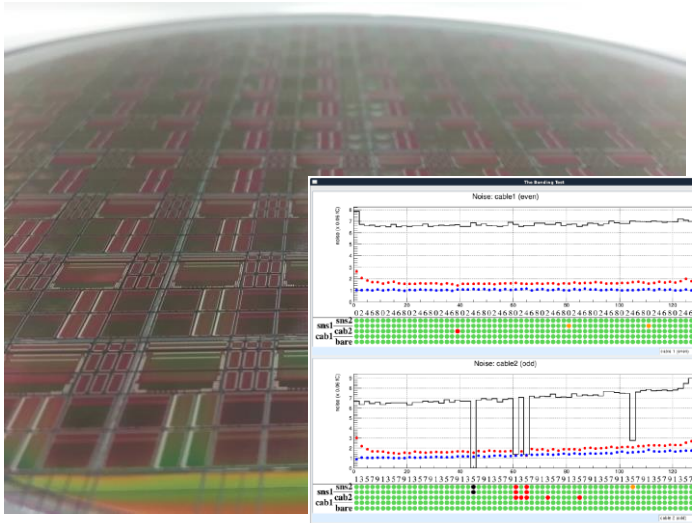


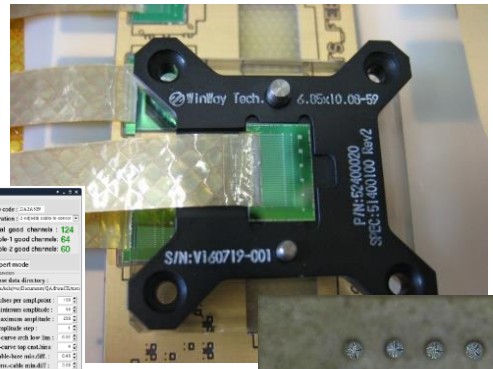


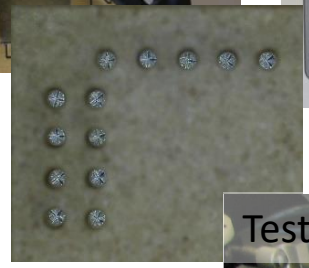
Testability

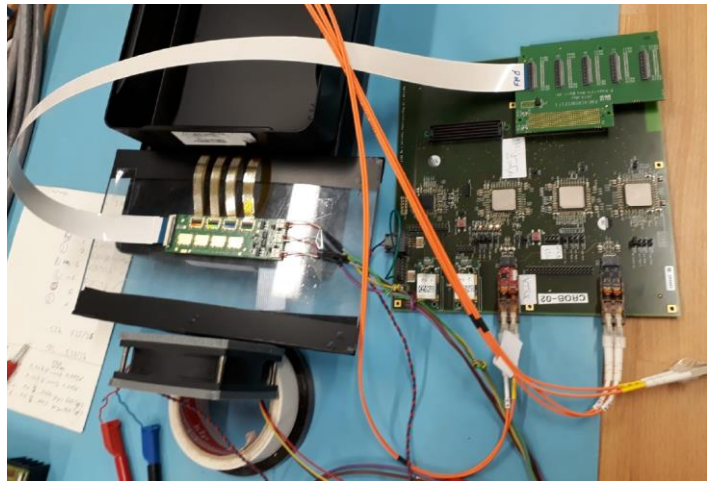
- Pogo-probe pads -> testing without wire-bonding OR wafer prober DURING ASSEMBLY
- Multiple potentials available on pads -> faster wafer-level testing
- Global ADC input -> faster calibration

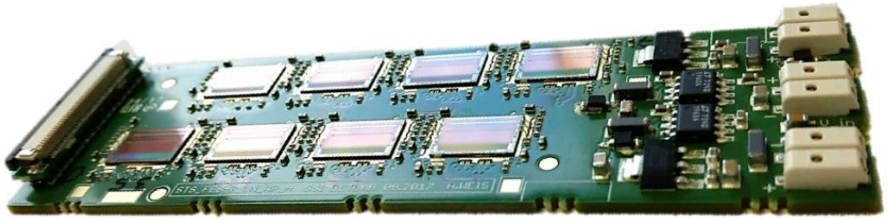




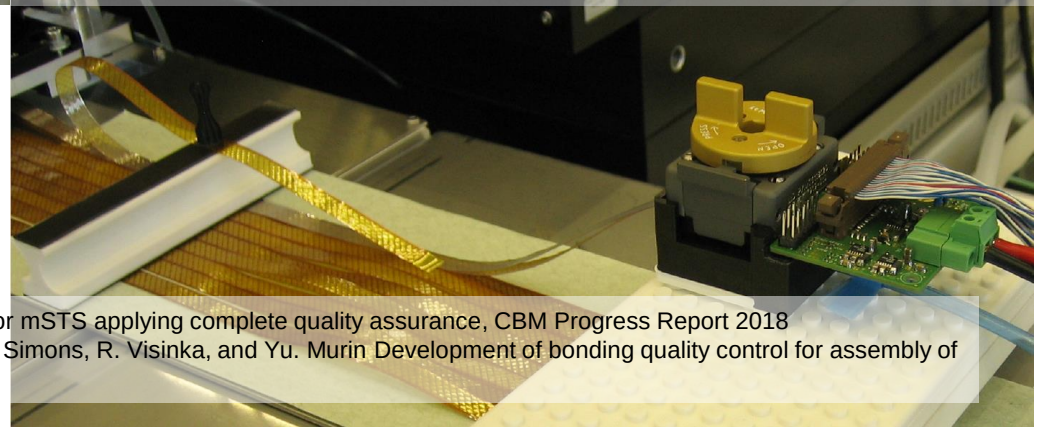






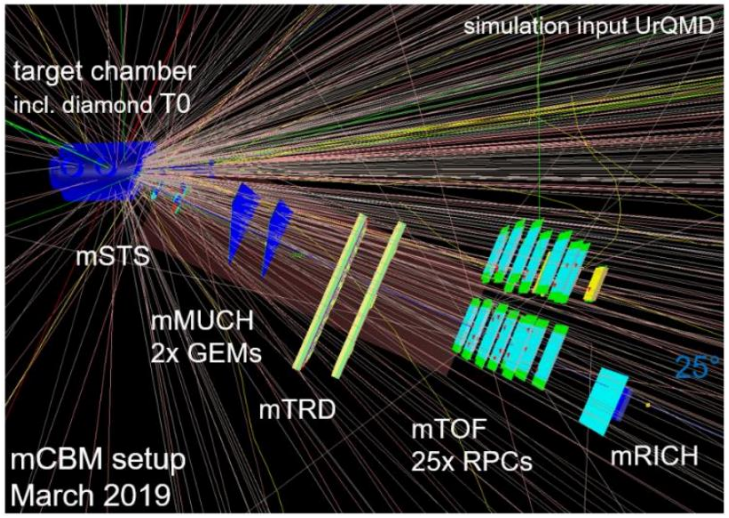


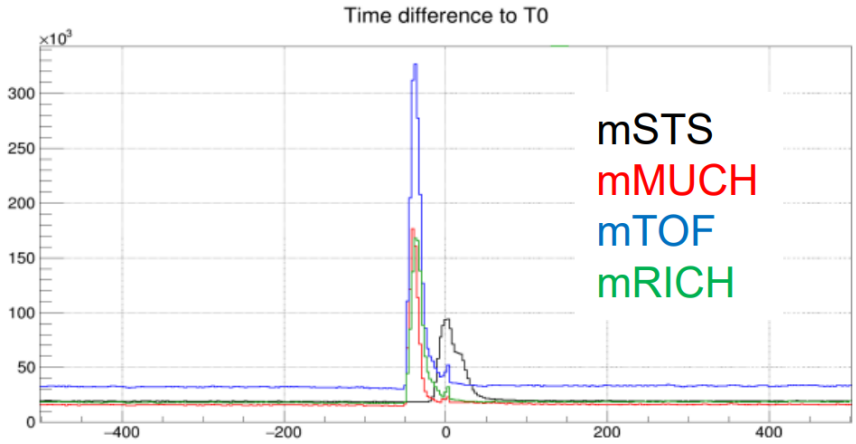
Testing of the FEB8 after the wire bonding of ASIC-rows.



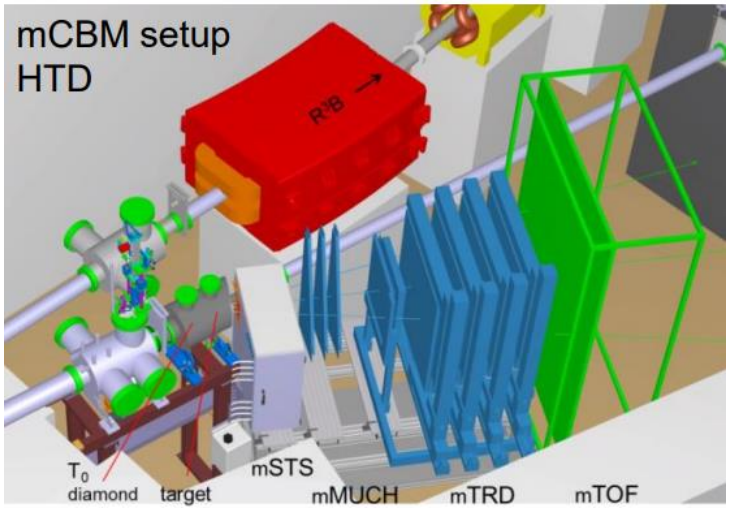
C. Simons, R. Visinka, M. Dogan, A. Rodriguez-Rodriguez, J. Lehnert, and R. Kapell, Assembly of modules for mSTS applying complete quality assurance, CBM Progress Report 2018
N. Sukhov, D. Dementev, M. Dogan, A. Kolozhvari, A. Rodriguez Rodriguez, C. J. Schmidt, M. Shitenkow, C. Simons, R. Visinka, and Yu. Murin Development of bonding quality control for assembly of the silicon microstrip sensor modules

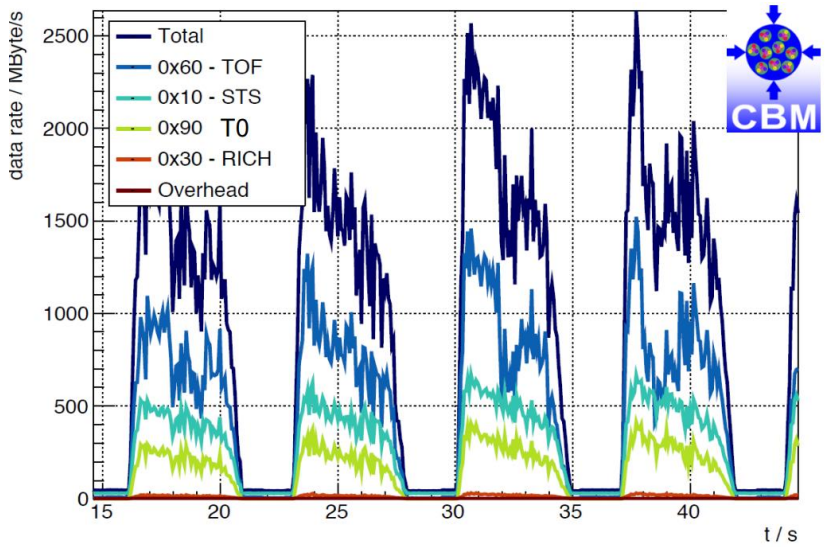
March 2019 mini CBM

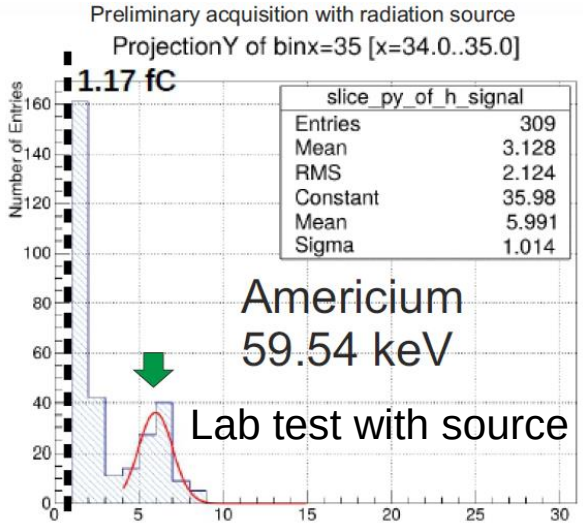


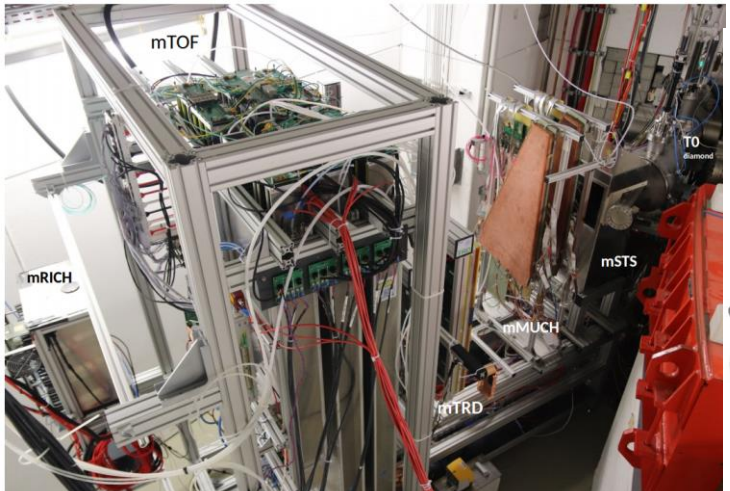


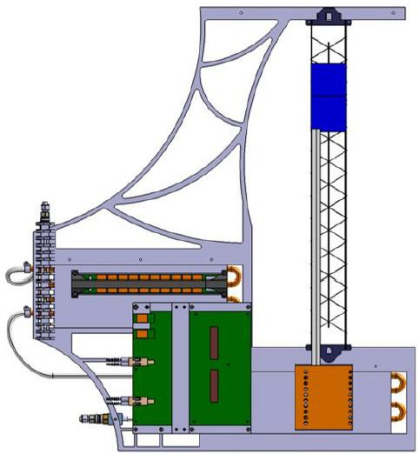
$t_{subsystem}$ – T0 [ns]

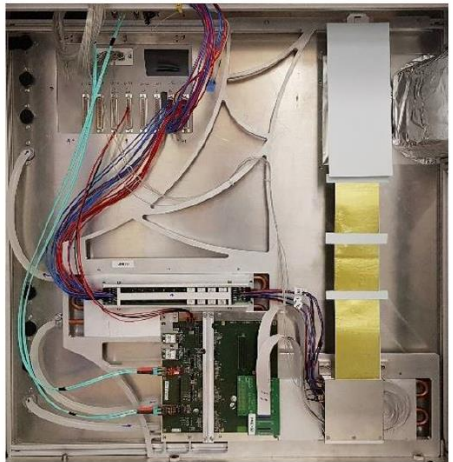












Courtesy:
Norbert Hermann, Ajit Kumar, J.M. Heuser

Summary

- STS-XYTER2.1 was fabricated and thoroughly tested as a read-out of silicon micro-strip sensors + micro-cables and GEM detectors. 128 channels, self-triggering, time (3.125 ns), amplitude (5-bit) digitizing in each channel.

- STS-XYTER2.2 Engineering Design Review will be held on 15.11.2019
- Submission targeted at end of December 2019 (production release in June 2020)

Some of the changes:

- Diagnostic: more potentials added for on-chip monitoring (all VDDs)
- Layout: reduce risk of short during bonding of digital power
- Analog: implement diode-based ESD protection of the inputs
- Analog: fast reset modification: improved timing – full reset only for typical charge -> reduction of intrinsic dead time
- Digital: fix read-back of 5 registers

Thank you for your attention

Very recent results: **34th CBM Collaboration Meeting, Kolkata 2019, CBM Progress Report 2018**

JOURNAL PAPERS:

K. Kasinski, R. Szczygiel, W. Zabolotny, Back-end and interface implementation of the STS-XYTER2 prototype ASIC for the CBM experiment, Journal of Instrumentation, 2016 vol. 11 art. no. C11018.

K. Kasinski, R. Szczygiel, W. Zabolotny, J. Lehnert, C.J. Schmidt and W.F.J. Müller, A protocol for hit and control synchronous transfer for the front-end electronics at the CBM experiment, Nucl. Instrum. Meth. A 835 (2016) 66.

K. Kasinski, P. Koczon, S. Ayet, S. Löchner, C.J. Schmidt, System level considerations for the front end readout ASIC in the CBM experiment from the power supply perspective, J. Instrum. 12 (2017) C03023. http://stacks.iop.org/1748 0221/12/i=03/a=C03023

W. Zubrzycka, K. Kasinski, Leakage current induced effects in the silicon microstrip and gas electron multiplier readout chain a nd their compensation method, Journal of Instrumentation, 2018 vol. 13 art. no. T04003, s.s.[2], 1 10.

K. Kasinski, A. Rodriguez Rodriguez, J. Lehnert, W. Zubrzycka, R. Szczygiel, P. Otfinowski, R. Kleczek, C. J. Schmidt Characteri zation of the STS/MUCH XYTER2, a 128 channel time and amplitude measurement IC for gas and silicon microstrip sensors, Nuclear Instruments & Methods in Physics R esearch. Section A,Accelerators, spectrometers, detectors and associated equipment ; 2018 vol. 908, s. 225 235.

P. Otfinowski, P. Grybos, R. Szczygiel, K. Kasinski, Offset correction system for 128 channel self triggering readout chip with in channel 5 bit energy measurement functionality, Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip. 780 (2015) 114 118. doi:http://dx.doi.org/10.1016/j.nima.2015.01.048.

DAQ system:

Wojciech M. Zabołotny, Grzegorz H. Kasprowicz, Adrian P. Byszuk, David Emschermann, Marek Gumiński, Krzysztof T. Poźniak, and Ryszard Romaniuk "Selection of hardware platform for CBM Common Readout Interface", Proc. SPIE 10445, 1044549 (7 August 2017);

W.M. Zabolotny, G. Kasprowicz, A.P. Byszuk, D. Emschermann, M.Gumiński, B. Juszczyk, J. Lehnert, W.F.J. Müller, K. Poźniak and R. Romaniuk "Versatile prototyping platform for Data Processing Boards for CBM experiment", 2016 JINST 11 C02031

W.M. Zabołotny, A.P. Byszuk, D. Emschermann, M. Gumiński, B. Juszczyk, K. Kasiński, G. Kasprowicz, J. Lehnert, W.F.J. Müller, K. Poźniak, R. Romaniuk, R. Szczygieł, Design of versatile ASIC and protocol tester for CBM readout system, J. Instrum. 12 (2017) C02060. http://stacks.iop.org/1748 0221/12/i=02/a=C02060