Status of TRB/ASIC readout for phase 0 STS1 and front-end free sADC readout for straws

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TOPICS

1. STS1 – PASTTREC ASIC + TRB3 readout

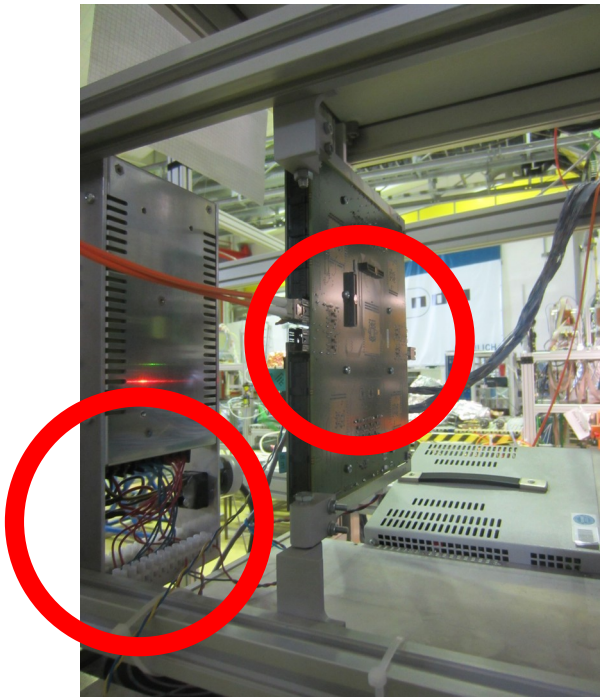
   – TRB3 crate
   – TRB3 boards status
   – software and ASIC communication test

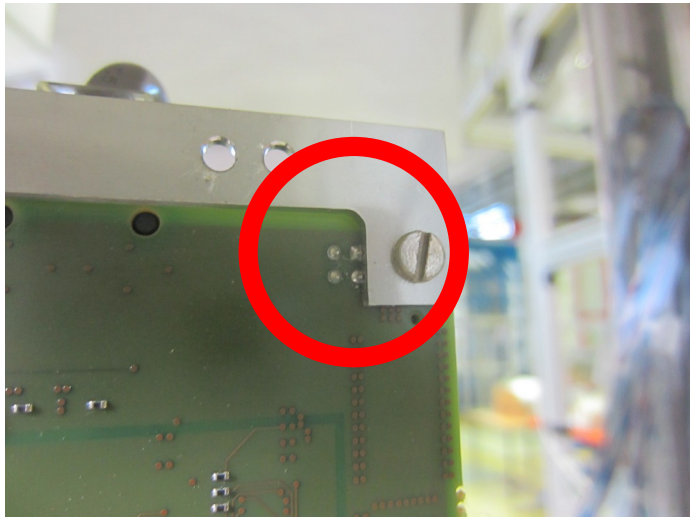
2. ASIC board test – long signal cable

3. Progress of front-end free sADC straw readout

4. Summary and outlook

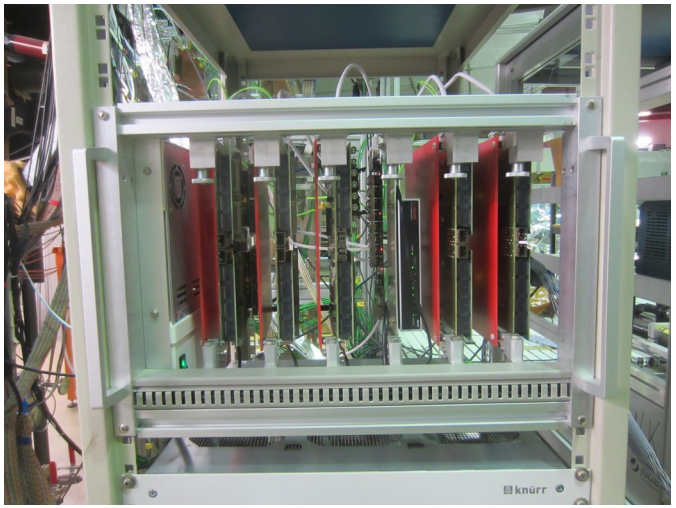
TRB3 crate before modifications

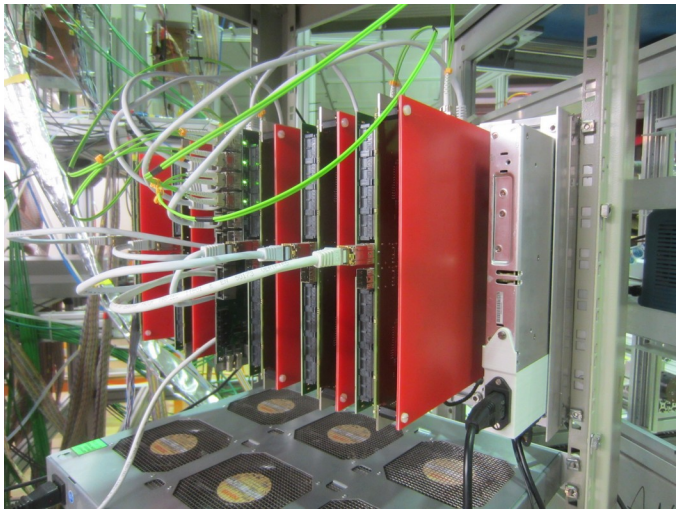


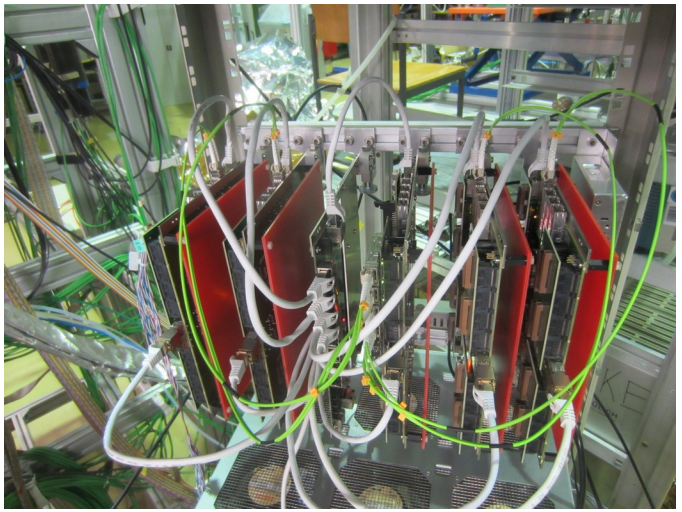


– PS safety has to be improved – 230V protection
– mechanical changes needed
– TRB3 backside protection has to be added

TRB3 crate after modifications







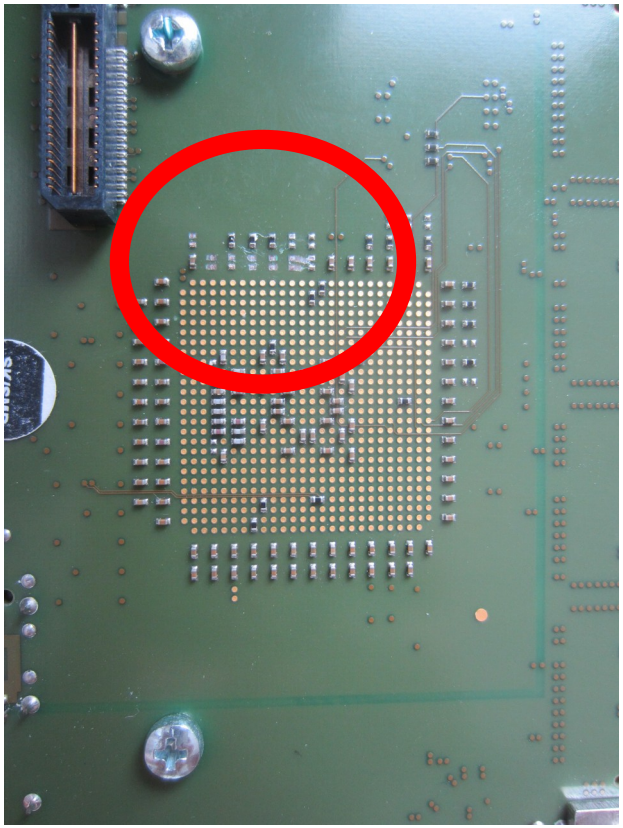
TRB3 crate after modifications

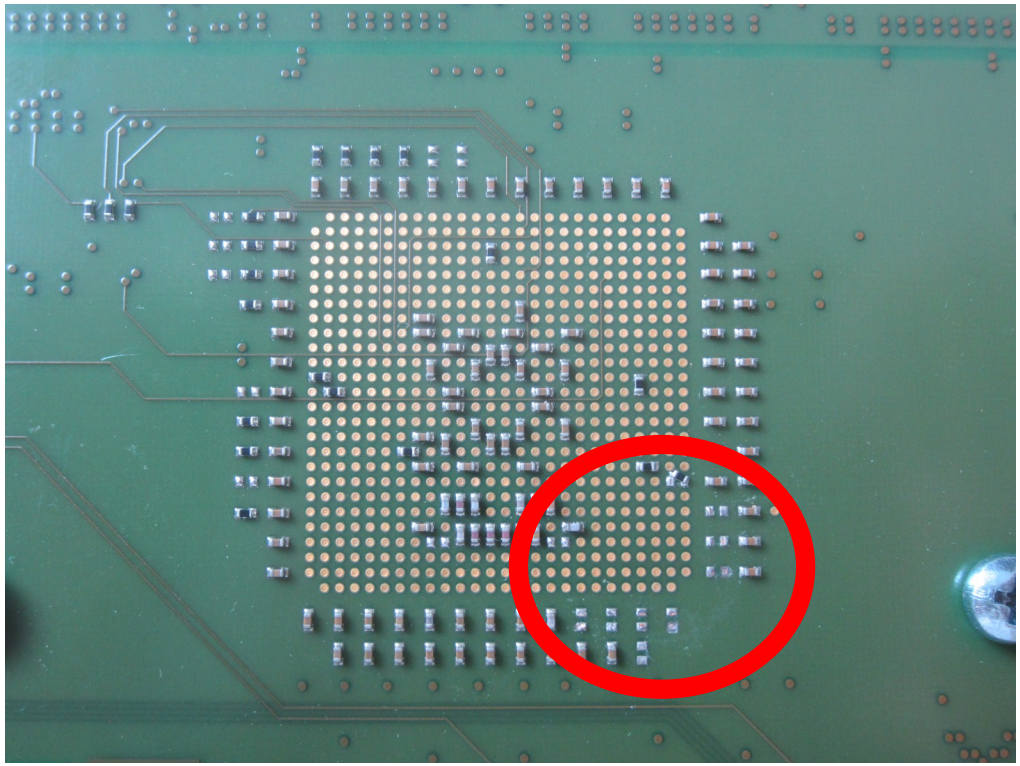
– safety modification made – 3d printout for PS
– mechanical parts modified (shaped)
– raceway for cables added
– protection on backside of TRB3 boards added
– tool less mounting/dismounting of TRB3 boards

– 5 TRB boards + switch and trigger distribution
– inter board connection with short cables

TRB3 boards I

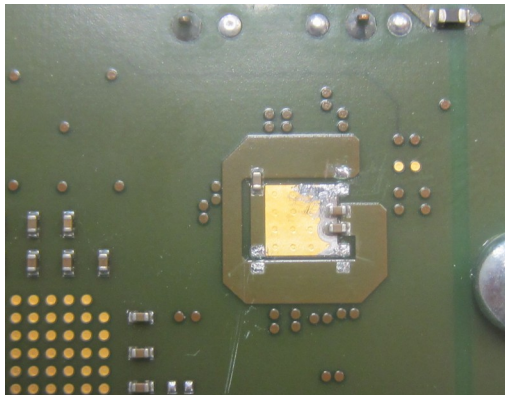
Mechanical damages on boards “discovered”

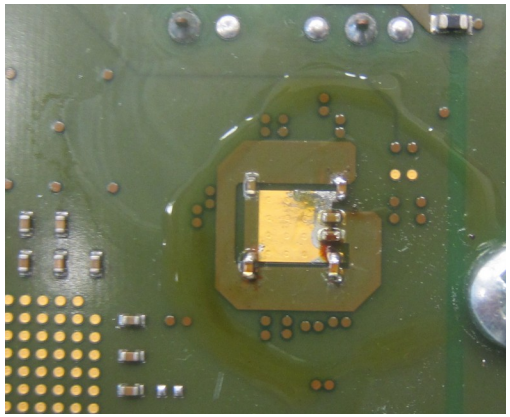




TRB3 boards II

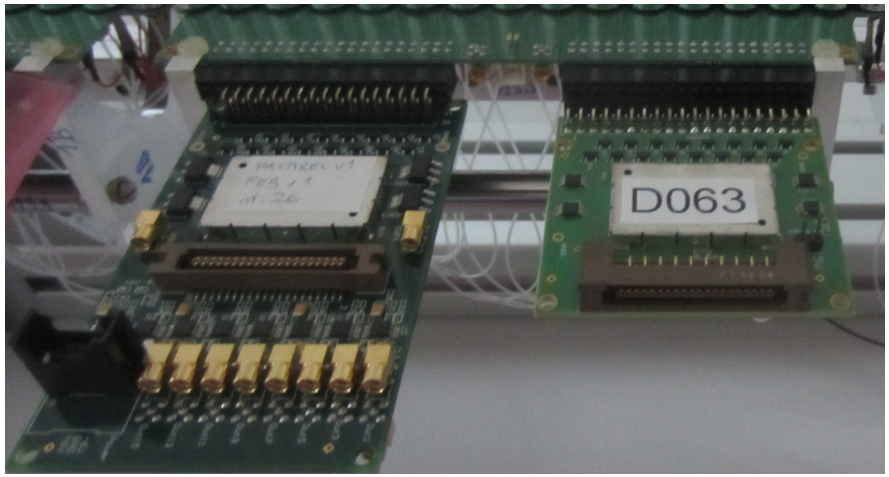
- 4 boards sent for test/repair to GSI
- 3 new boards from Krakow
- “small” repair done in FZJ(ZEA) (on 2 boards)





- 5 TRB3 boards available – communication with all 25 FPGA possible
- started ASIC communication tests
- using “old” TDC/PASTTREC version

ASIC board tests I



Goal:

- test FPGA (connection, TDC)
- test LVDS cables
- test ASIC channels, also connected to straws
- prepare ASIC configuration (baseline, etc..)
- ToT with cosmics/sources ?
- do not disturb STS1 preparations

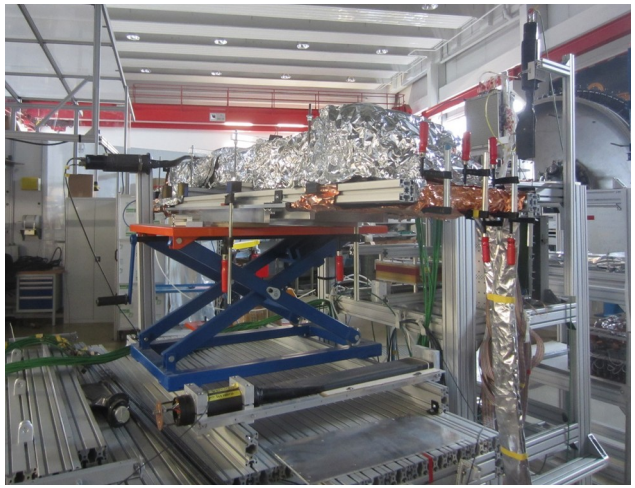
Solution:

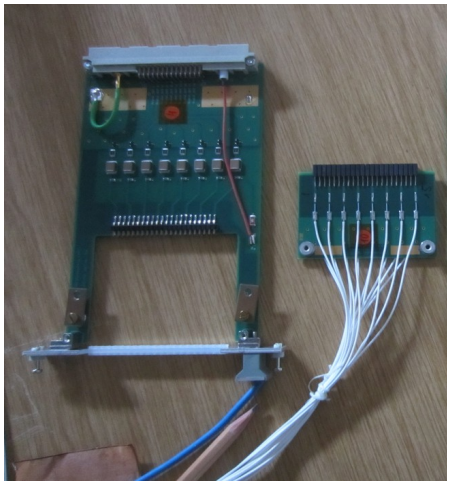
- use straw setup used for sADC straw readout

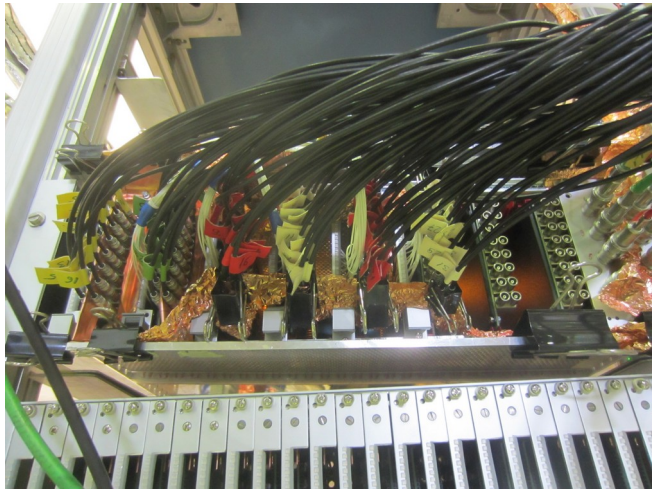
Byproduct:

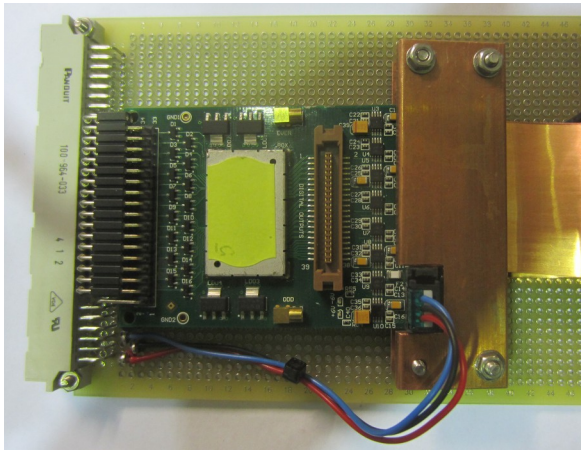
- test ASIC behavior and analog signals after long cable

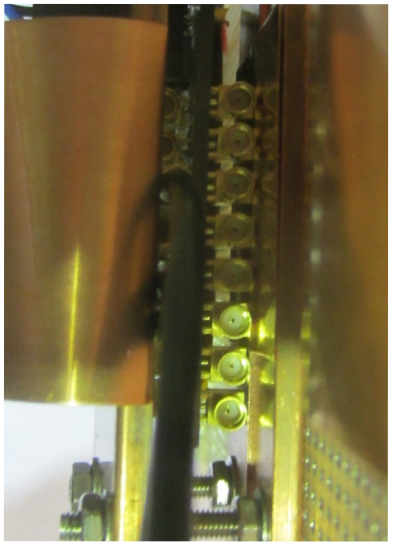
ASIC board tests II



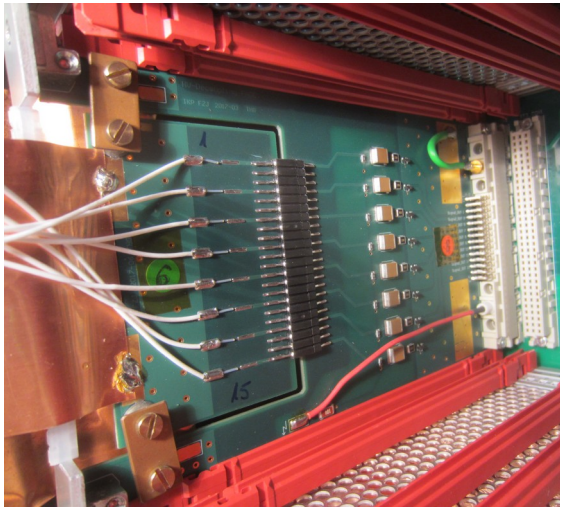


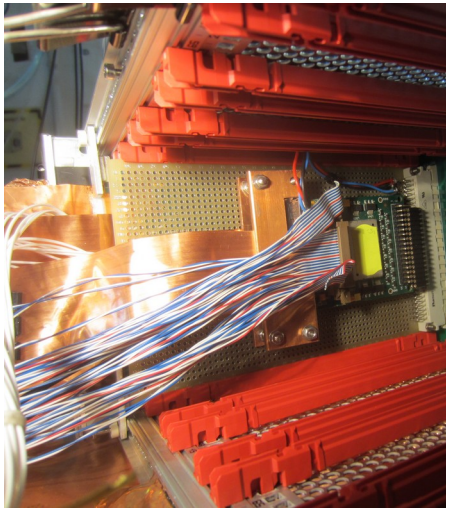


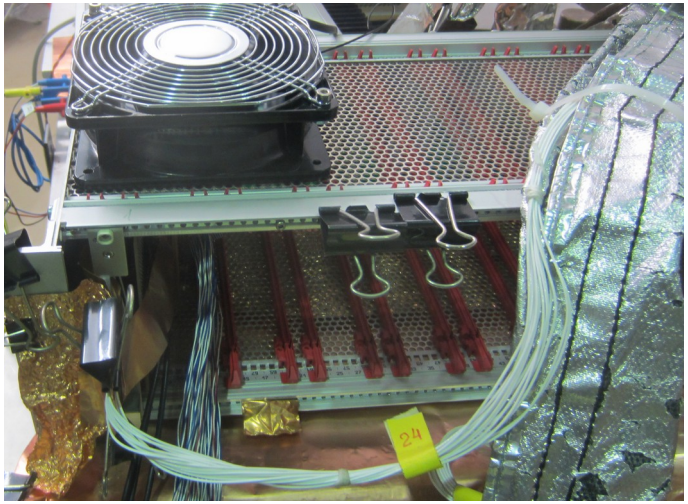


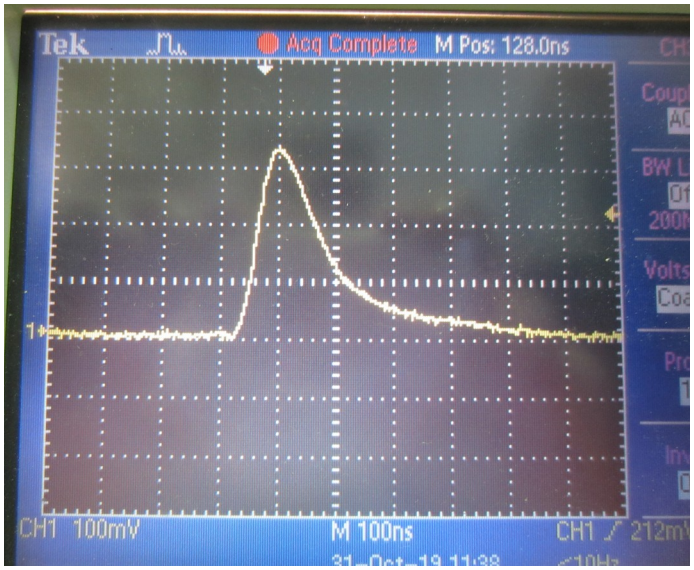


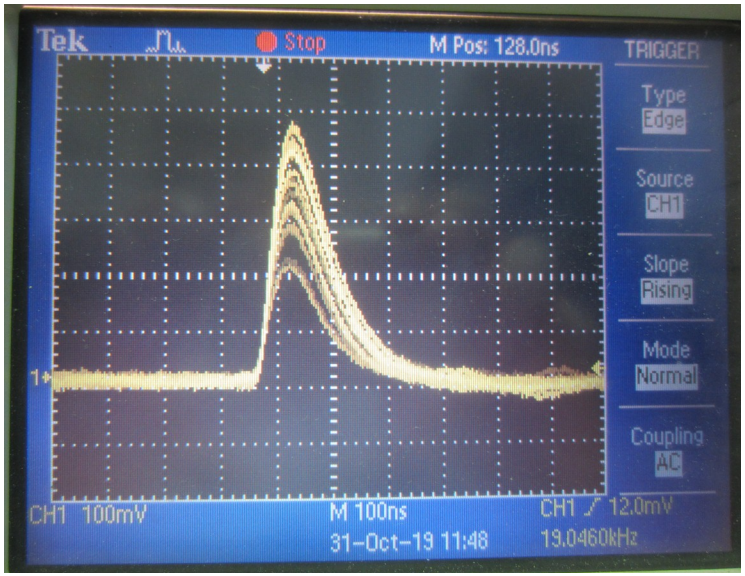
ASIC board tests III











ASIC board tests IV

Done/in progress:

- TRBnet software and ASIC scripts installed
- TRB3 boards configurations mostly done
- first ASIC communication test done
- tests of ASIC configuration scripts in progress

Byproduct:

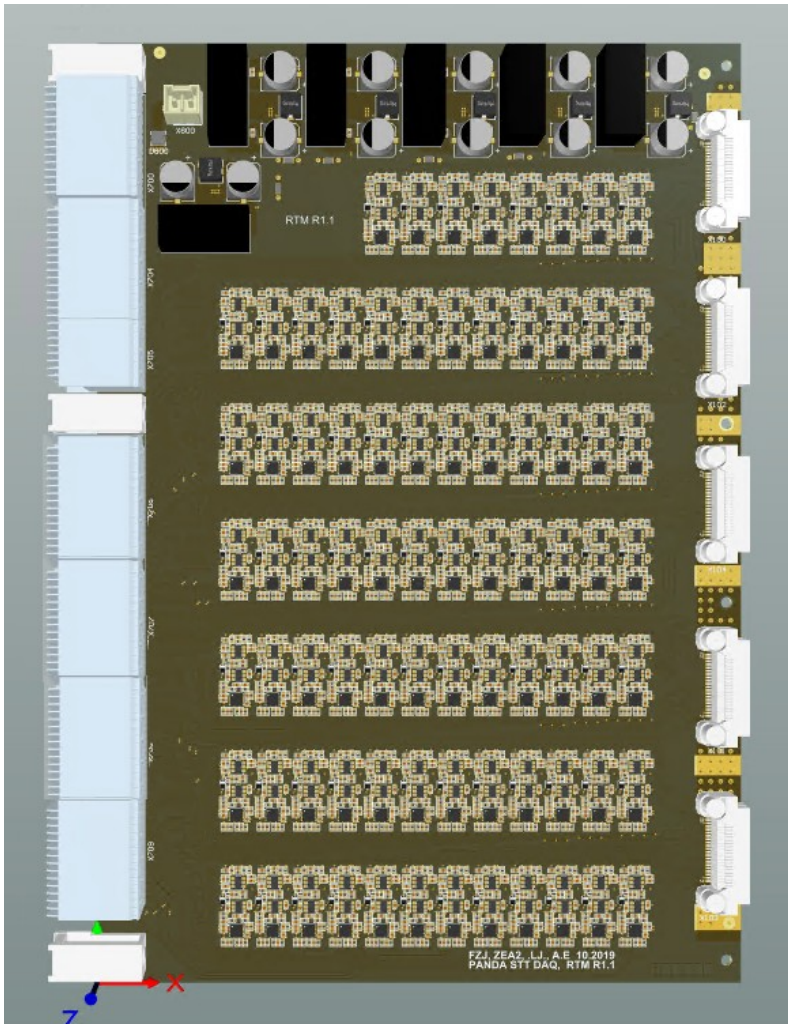
- ASIC analog output signals after long cable look very promising

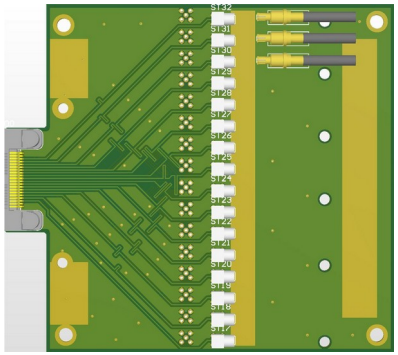
sADC front-end free straw readout progress I

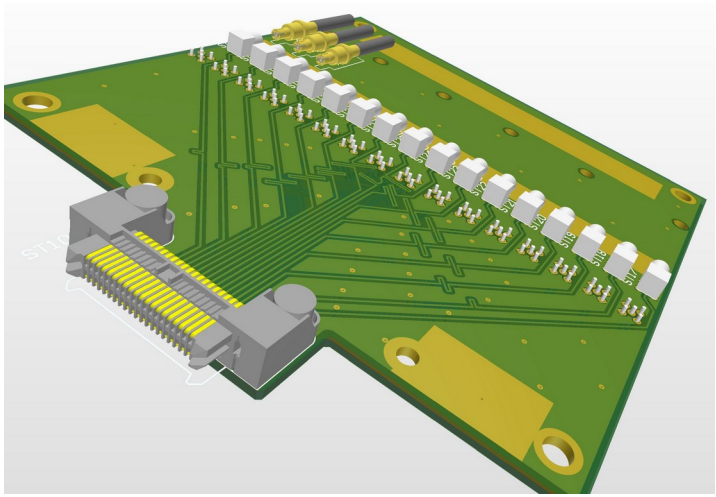
Ongoing activities:

- order of 4 corrected ampl. board in progress
- adapter for direct coupling of analog signals (MMCX) specified and designed – possibility to use sADC system as multichannel oscilloscope
- ampl. rear board equipped only with single end to differential part in preparation
- FPGA firmware for all 160 channel in preparation

sADC straw readout progress II

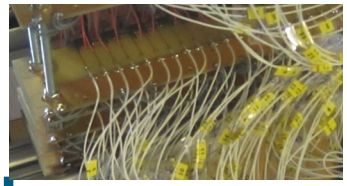






Summary and outlook

- TRB3 create prepared, TRBnet software installed
- 5 working TRB3 boards available for tests
- communication with PASTTREC ASIC possible
- first test of ASIC after long cables – "front-end free" readout with ASIC ?
- small "server" for TRB readout ordered



- corrected ampl. board for sADC system ordered
- adapter for direct coupling of analog signal

- connect TRB3 readout to STS1, ASIC configuration and full system tests, server setup

JÜLICH
FORSCHUNGSZENTRUM

Thank you