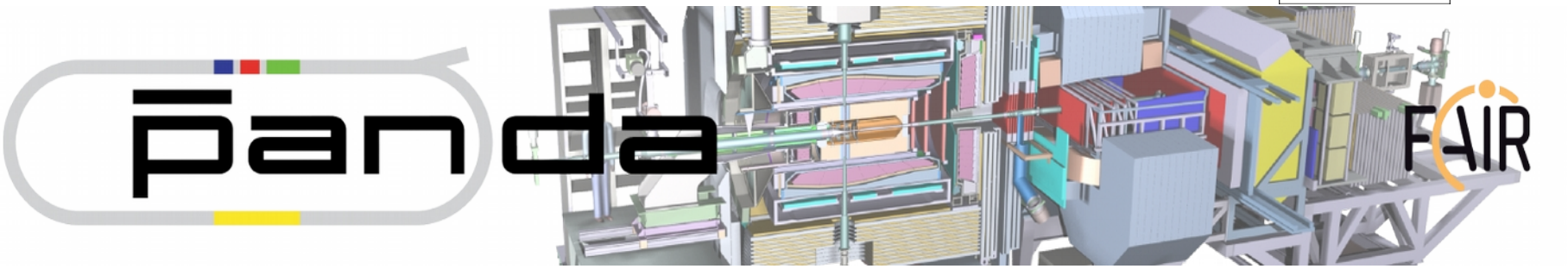
APD Gain Optimization for the APFEL ASIC & Slice Assembly Status for the

JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN



Target Spectrometer

GSI

Federal Ministry of Education and Research

HIC for FAIR
Helmholtz International Center

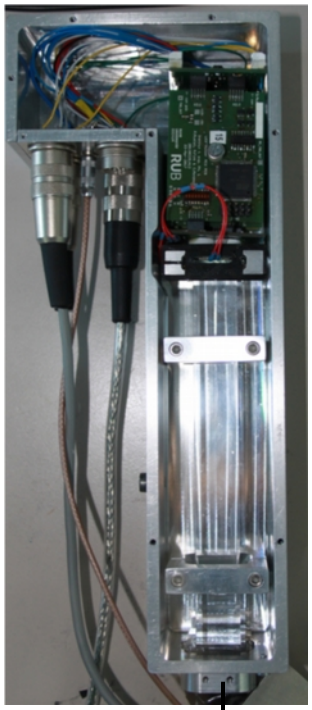
Markus W. H. Moritz

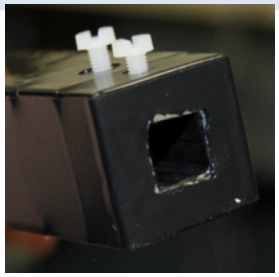
2nd Physics Institute, Giessen University, Germany

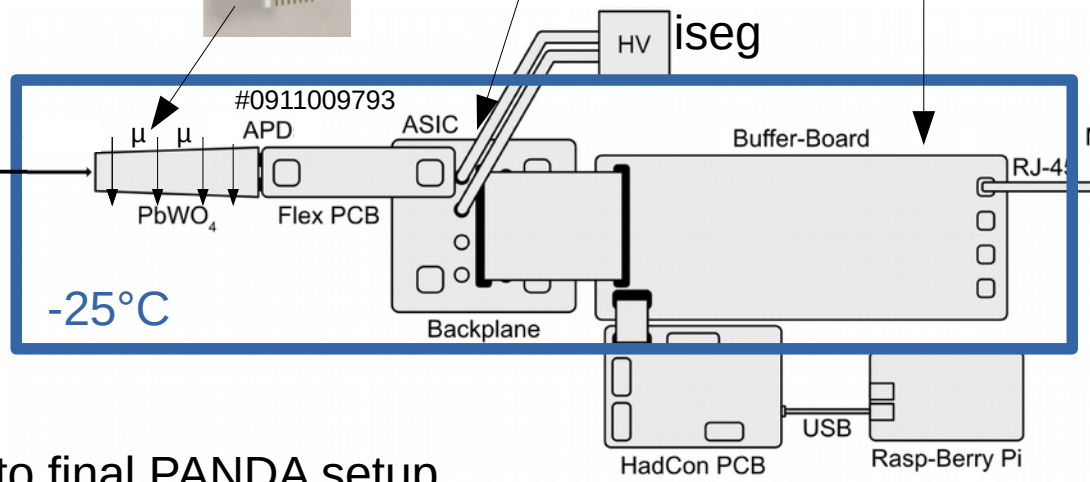
PANDA CM, November 2019

APD Gain Optimization for the APFEL ASIC

Setup







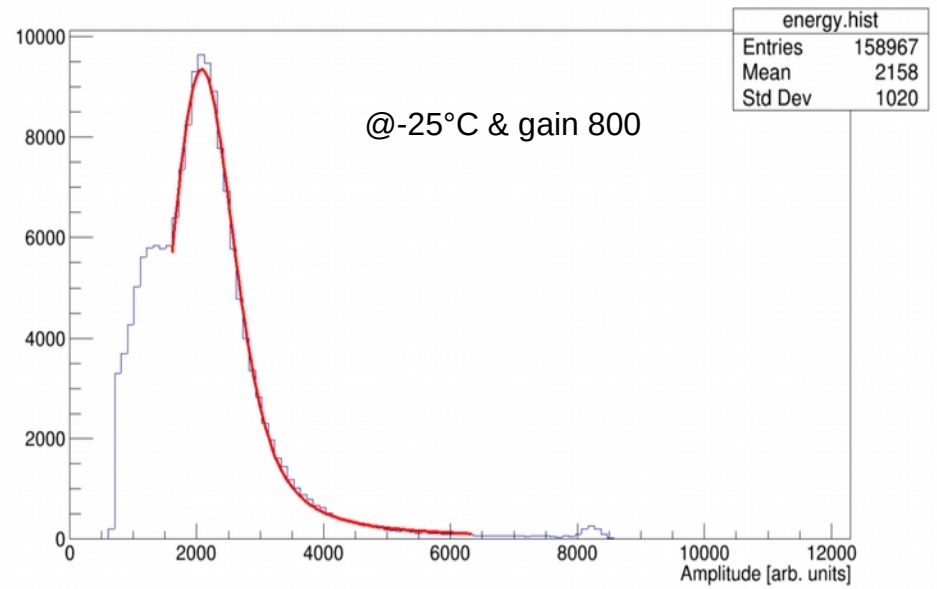
PANDA SADC with opt. feature extraction (Oliver Noll)

very close to final PANDA setup

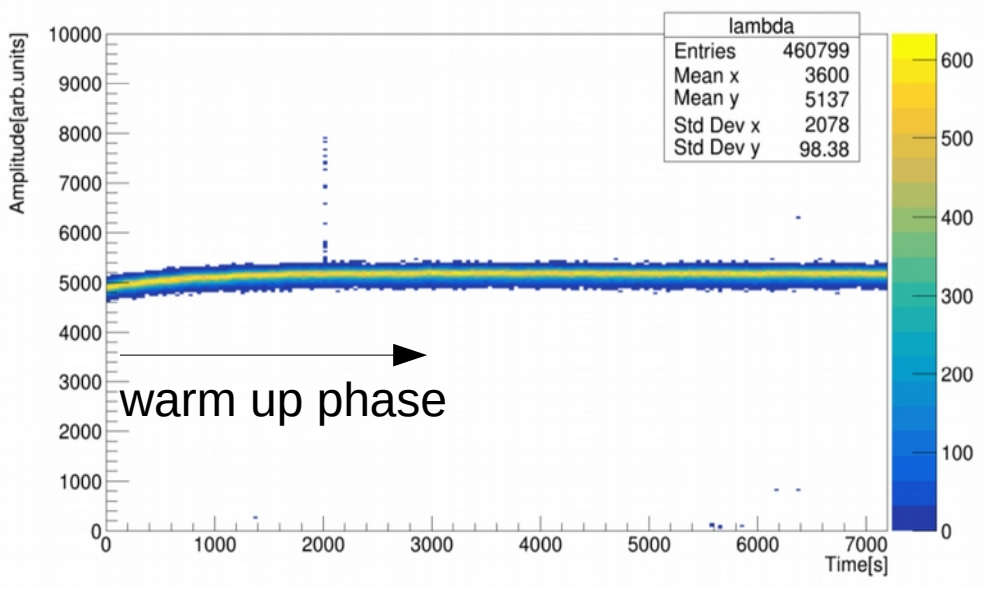
APD Gain Optimization for the APFEL ASIC

Procedure

- calibration with cosmic muons



- light pulser stability test



For broad dyn. Range:

- thick fiber bundle
- internal attenuation not sufficient to reach a few MeV

→ attenuation foils

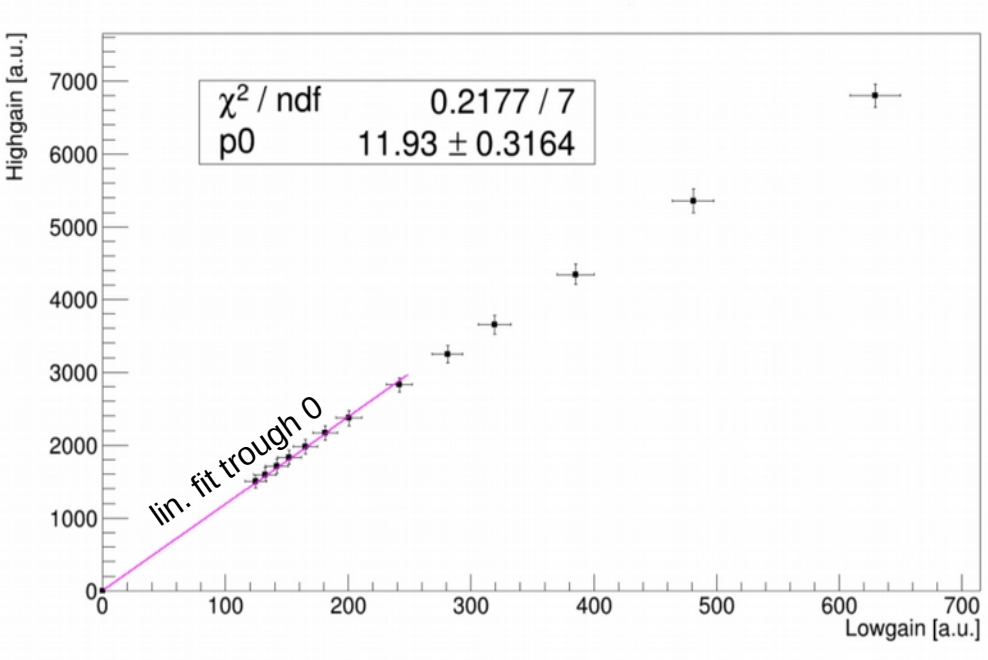
→ collimators

→ 11,3 MeV – 1869,5 MeV

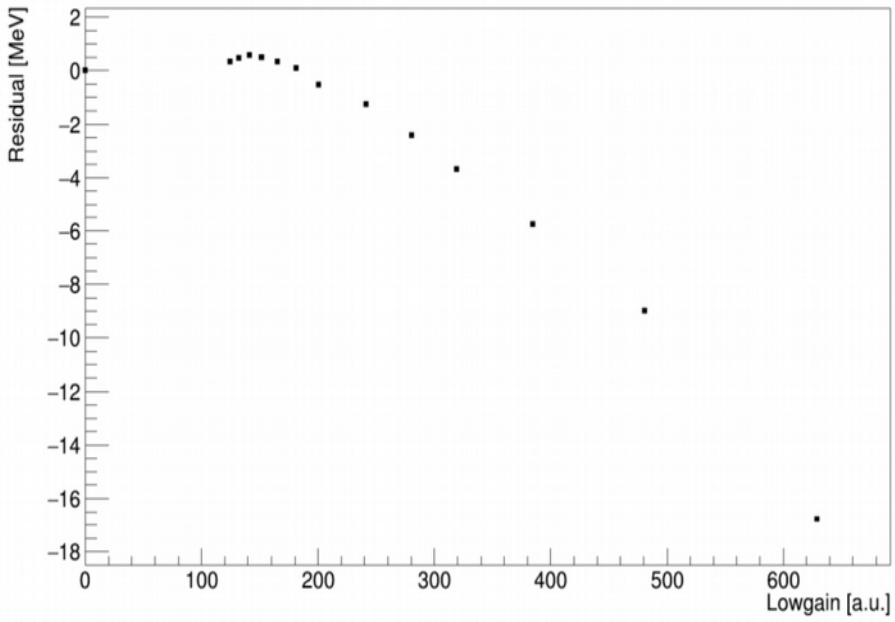
- 2 kHz pulse rate
- 150 s each intensity (energy)

Analysis

- linearity high vs low gain

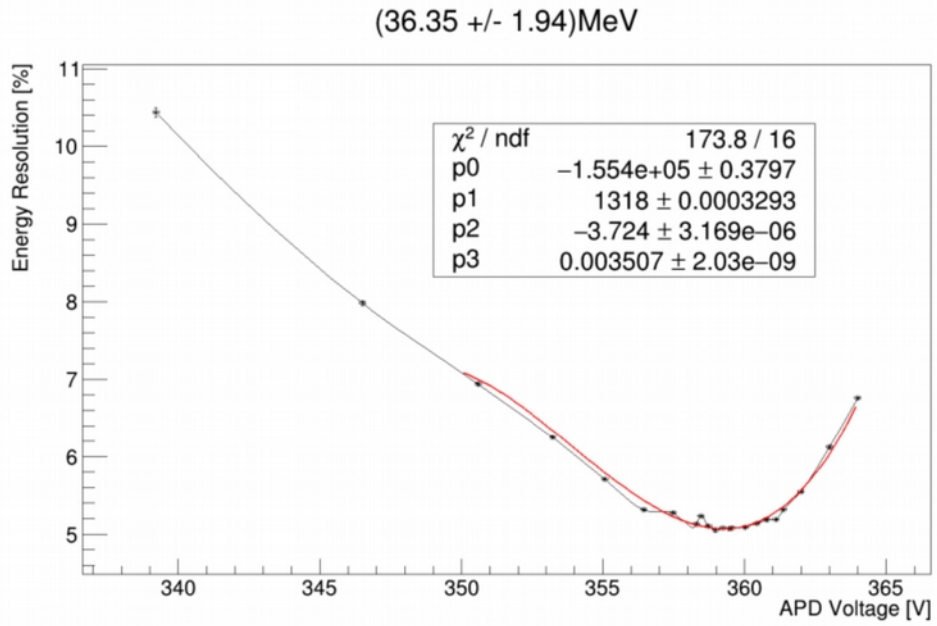


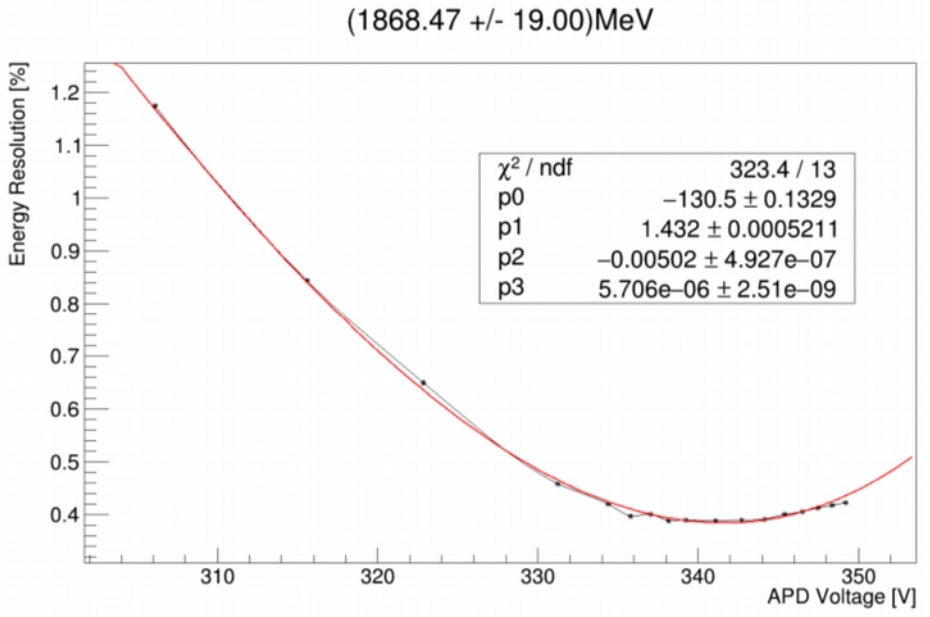
- residual



APD Gain Optimization for the APFEL ASIC

Analysis





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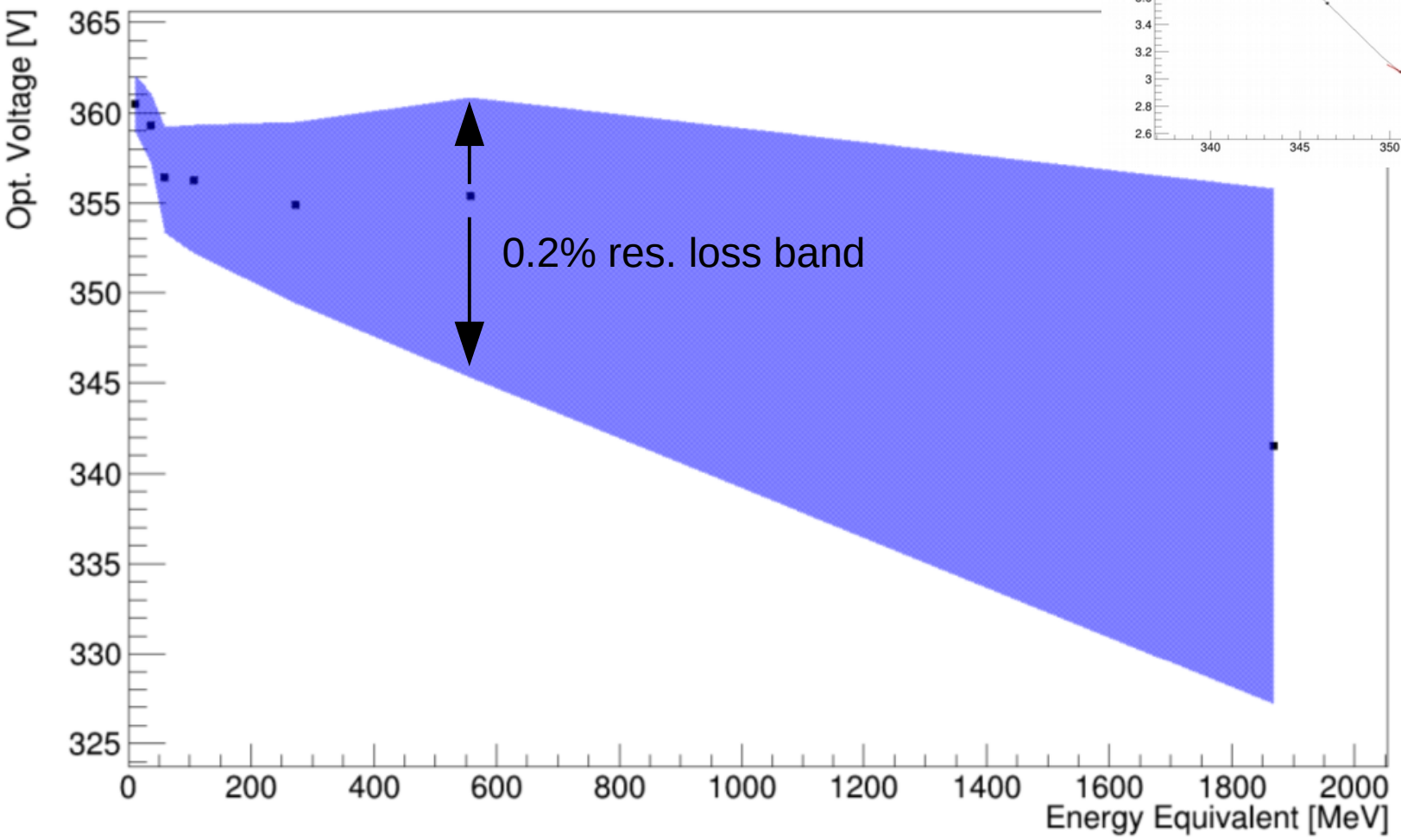
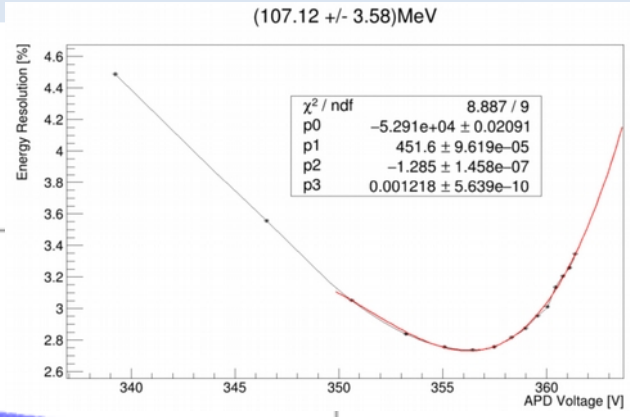
Analysis





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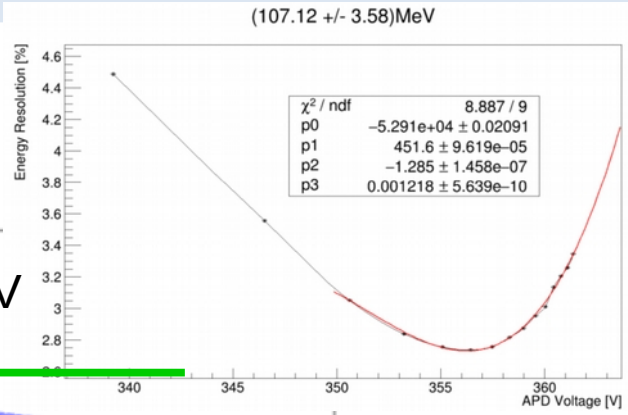

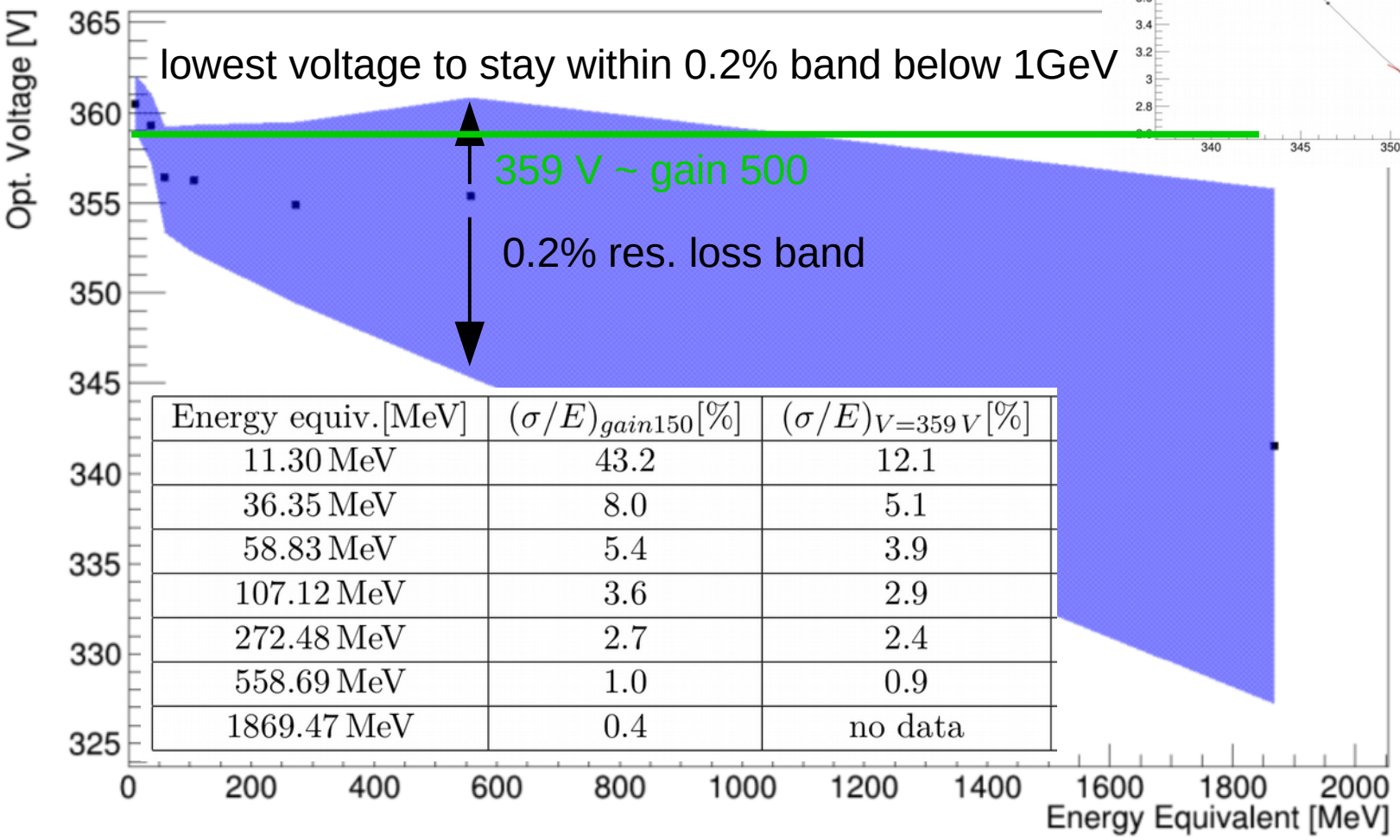

Energy equiv.[MeV]	$(\sigma/E)_{gain150}$[%]	$(\sigma/E)_{V=359\,V}$[%]
11.30 MeV	43.2	12.1
36.35 MeV	8.0	5.1
58.83 MeV	5.4	3.9
107.12 MeV	3.6	2.9
272.48 MeV	2.7	2.4
558.69 MeV	1.0	0.9
1869.47 MeV	0.4	no data

APD Gain Optimization for the APFEL ASIC

Discussion

PWO-II LY @ +18°C: 20 PMT-phe/MeV
PWO-II LY @ -25°C: 100 PMT-phe/MeV (LY@18°C X4)

APD covers ~13% crystal endface
PMT QE = 20%, LAAP QE= 80% → 52 APD-phe/MeV
APFEL ASIC max Input: 8.5 pC

$$E_{max}(gain_{opt}500) = \frac{8.5\,10^{-12}\,C}{52 \cdot 1.6 \cdot 10^{-19}\,C/MeV \cdot 500} = 2043.3\,MeV$$

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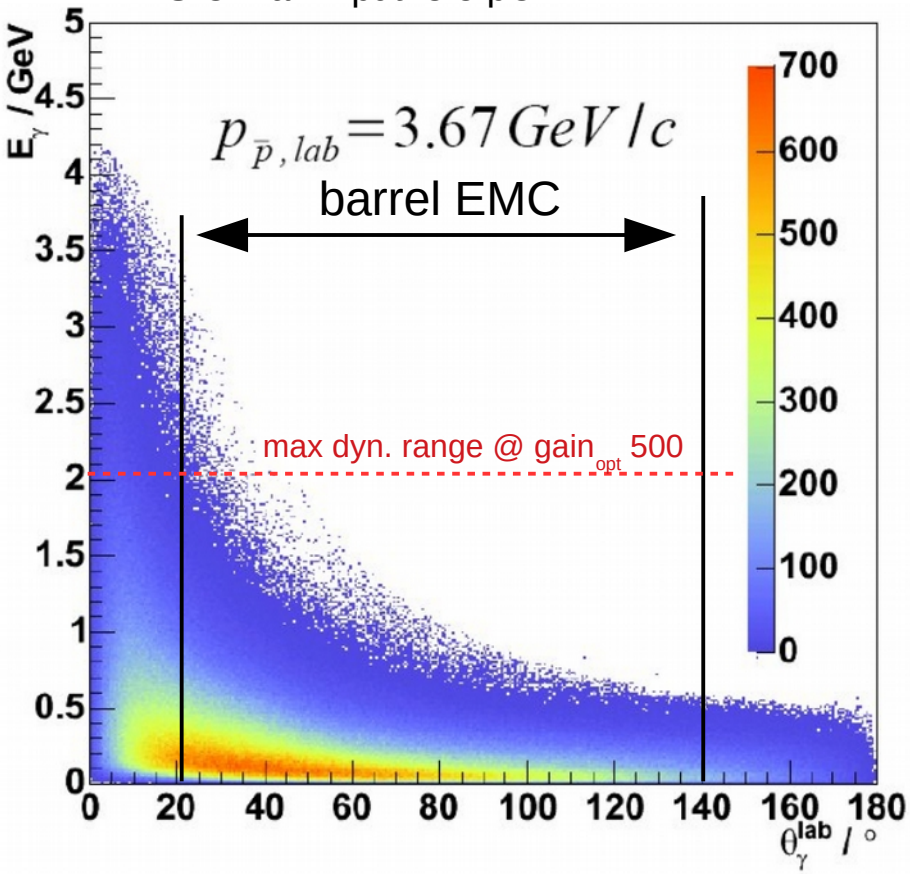

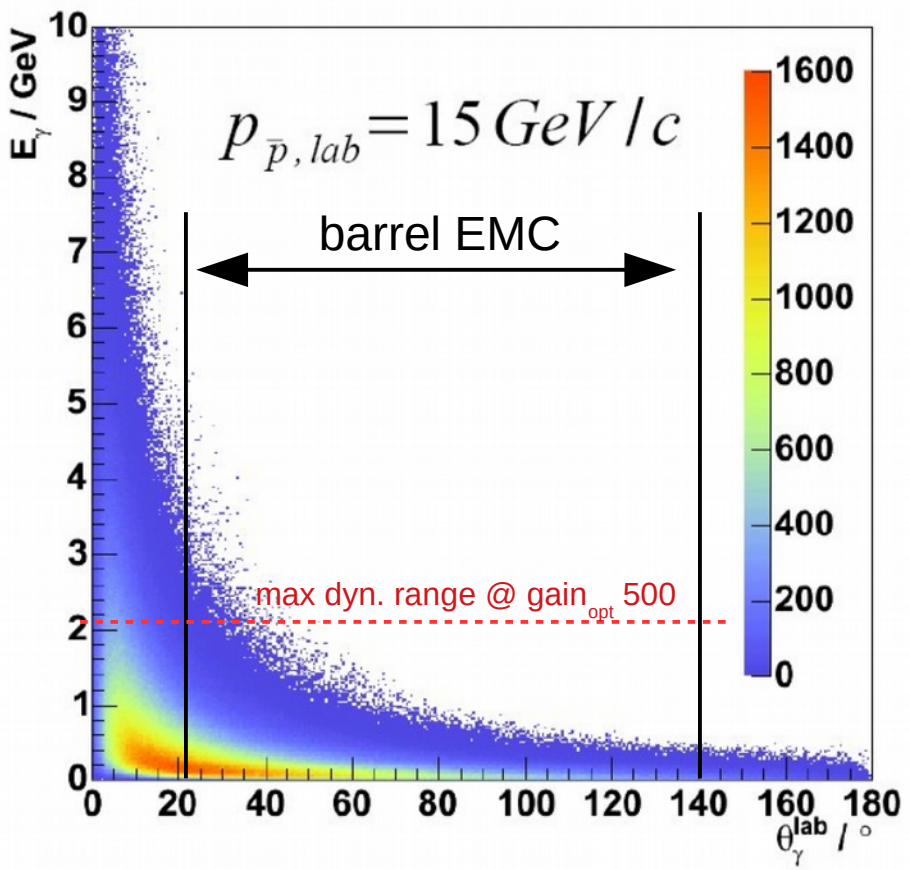

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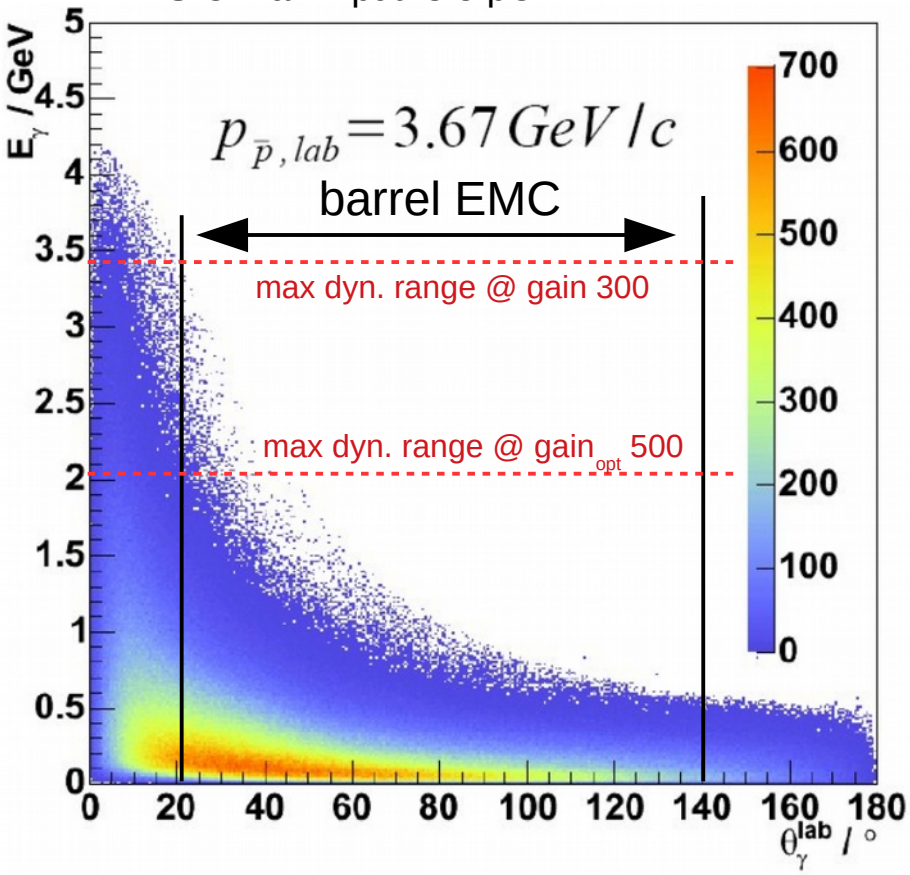

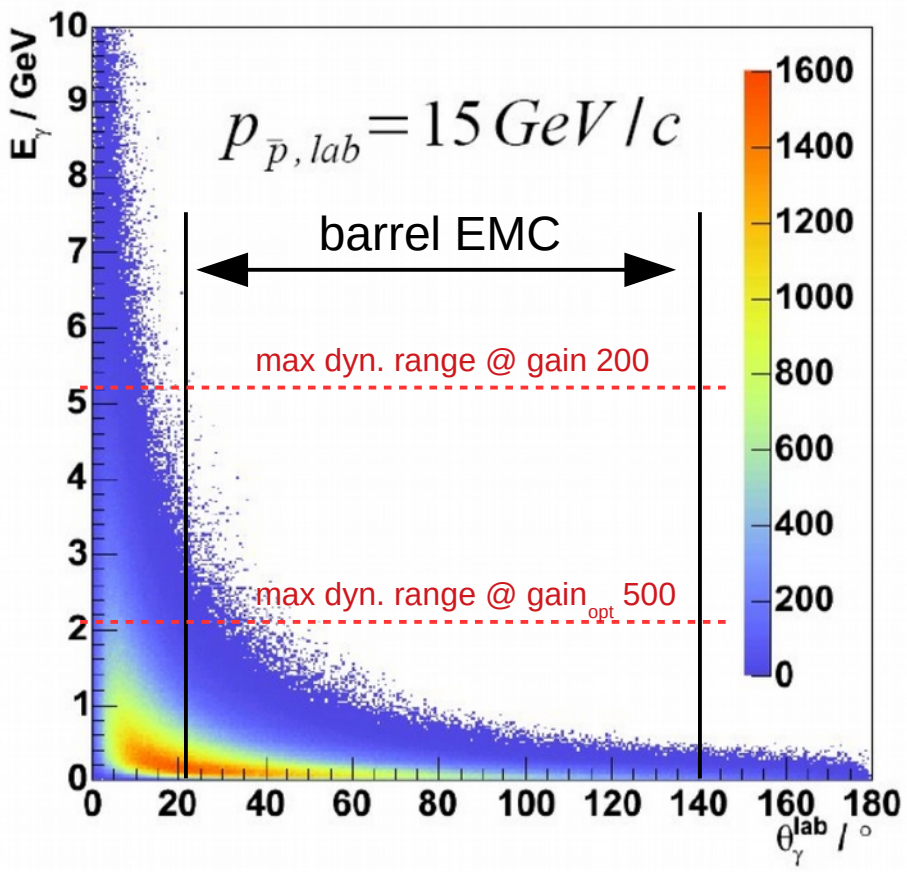

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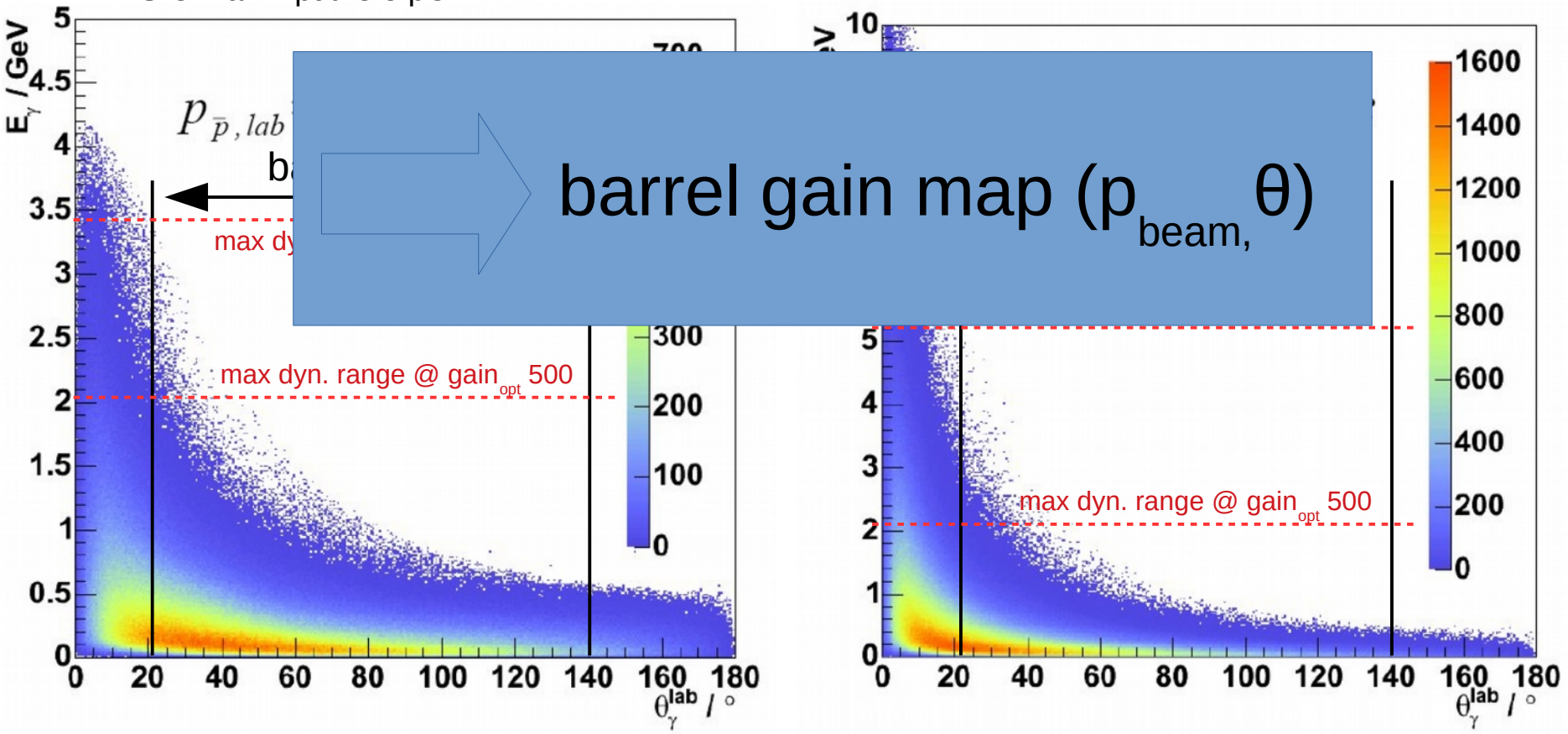
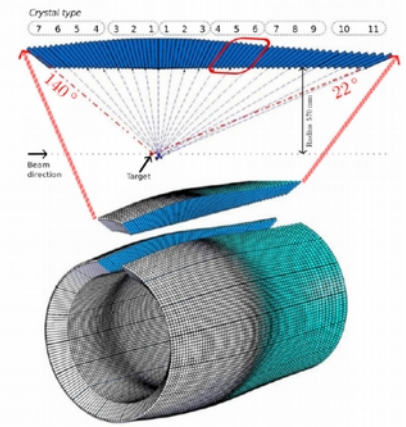
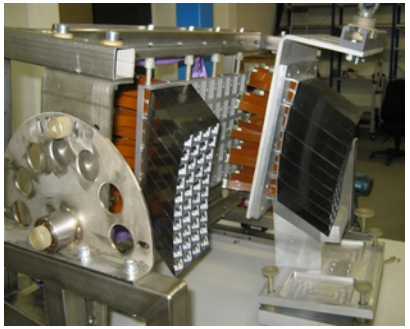


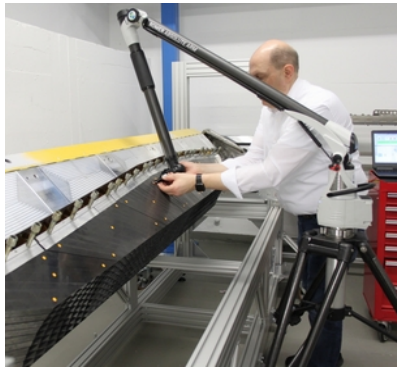
Slice Assembly Status

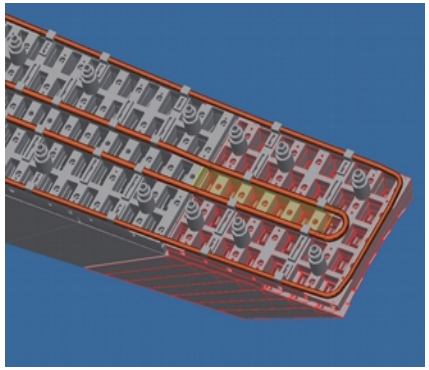
Envisaged milestone (M8):
Assembly of 1st full Barrel EMC slice

- Infrastructure ✓
- Mechanics (except Supportbeam) (✓)
- 710 detectors ✓
  - 710 crystals in 11 different geometries ✓
  - 1420 APDS
    - Screening including irradiation ✓
    - Matching ✓
    - Glueing ✓
  - Capsules ✓
  - Wrapping ✓
- Assembly of 18 modules ✓
- Assembly of Supermodules ✓
  - 360 left and 360 right handed APFEL-ASIC with flex PCBs ✓
  - ASIC housing or fixtures ✓
- Assembly of full slice X
  - Cooling & thermal insulation in progress
  - Backplanes in progress
  - Light pulser fiber coupling in progress
  - Design Supportbeam in progress





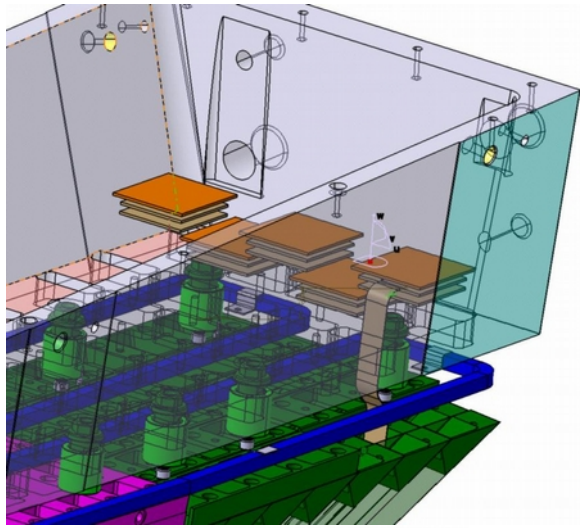


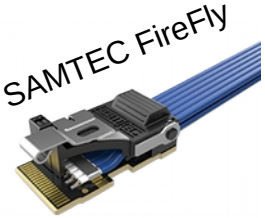


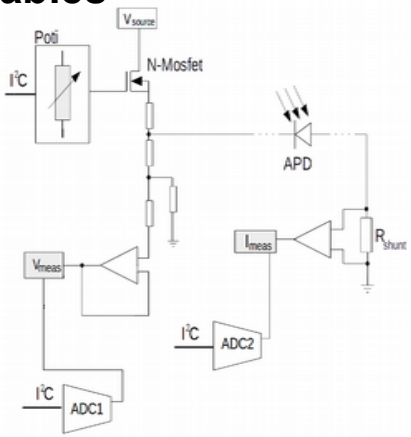
Slice Assembly Status – Serial Adapter ASIC

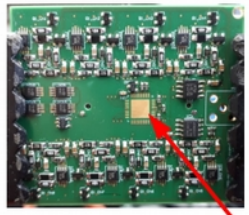
Barrel Backplanes: 3 Layers

- **Top: HV distribution & regulation**
  - Adjust bias voltage of 8 APDs
  - 50V from HV input downwards in < 0,1V steps
  - All channels fed from the same HV source
    → safes space inside support beam
  - Online measurement of APD voltage and current
- **Middle: Connector board for signal cables**
- **Bottom: Board for FlexPCBs / ASICS**
  - Connectors to FEs
  - 8x2 Diff. Line drivers
  - APFEL I/F buffers
  - Temp/Humidity sensors









8-ch HVD final prototype
size: 6 x 5.5 cm²

Serial Adapter ASIC
(next slide)

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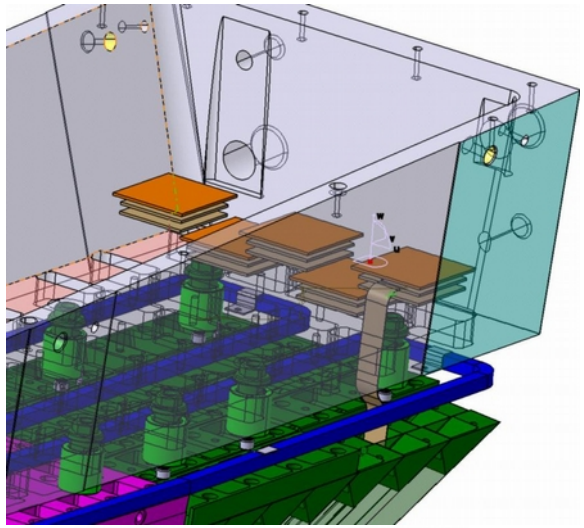
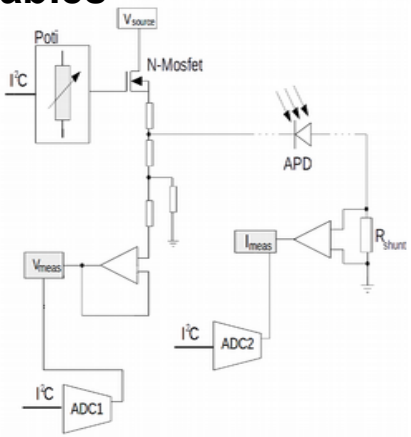
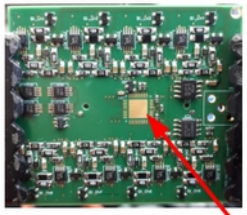




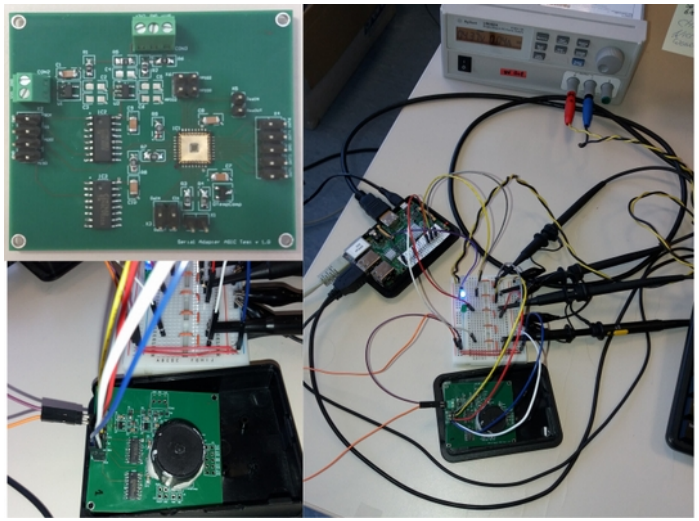


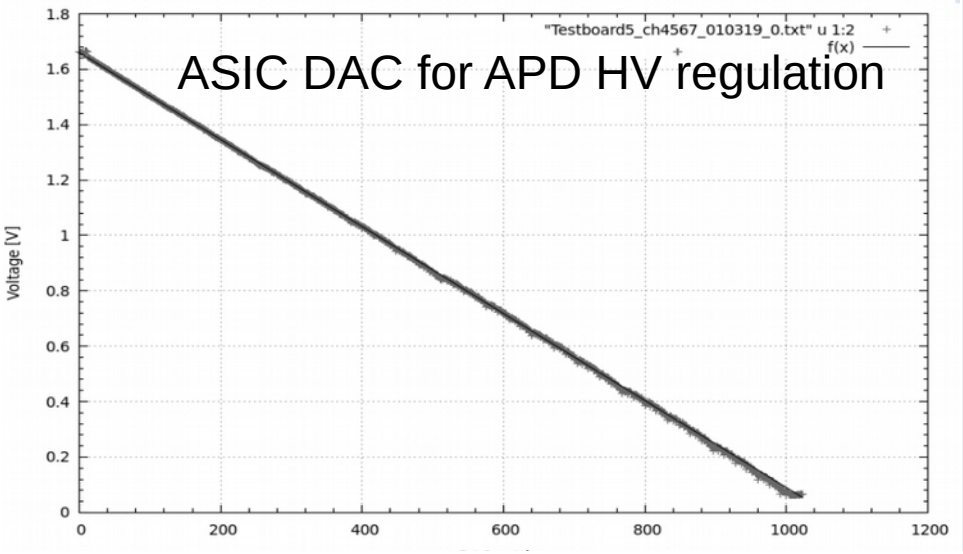
8-ch HVD final prototype
size: 6 x 5.5 cm²

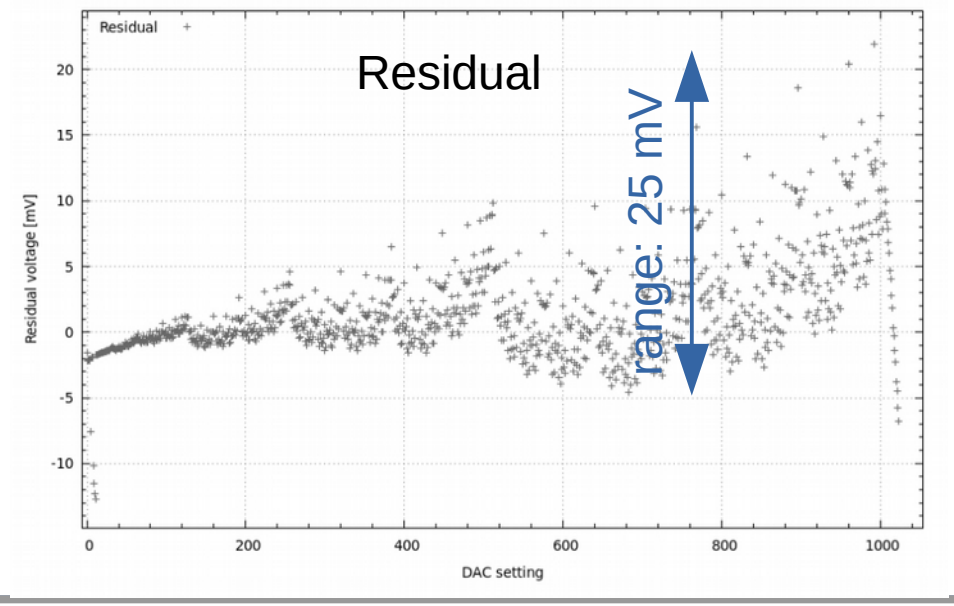
Combines different FE busses & DAC for HV adjustments

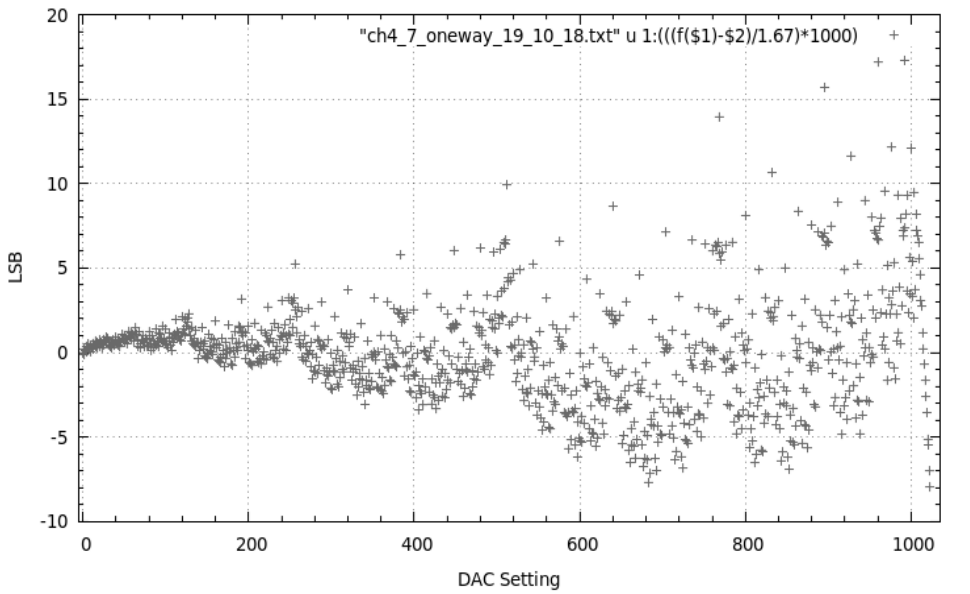
Serial Adapter ASIC (next slide)

Slice Assembly Status – 1st Serial Adapter ASIC

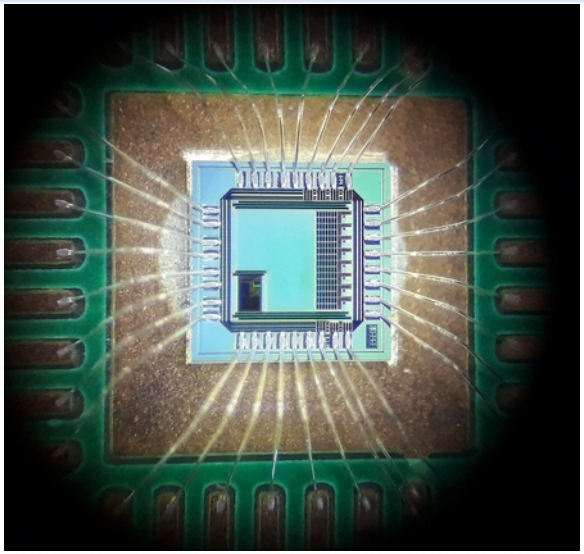


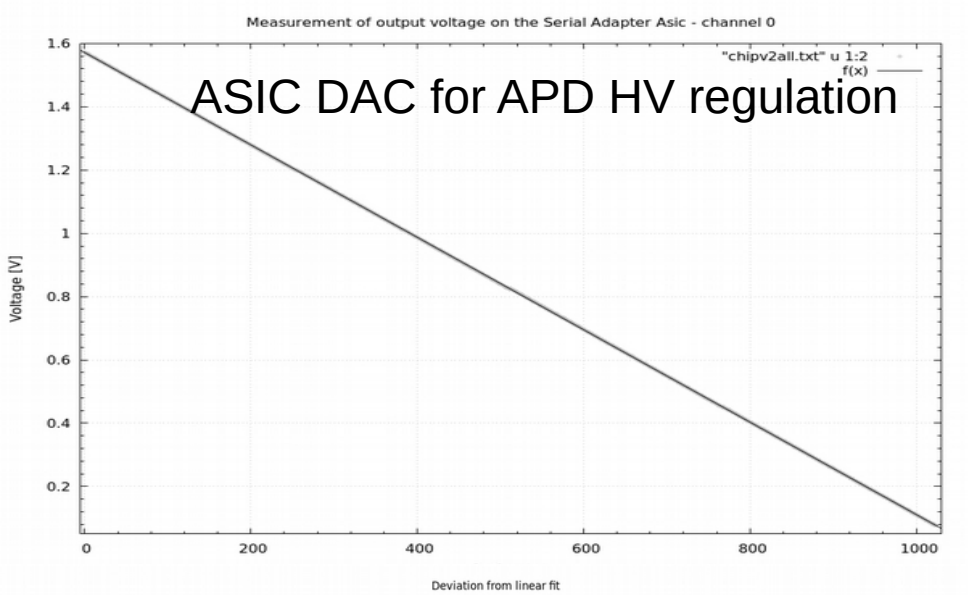


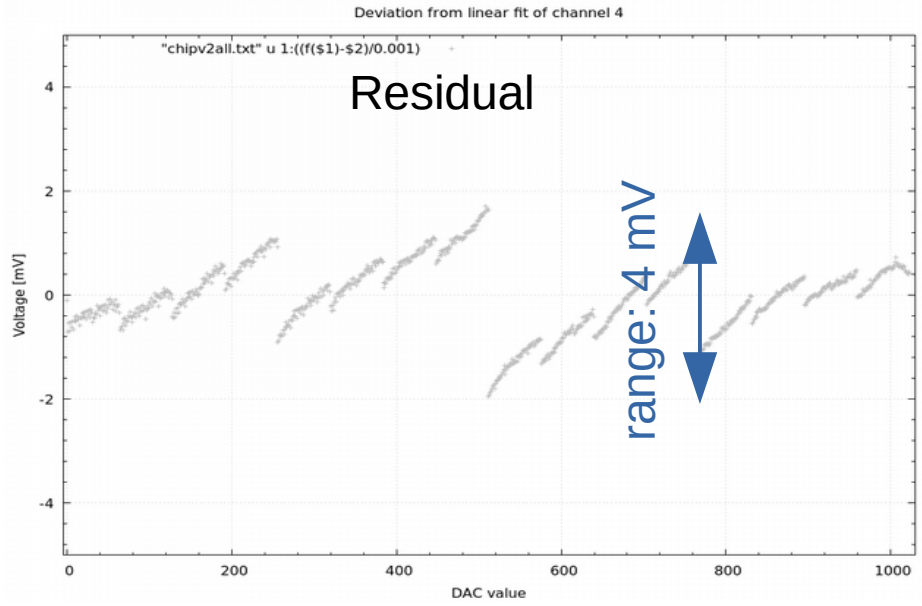


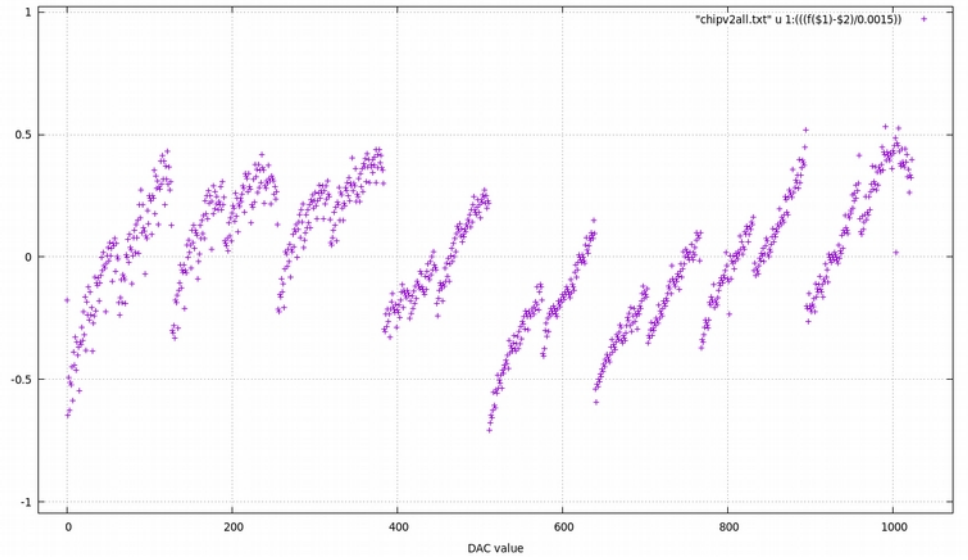


Slice Assembly Status – 2nd Serial Adapter ASIC

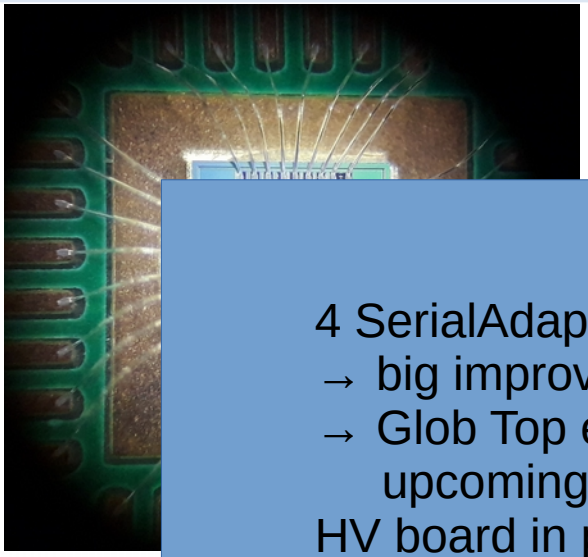


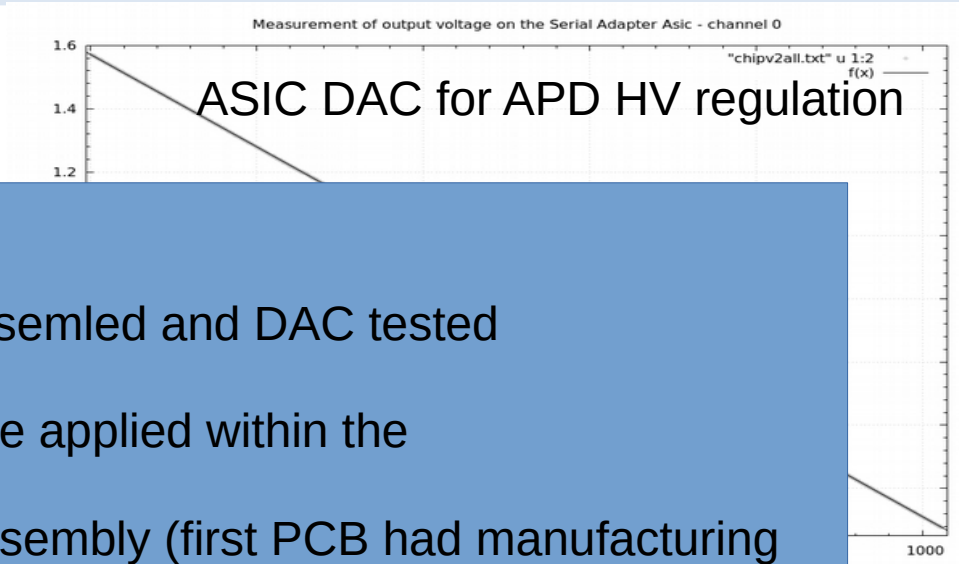






Slice Assembly Status – 2nd Serial Adapter ASIC

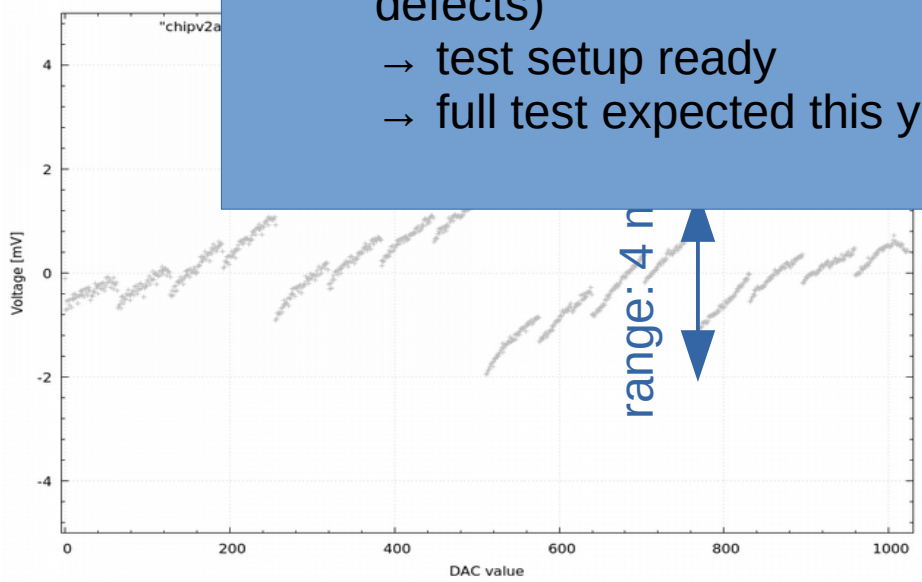




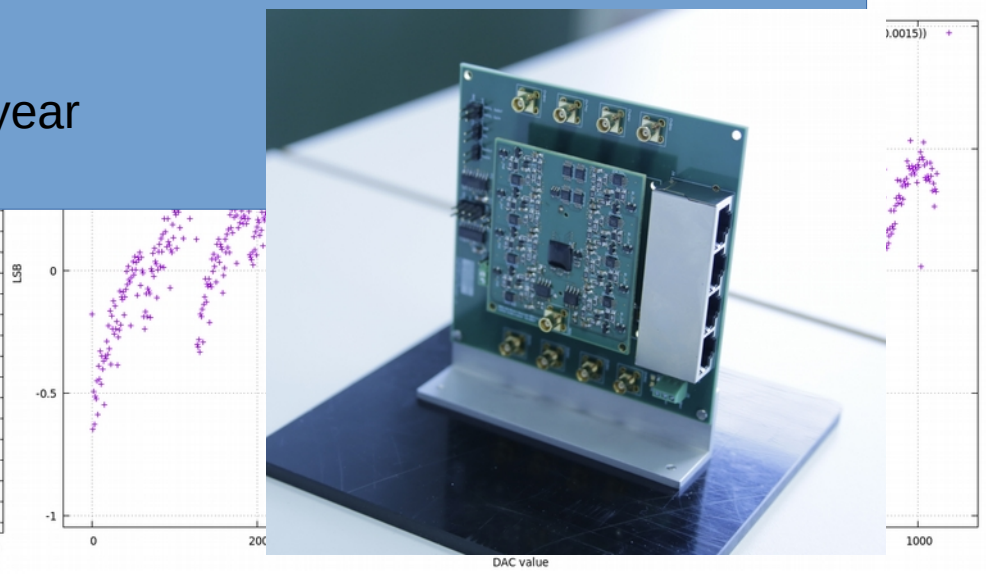
ASIC DAC for APD HV regulation

4 SerialAdapter (V110) assemled and DAC tested
→ big improvement
→ Glob Top expected to be applied within the upcoming weeks

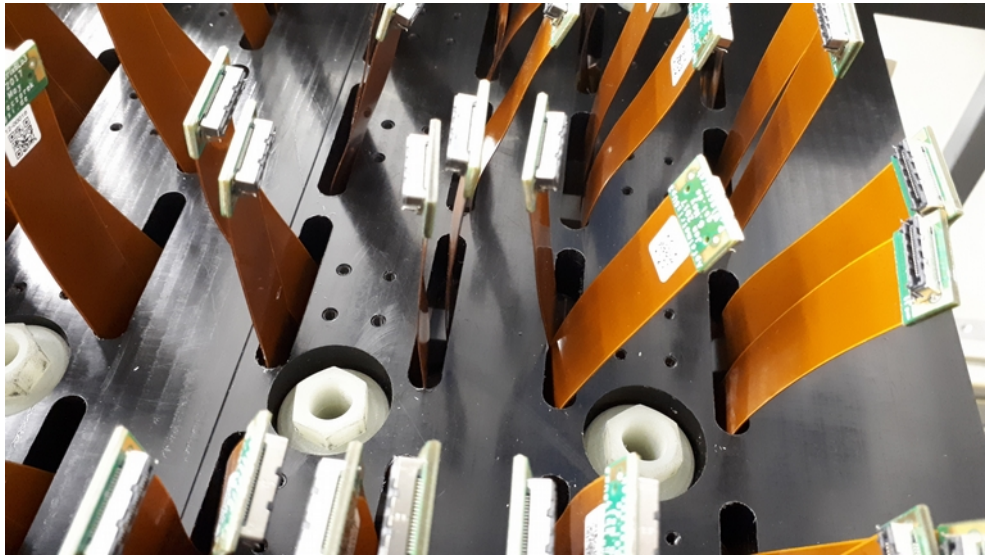
HV board in production/assembly (first PCB had manufacturing defects)
→ test setup ready
→ full test expected this year



range: 4 n



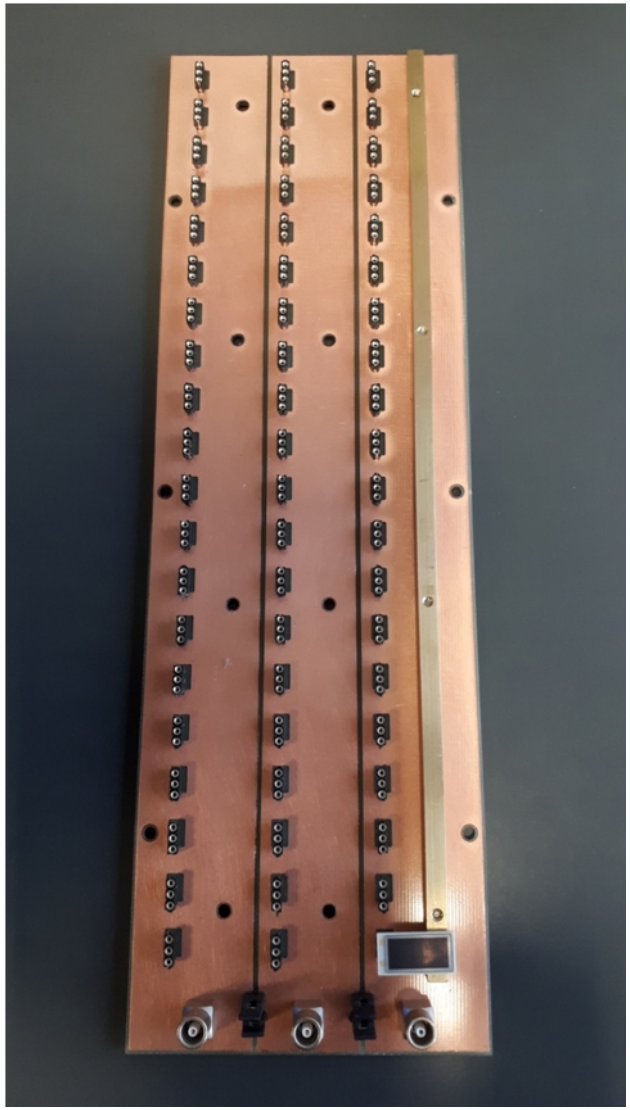
Slice Assembly Status – Support Beam Optimization

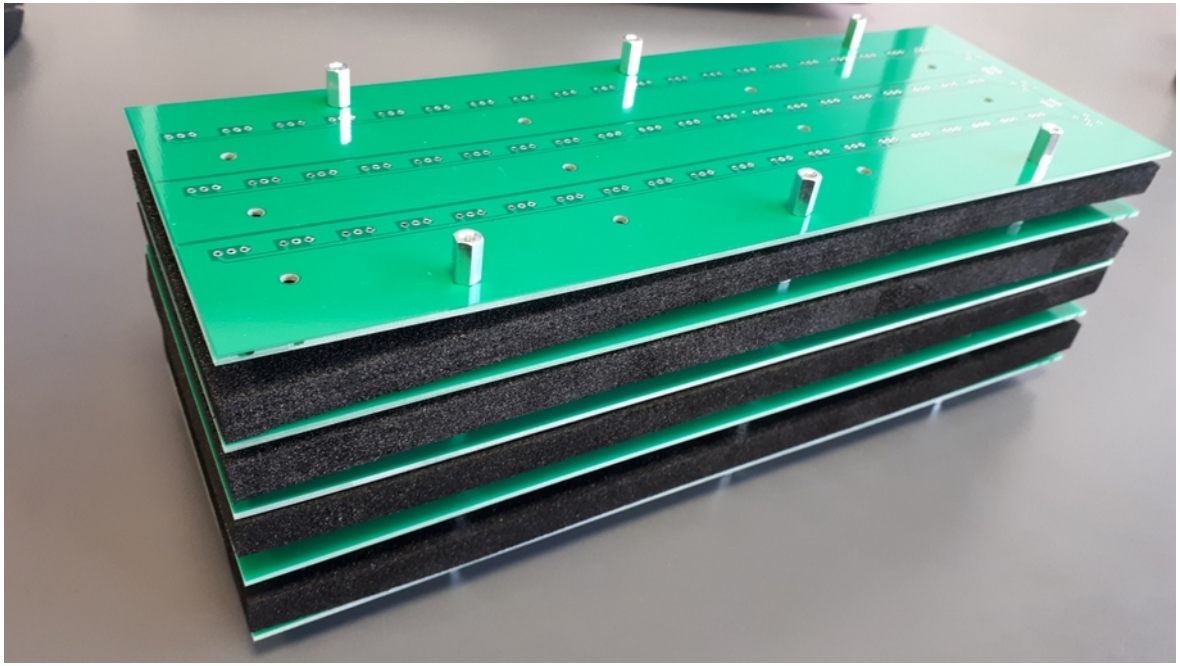


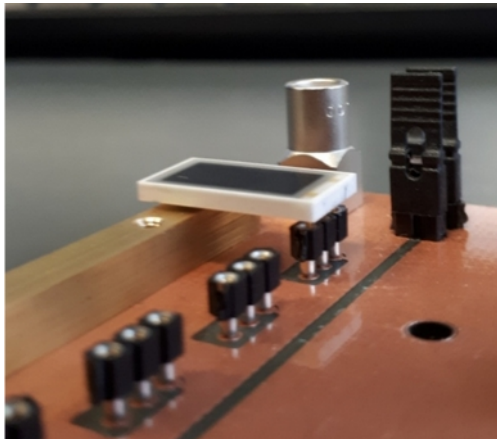
Slice Assembly Status – Support Beam Optimization

mechanical stiffness
needs to be reevaluated

APD Handling PCBs





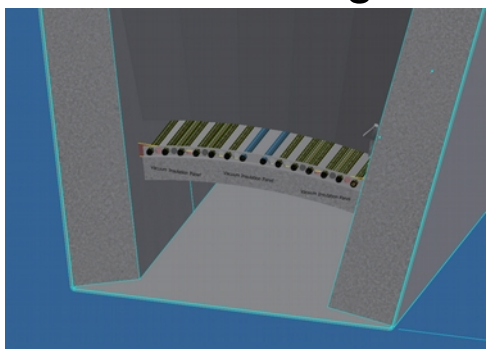


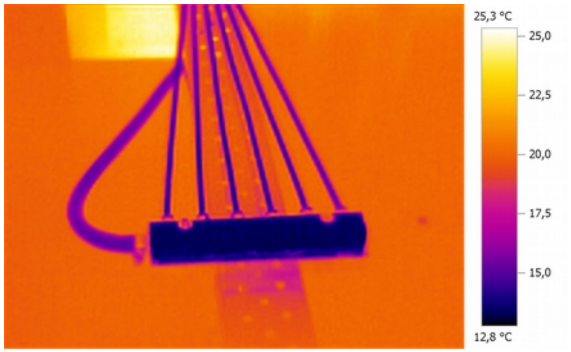
- PCBs can be used for
  - Irradiation
  - Annealing
  - Transportation
- 60 APDs each

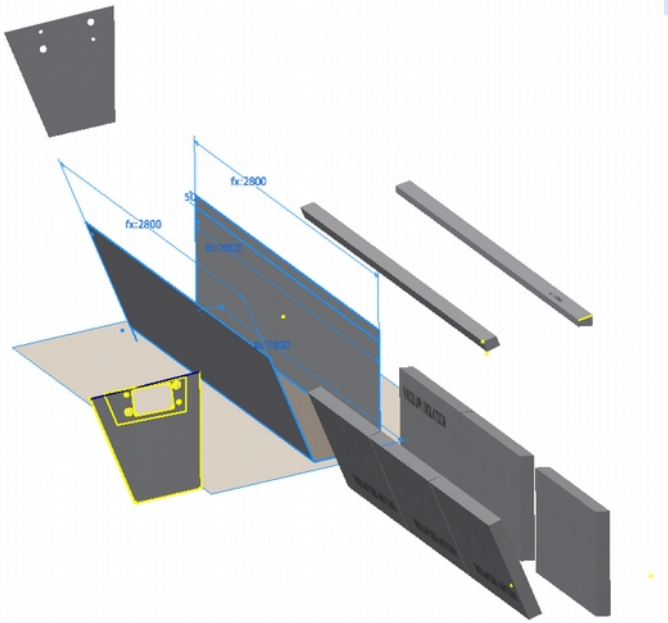
APD irradiation

Cooling

- Workshop @ Bochum produces box currently
- Front-Cooling geometry and material tests ongoing
- Different geometries for coolant lines for optimal flow/cooling power and homogeneous flow distribution using manifolds







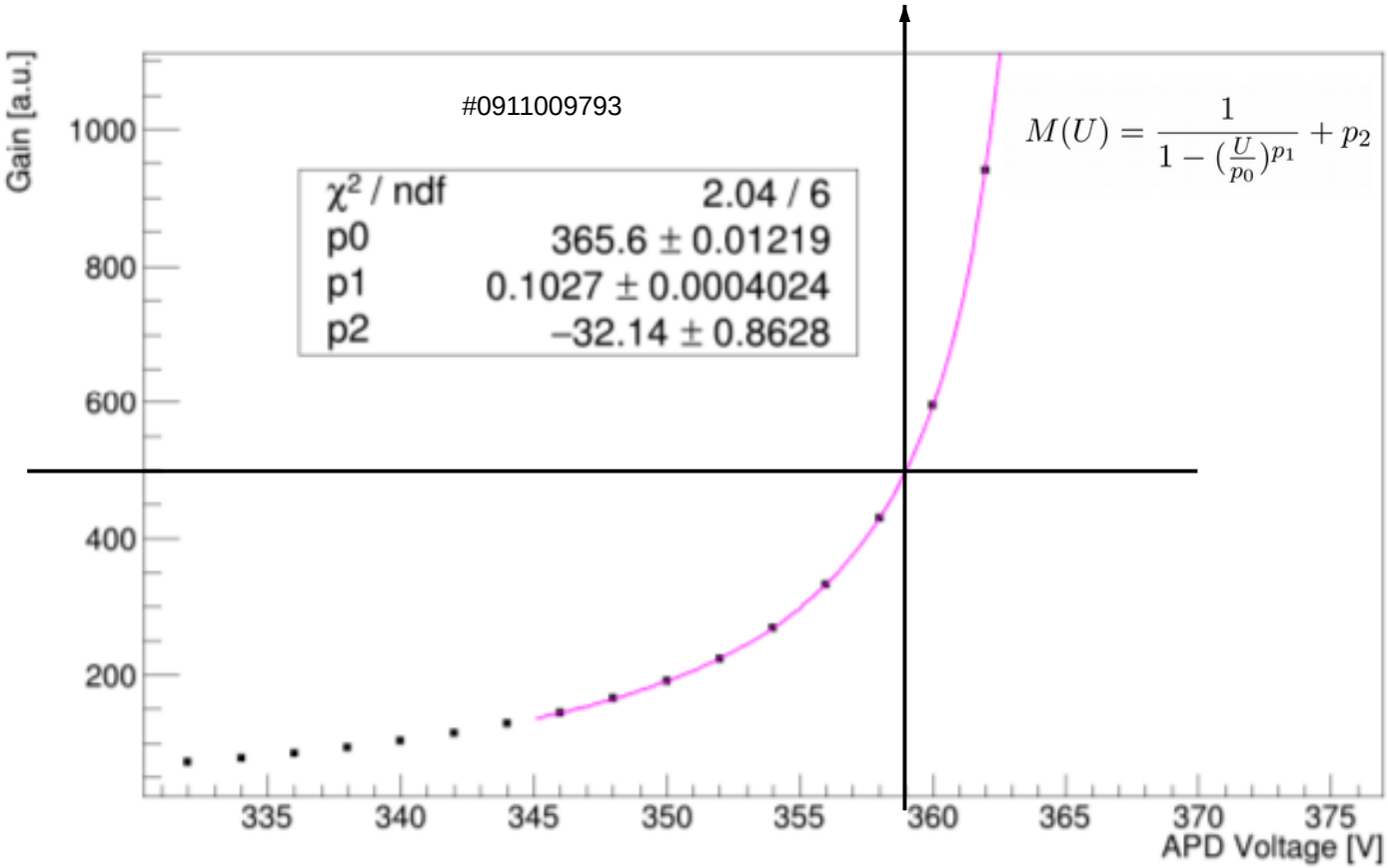
- Adapting PANDA THMP Hardware to be used with all sensors for pre-series Slice Test (pressure drop, flow, temp...)

Conclusion

- **APD gain**
  - Increment up to 500 will improve the energy resolution
  - Gain map with respect to the needed dyn. Range ($p_{beam,}$ θ)
- **Serial Adapter ASIC**
  - DAC bug for APD HV regulation is fixed
  - Full test of HV regulation board will be completed this year
- **Mechanics**
  - Mock-up of new support beam design is ready
  - Stiffness of new design unknown
- **Cooling 1st Slice**
  - Cooling-box is currently produced by the workshop in Bochum
  - Flow and thermal insulation optimizations are ongoing
  - PANDA-THMP system is currently prepared for 1st Slice test

BACKUP SLIDES

Backup


#0911009793
$M(U) = \frac{1}{1-(\frac{U}{p_0})^{p_1}} + p_2$
χ^2 / ndf 2.04 / 6
p0 365.6 ± 0.01219
p1 0.1027 ± 0.0004024
p2 −32.14 ± 0.8628
Gain [a.u.]
1000
800
600
400
200
335
340
345
350
355
360
365
370
375
APD Voltage [V]