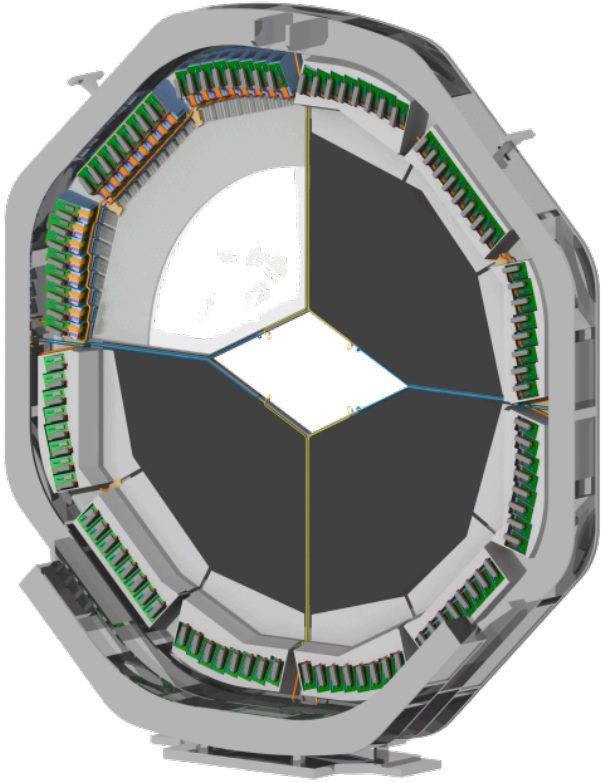
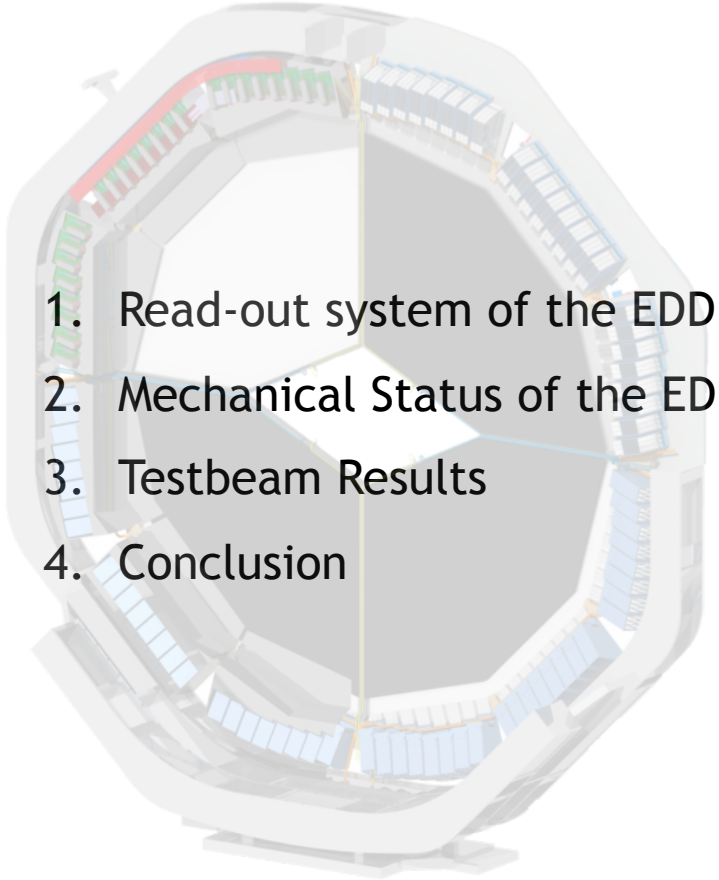
Status of the PANDA Endcap Disc DIRC Project



Simon Bodenschatz, Lisa Brück, Michael Düren, Avetik Hayrapetyan, Jan Hofmann, Sophie Kegel, İlknur Köseoğlu-Sari, Jhonatan Pereira de Lira, Mustafa Schmidt, Marc Strickert

PANDA CM 19/3- 2019/11/03

Outline



1. Read-out system of the EDD
2. Mechanical Status of the EDD
3. Testbeam Results
4. Conclusion

Existing Design (2018 - 2019)

ToFPET 2 PETsys

Analog signal (MCP-PMT)

Digitized signal (FEM)

FEB_D_v2 (FPGA)

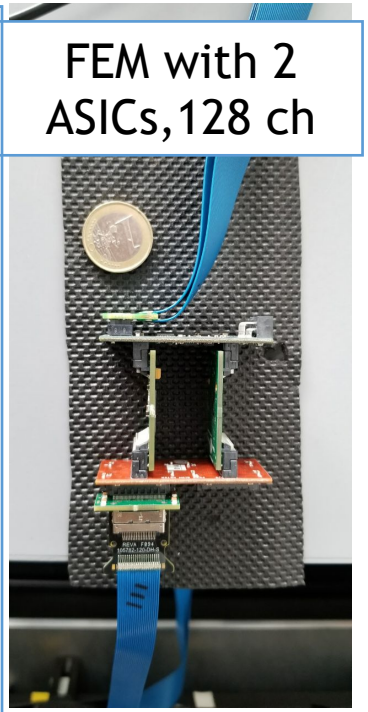
Fan-out box

DAQ board

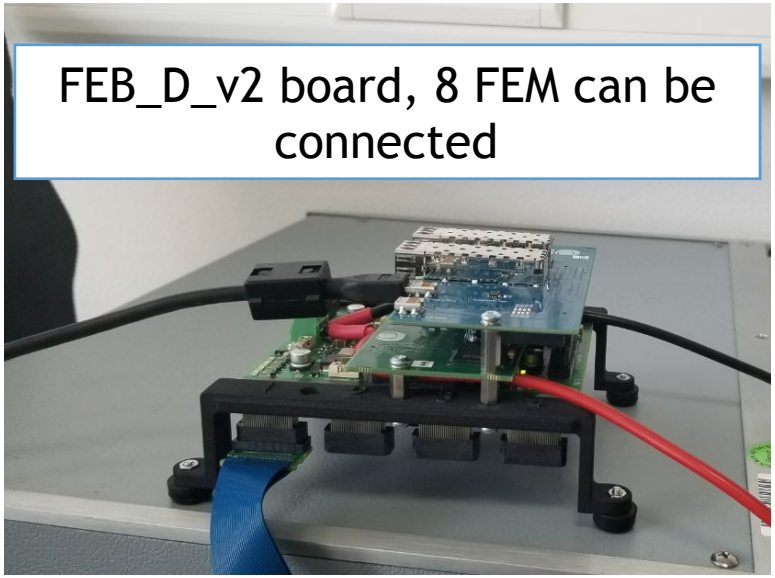
System clock (200MHz)
Synchronization signals

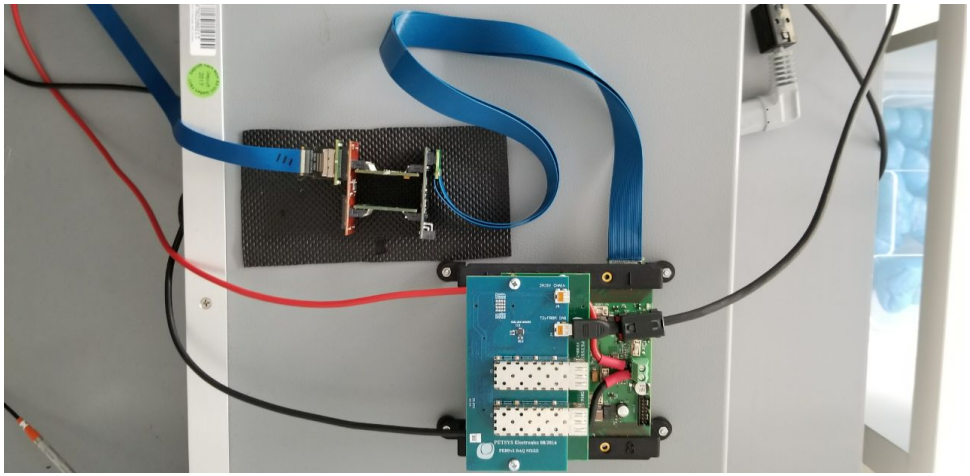
Max data rate 250 Mevents/s

FEM with 2 ASICs,128 ch



FEB_D_v2 board, 8 FEM can be connected



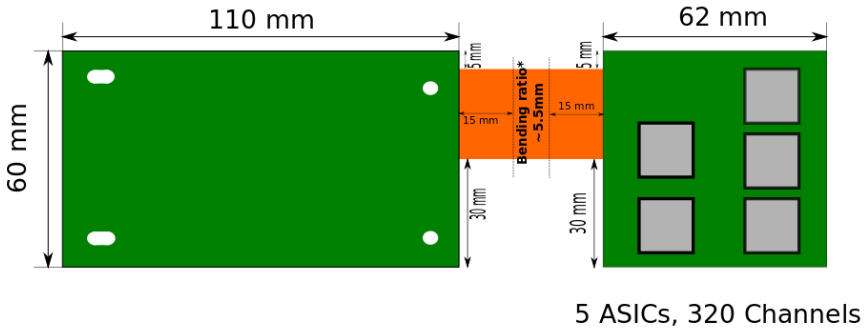


Test beam 2018

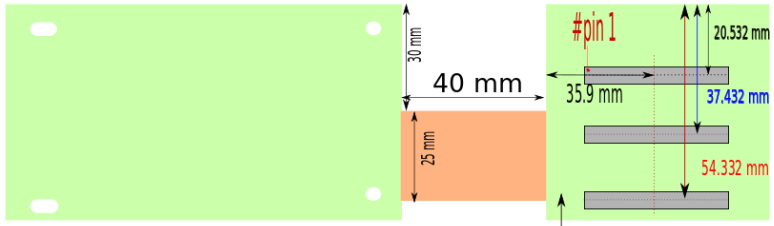
✗ Negative polarity

✓ Positive polarity

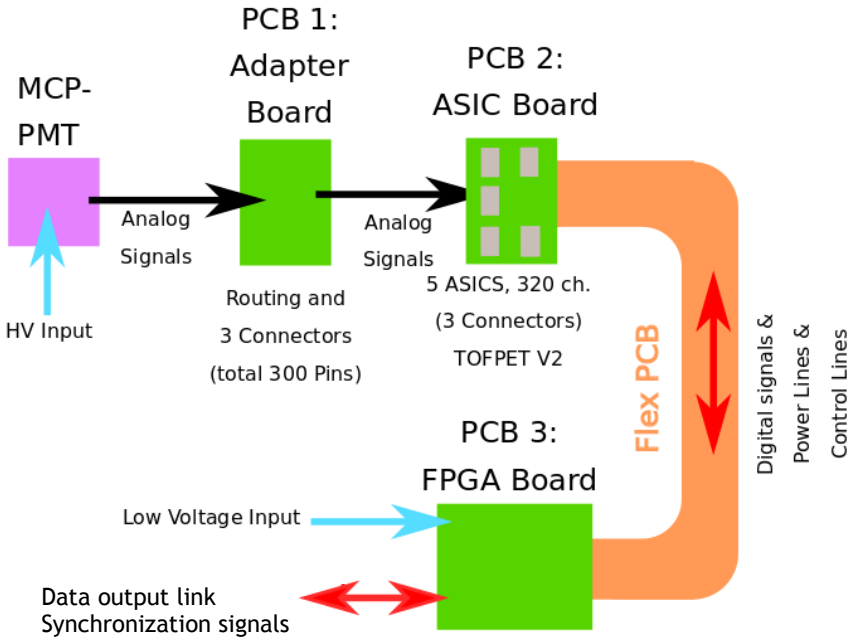
Design for Prototype & Phase 1



5 ASICs, 320 Channels

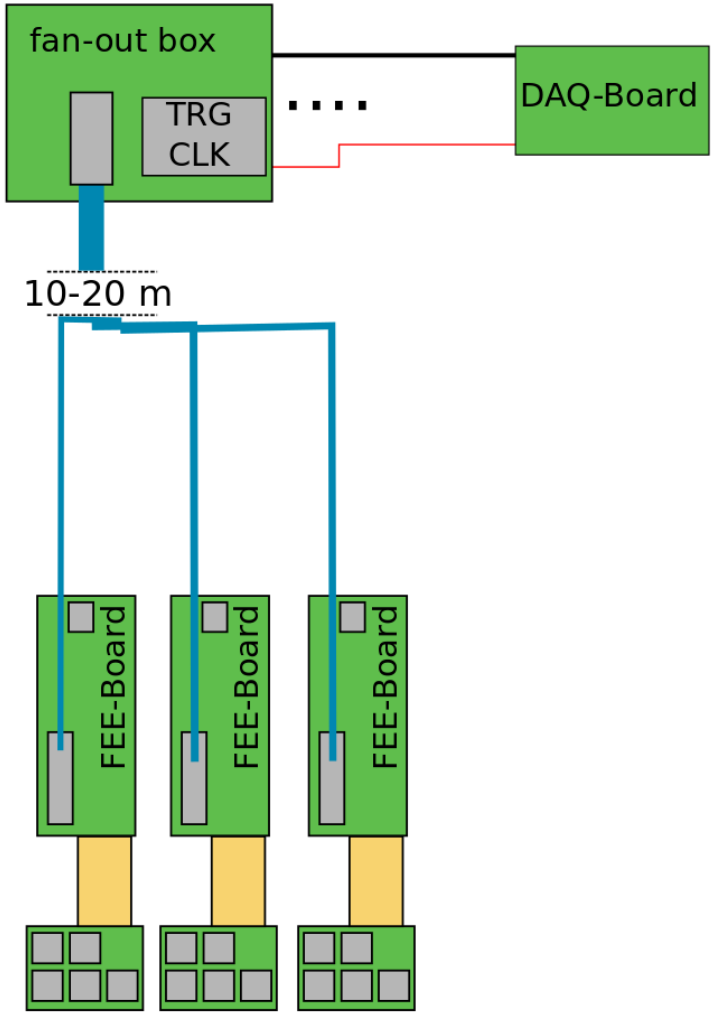


Connectors to adapter PCB



- Design will be done by PETsys company.
- ☑ New ASICs are going to be compatible both negative and positive polarity.
- ☑ New ASICs and 2 FE-Board will be delivered in few months.
- uHDMI - HDMI cable will be used.
- For phase 2, design might be changed according to suggestions of DAQ group.

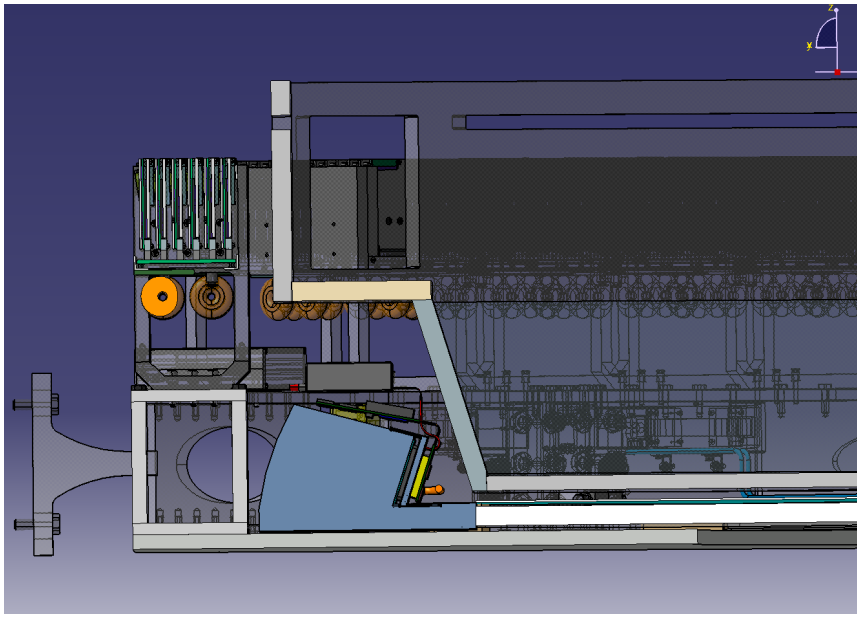
Design for Prototype & Phase 1

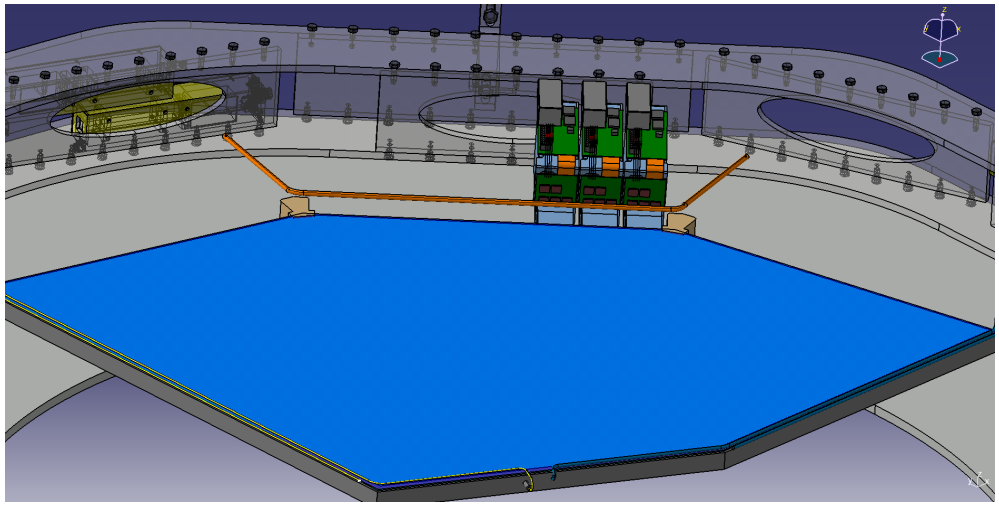


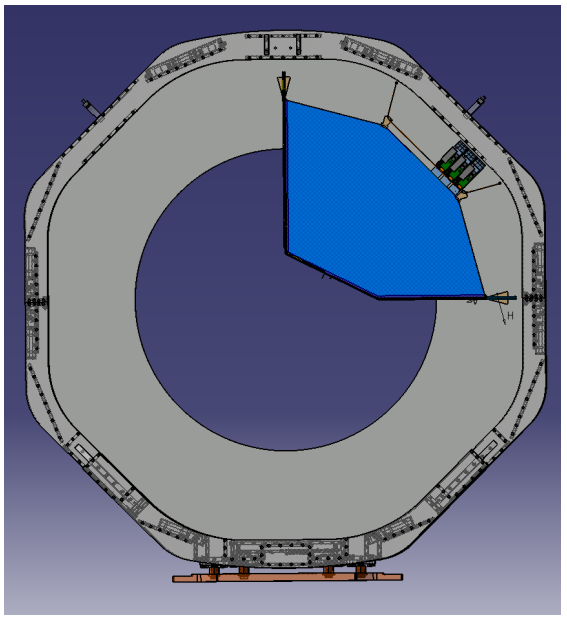
- 3 ROMs, 3 MCP-PMT
  - 1 DAQ-Board for Prototype & Phase 1
- Data will send via uHDMI cable to fan-out box (12 connections)
- Clock & Synchronization will be provided by DAQ-Board

Design for Prototype & Phase 1

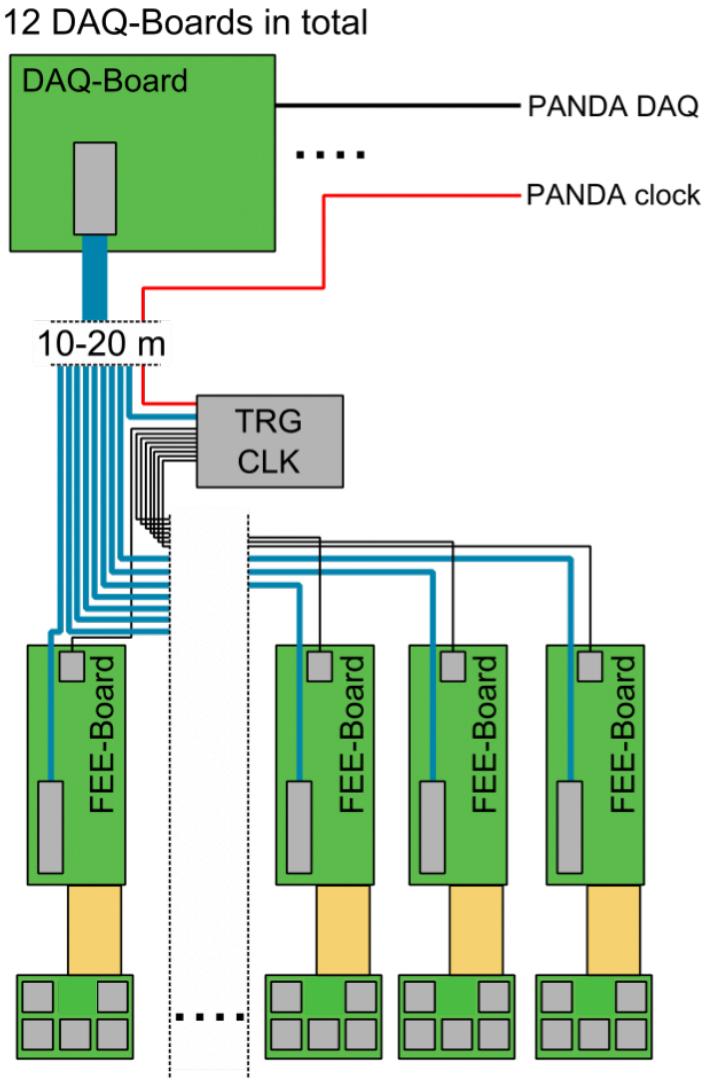
- We need additional funding for a more complete setup during Phase-1.
- Our desire is to have one full quadrant for Phase-1
  - 24 ROMs, 24 MCP-PMTs
  - 72 FEL
- We can install our prototype for phase 1 with 3 ROMs if we will not have an additional funding.







Design for Phase 2



- Depending on the results from Phase-1, FEE design can be changed.
- ASICs board can be combined by DAQ-group design according to their suggestions.

Requirements:

• at maximum 100 kHz per channel

→ converts to 30 MHz per ROM

FEB/D allows up to 10^8 events/s

✓ DAQ-Board allows up to $2.5 \cdot 10^8$ events/s

➢ 8 ROMs per DAQ-Board

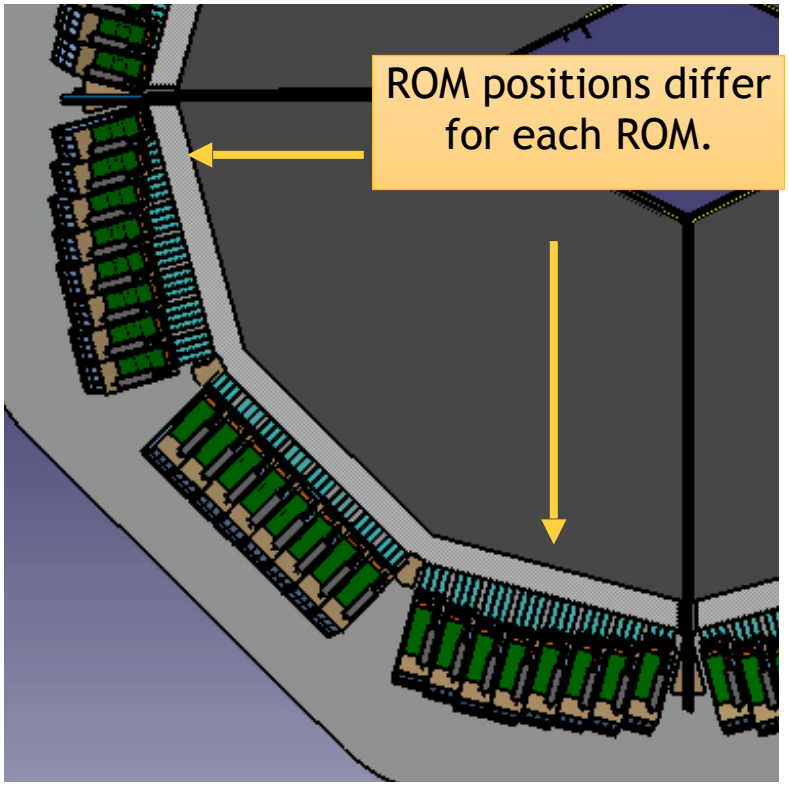
➢ 3 DAQ-Boards per Quadrant

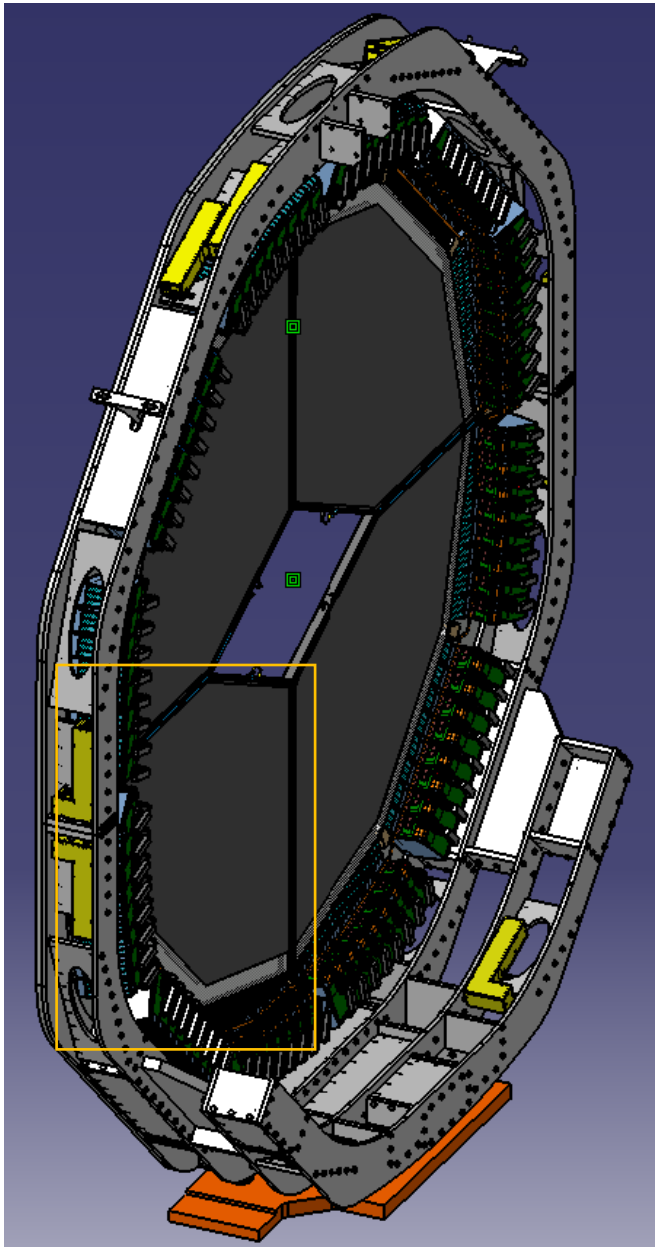
➢ 12 DAQ-Boards in total

(96 FEE-Boards)

Design for Phase 2, Mounting plate & Support frame

- 96 ROMs align around the EDD radiator
- Because of the EMC insulation, ROM position differs for each region.





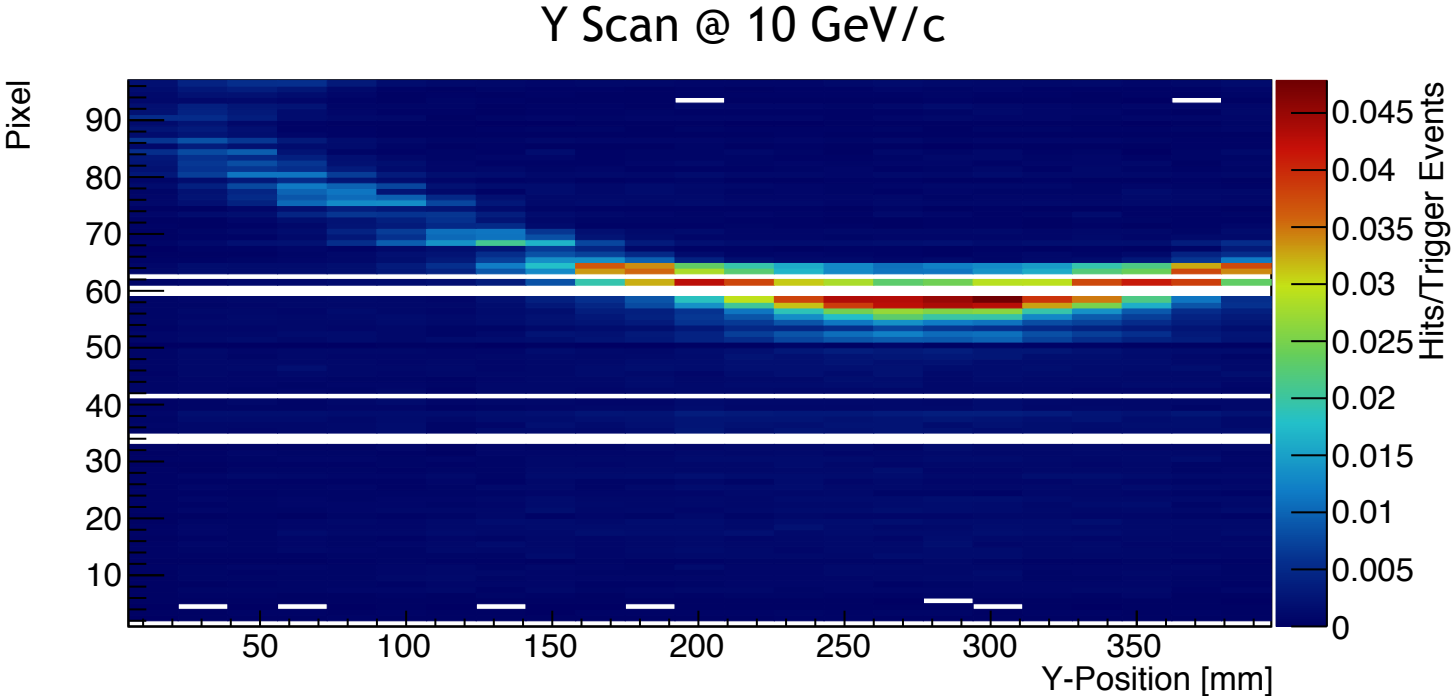
Problems

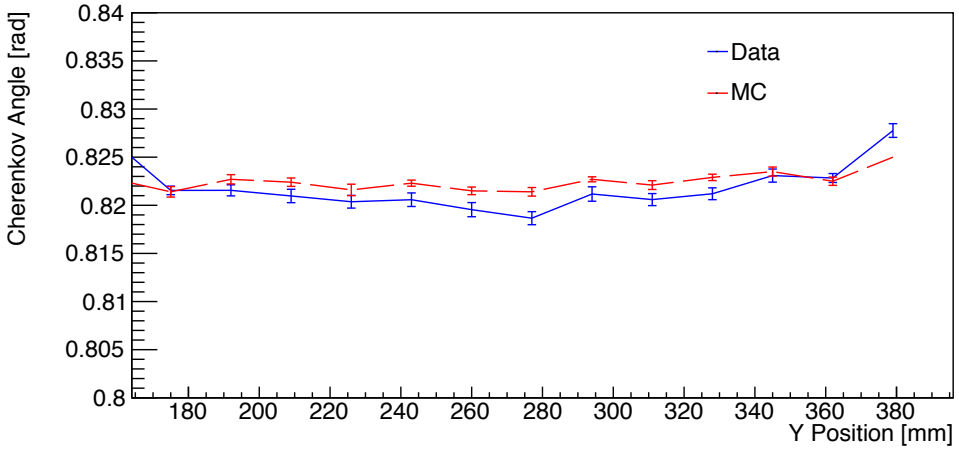
- There are limits both z-direction and radial direction.
- No space for cable alignment
  - HV cables, LV cables, Optical link
- Cooling system for FPGA has not been implemented yet!
- No space for HV divider
- Not enough space for FEE!

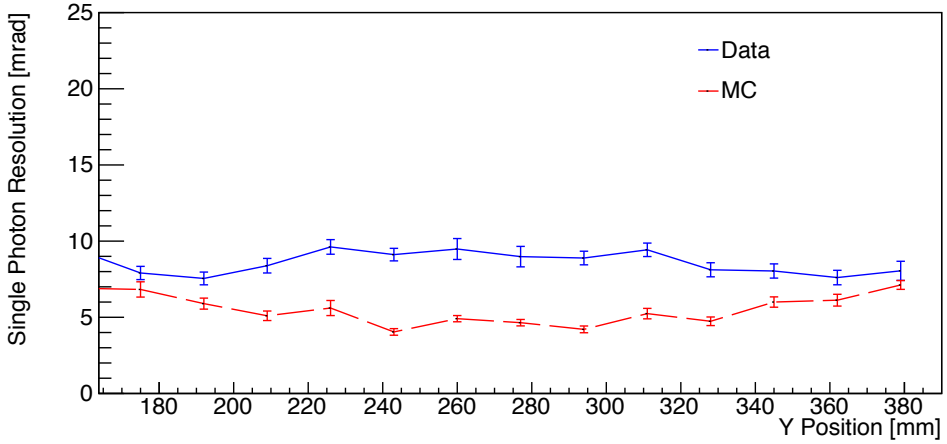
Proposed Solutions from previous CM

1. Reduce number of ROMs in each quadrant, not preferable. (Efficiency loss!)
2. Moving EDD through the upstream direction ~ 23 mm. EDD is in-between GEM detectors and forward EMC. -> GEM group tried to find a solution but as a result this is not possible either.
3. EMC group has already produced insulation part. From neighbors, we could not get extra space!

Selected test-beam results for the EDD Prototype: 2018



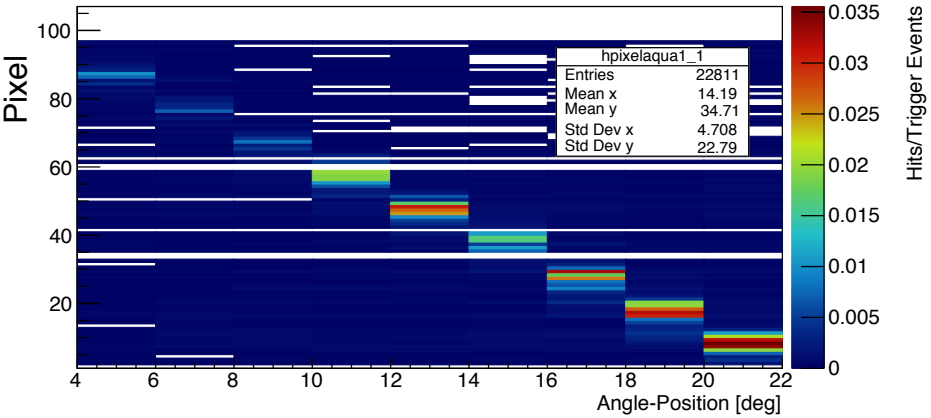




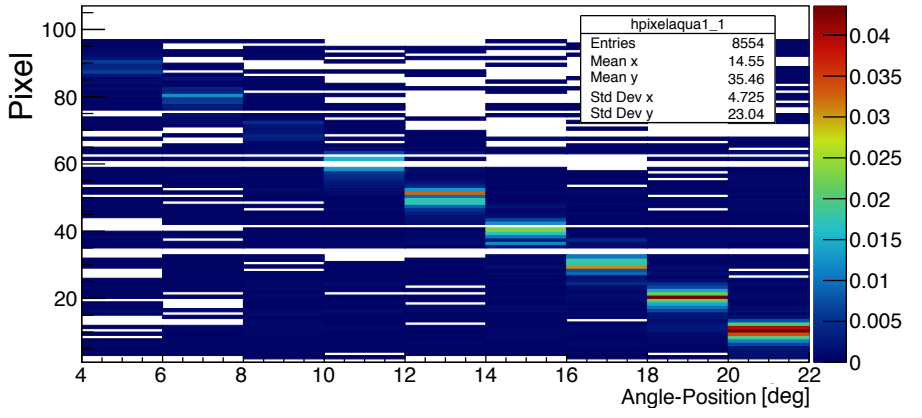
Selected test-beam results for the EDD Prototype: 2018

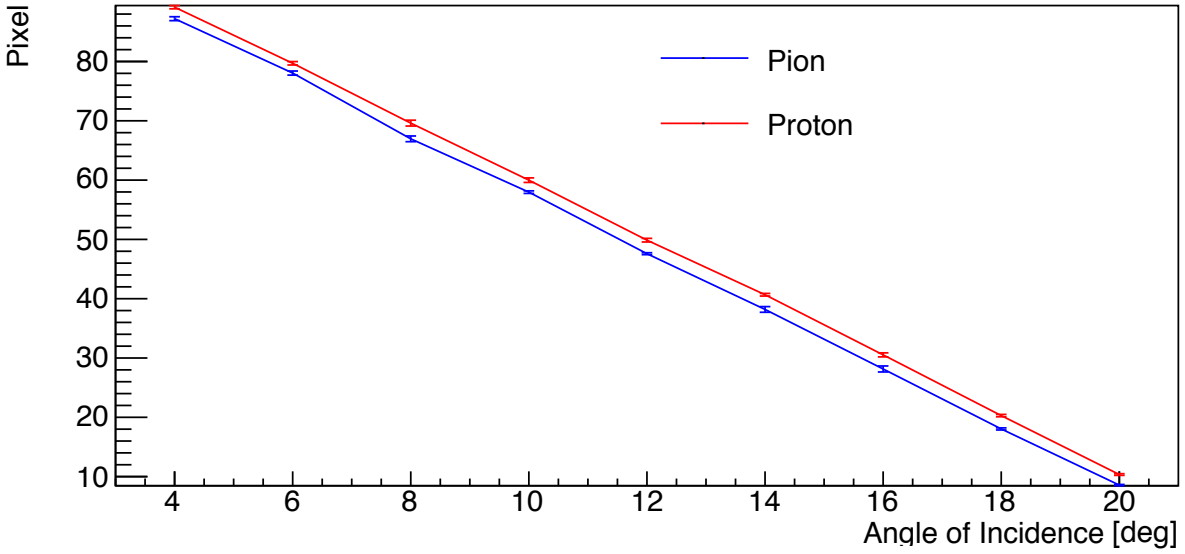
Angle Scan @ 7 GeV/c

Pion



Proton

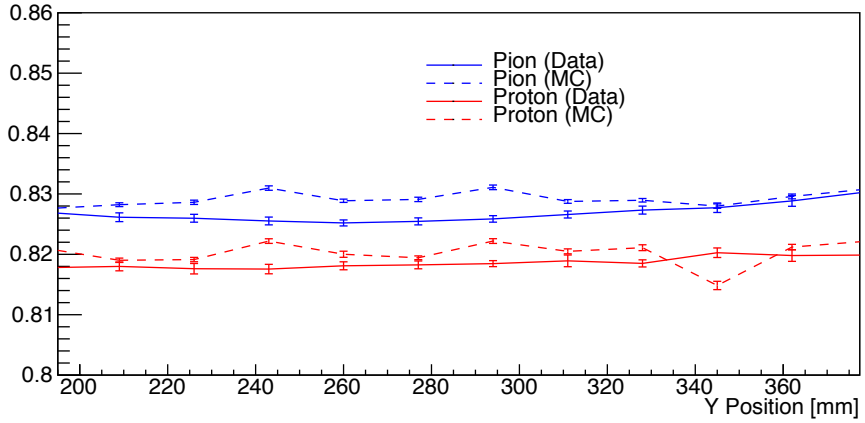




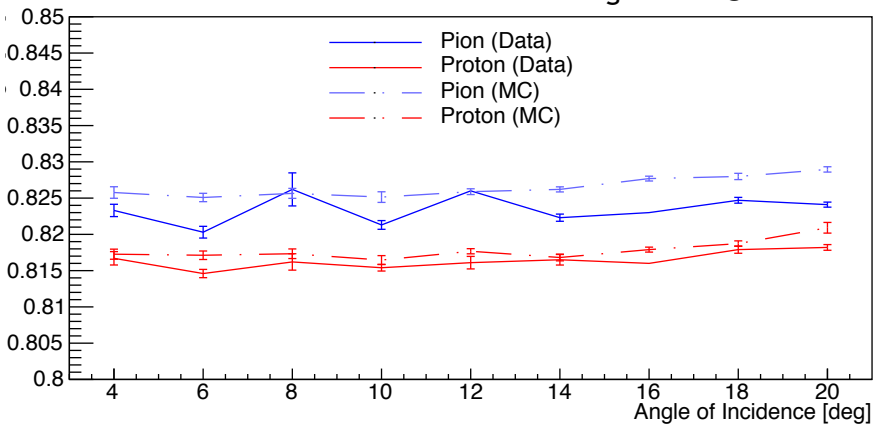
Selected test-beam results for the EDD Prototype: 2018

Cherenkov Angle [rad]

Vertical Scan @ 7 GeV/c

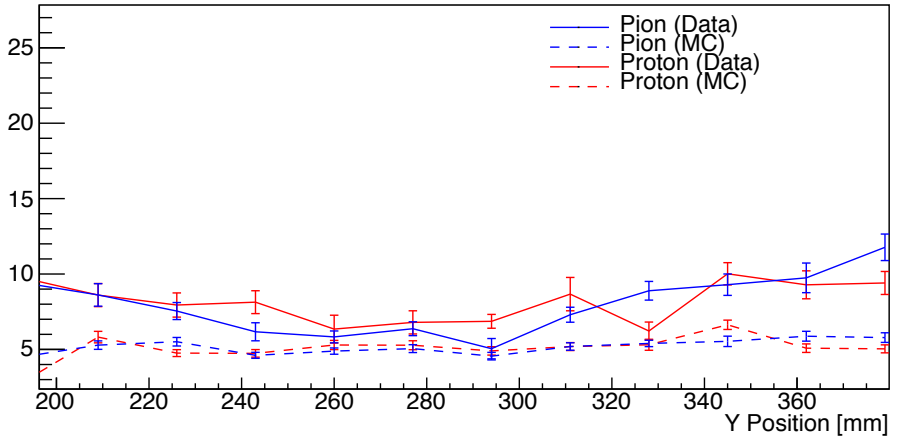


Angle Scan @ 7 GeV/c

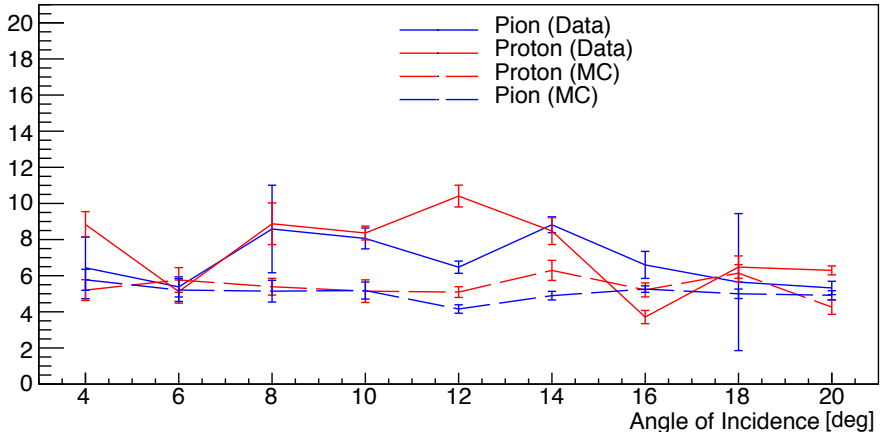


Single Photon Resolution [mrad]

Vertical Scan @ 7 GeV/c

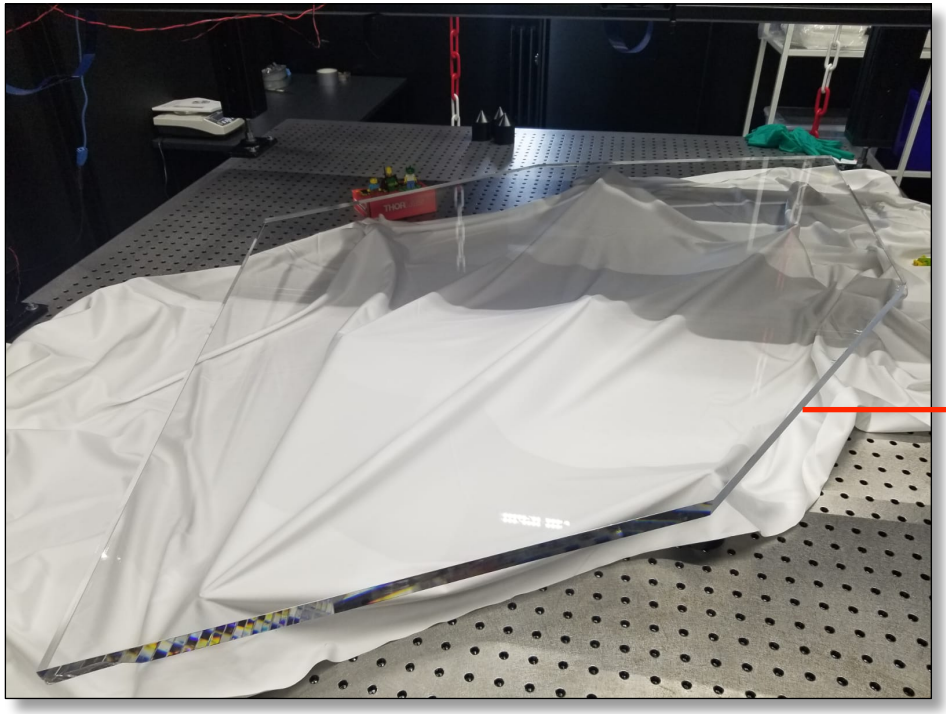


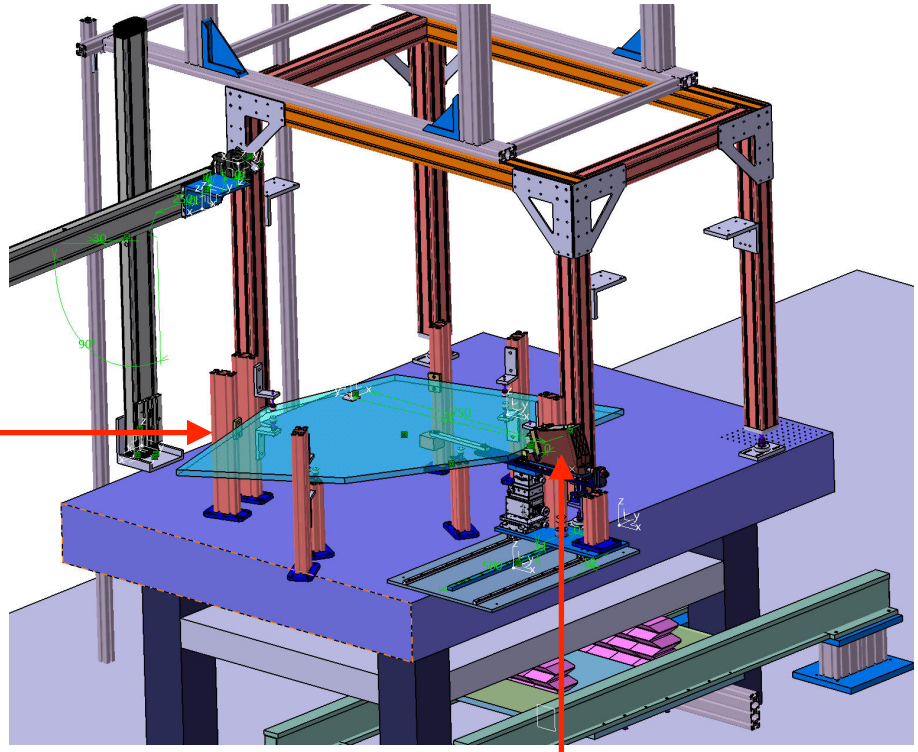
Angle Scan @ 7 GeV/c



Quality Measurements

- Quality measurements will be done. A setup for optical quality control is currently tested by Sophie Kegel.

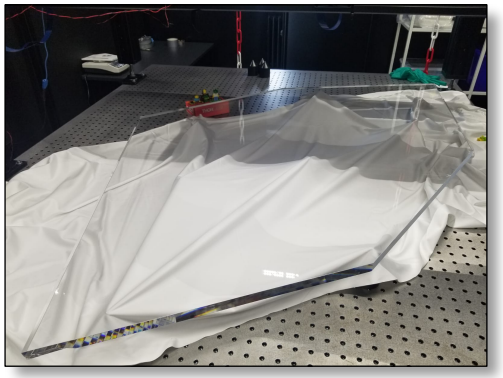




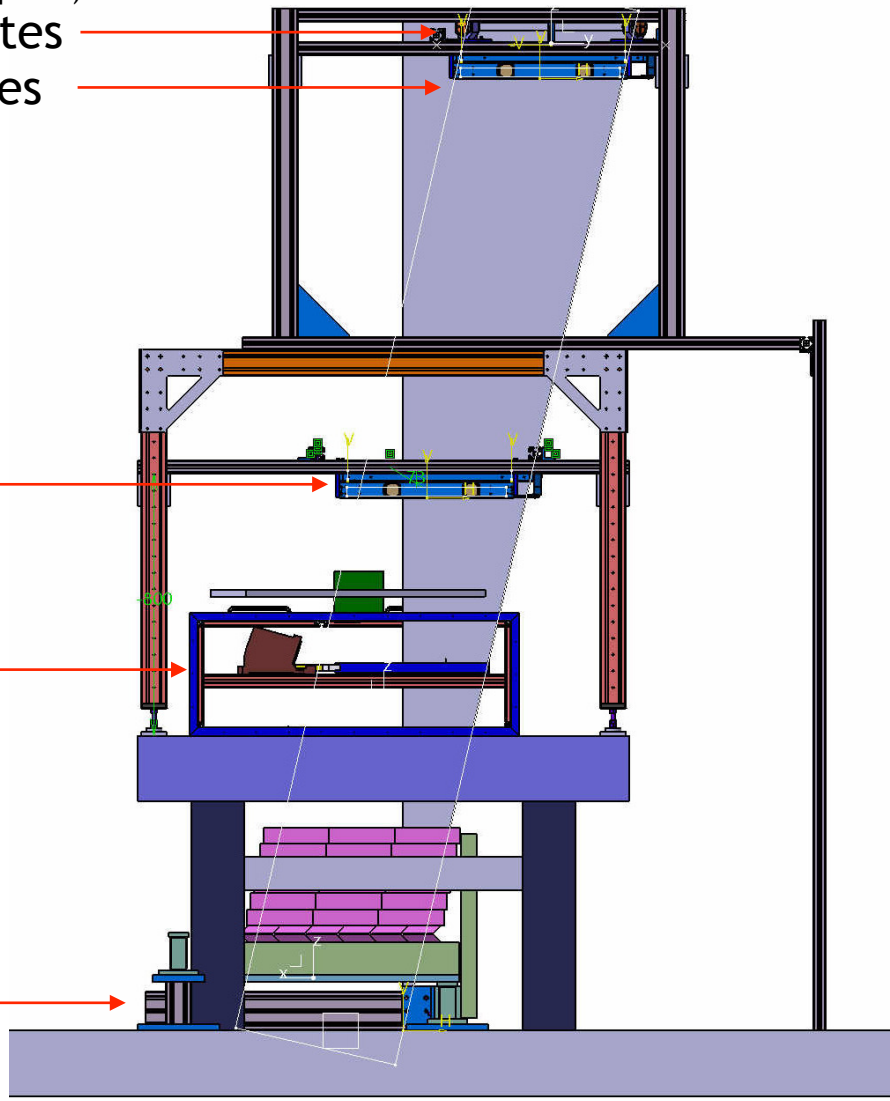
After quality test:

- FE-Boards will be tested in GCS with full radiator.

Radiator plate in full size



(Scintillator plate)
Trigger plates
Cosmic Boxes
(SiPM bars)



Thank you for your attention