

Controls Dry Run Planning

Regine Pfeil, *Hanno Hüther* 09.09.2019



- Since the last beam time, substantial enhancements have been implemented on all layers of the control system. Amongst others:
 - Timing Enigma release (saftlib 2.0, DM-UNILAC gateway refactoring, Data Master and WR-to-MIL gateway features for Storage Ring Mode)
 - New FPGA firmware (MIL DAQ, Watchdog, FG, MIL rescan)
 - New SCU Ramdisk (for SCU4 and Libera tests)
 - New FESA 3 7.0.0 release (CMW/RDA 3.0.1, saftlib 2.0, Timing Enigma)
 - Adapted FESA classes (FESA 3 7.0.0)
 - MASP (STABLE_BEAM, MASP GUI, monitored actuators)
 - Storage Ring Mode (BSS/Director, LSA, Model for ESR, Storage Ring Mode Expert App)



This is just an excerpt. See Dry Run Planning wiki page.

- In-depth testing of Storage Ring Mode
 - All features (Break Points, Manipulation, Repetition, Skipping)
 - Storage Ring Mode Expert Application
 - Correct behavior of (a subset) of ramped devices
- Beam transfer from ESR to CRYRING
 - Coupling, timing and trimming
- Function Generator enhancements
 - Preparation time reduced, stopping only affected Patterns during trim
- Devices to be added to LSA data supply
 - ESR Kicker & Timing Generator, timing controlled actuators, new CRYRING source, ...



- In general, Controls will only be able to perform depth tests (not breadth tests) due to time and resource contraints.
- In some areas, expert knowledge and/or operating experience might be necessary for testing.
- Additionally, help in organizational matters could free up resources for testing.



Some examples where help would be beneficial:

- Ensuring that all requested devices are available ("Freischaltungen schriftlich aufheben")
- Breadth tests covering a wide range of devices (basic functionality for all devices, but also checking that ramping in Storage Ring Mode works, etc.)
- Testing that Beam Modes work as expected (including MASP GUI, masking and monitored actuators)
- Testing timing-controlled actuators
- Testing ESR Timing Generator and kicker
- Verifying hardware interlock signals for SIS AEG