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Status Report

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FEE Development Lines at KVI

- Analogue circuits design for the FEE
  - PCB for the ASIC preamplifier
  - Design of dual-range shaper
- Feature-extraction algorithms (VHDL code) for SADC data processing
  - Precise energy (at low sampling rate)
  - Precise timing (at low sampling rate)
  - Simple algorithms for double pile-up correction
  - Effect of the limited trace length (application for the hit-detection ASIC)
- Trigger infrastructure
  - SODA time distribution system (Xilinx port)
  - Data transfer protocol?

Development Lines
(Shaper development)

Design of dual-range shaper:

- Aim: Find optimal shaping time (pulse shape!) to find an compromise between high-rate capability/triggering level/energy resolution
- Implementation:
  - Analogue vs. Digital

!Note:

- Dynamic range 10^4 → dual range shaper/splitter
- Proto60 (LAAPD, Basel preamplifier):
  Cosmic rays (28 MeV) → 4.8 mV (10 GeV → 1700 mV)

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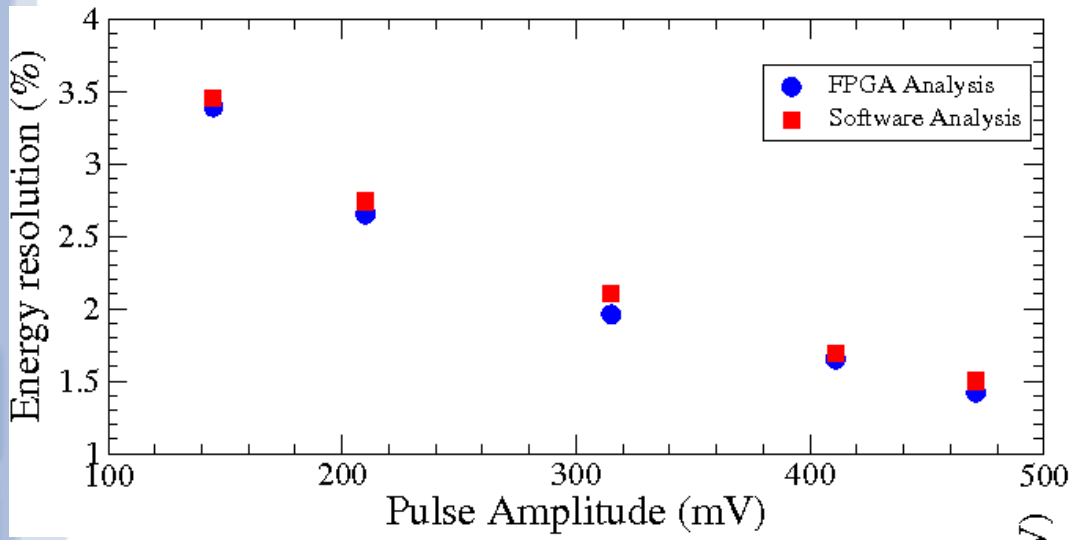
Feature-extraction

Implementation (VHDL)

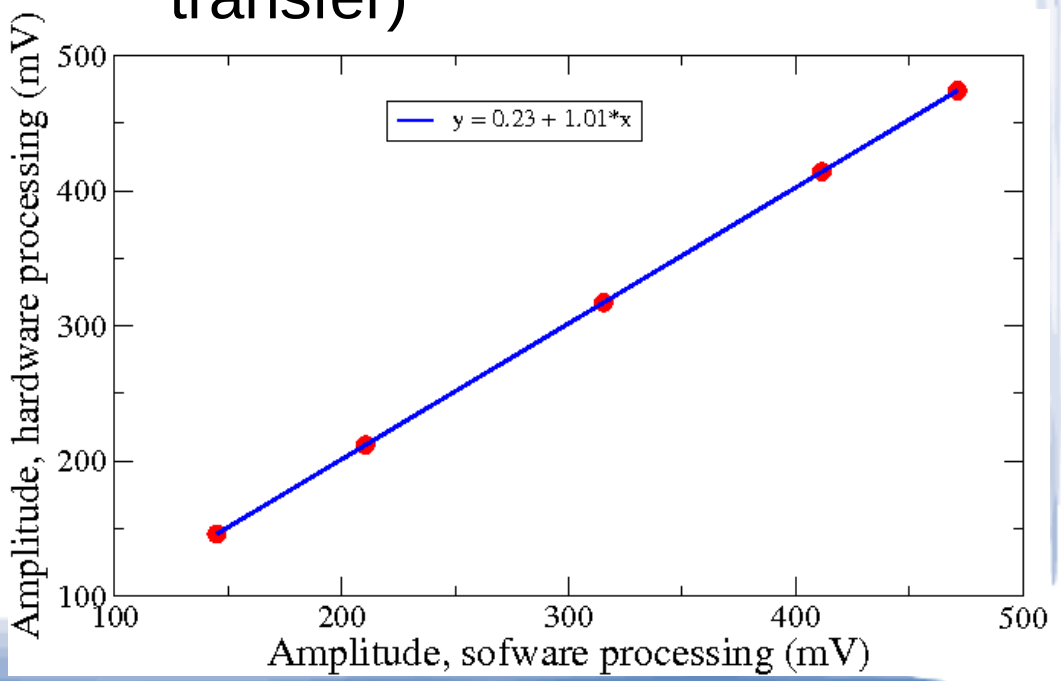
Algorithm development

Feature-Extraction
(VHDL implementation, ASIC pulse)

Energy



- Data taken with LED light-pulser
- Measurements done with 100 MHz 16 bit SADC
- Analysis performed in:
  - Software
  - Hardware (Xilins Spartan FPGA demo board, serial data transfer)



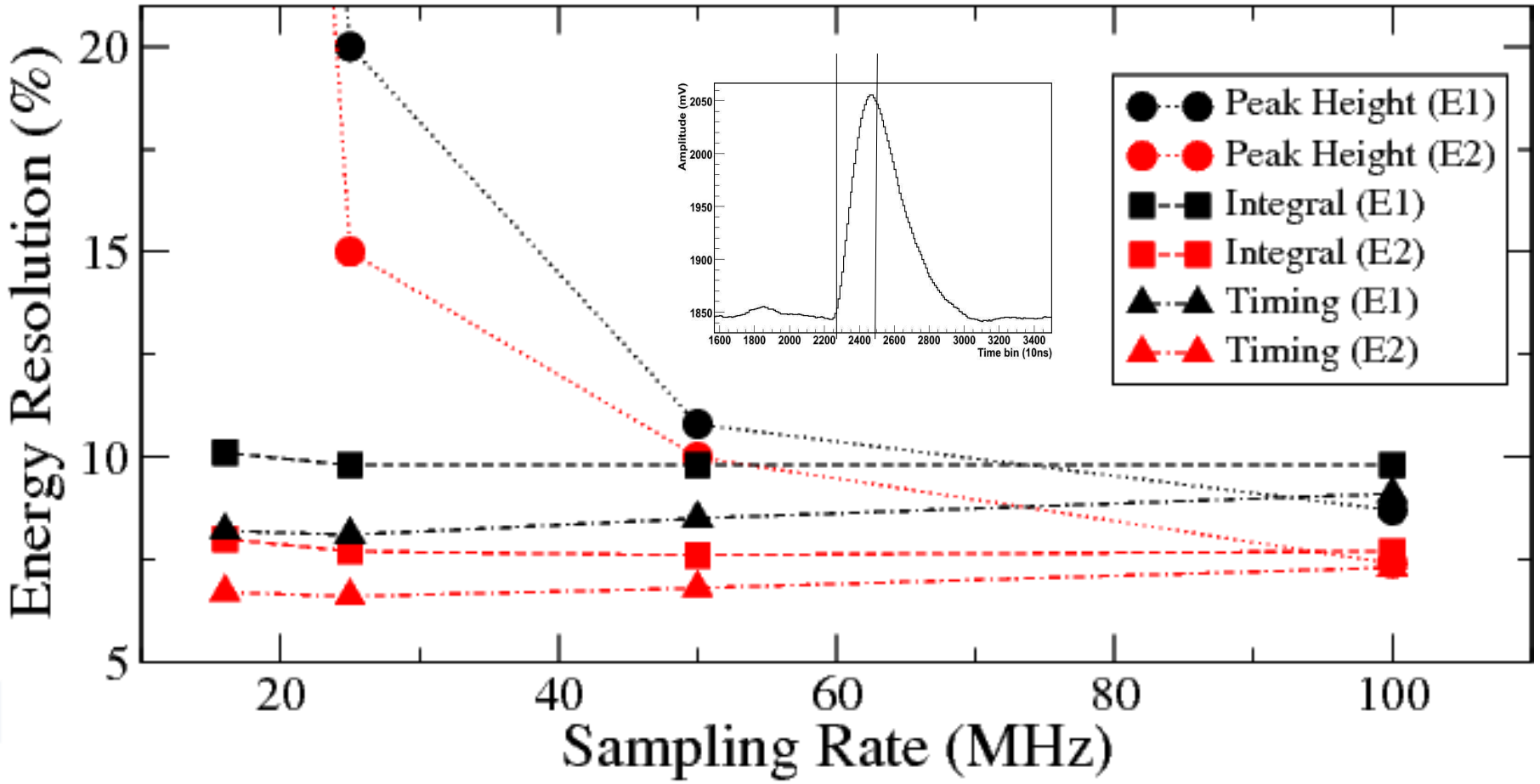
The VHDL implementation is working. Next steps:

- Test timing
- Port to existing SADC (FEBEX?)

Feature-Extraction

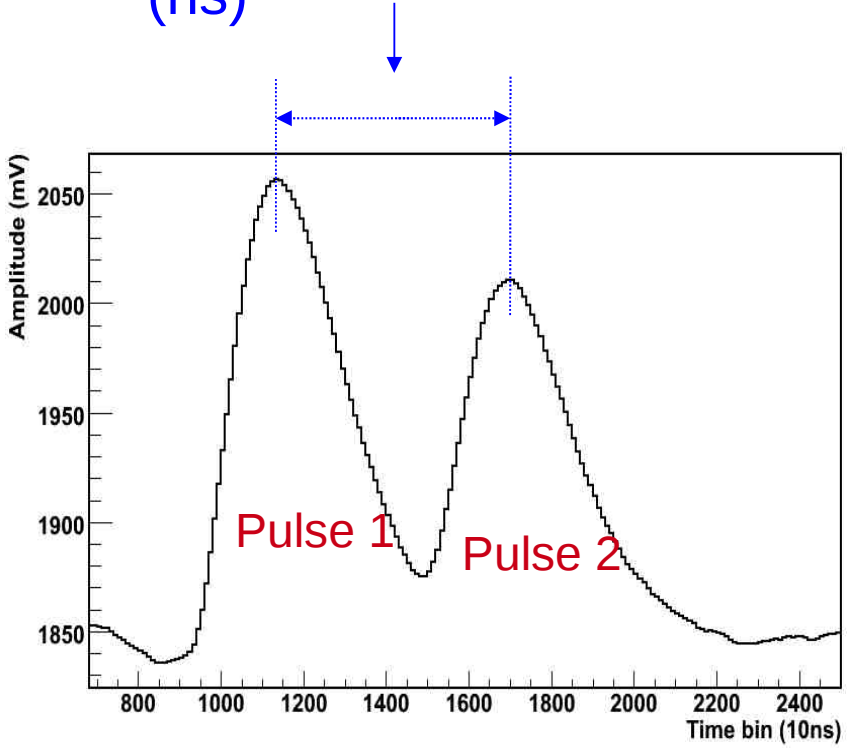
(Preparation for Pile-up recovery, Hit-Detection ASIC)

Extraction of the energy information from the digitized pulse:
(Energy resolution as a function of SADC sampling rate)



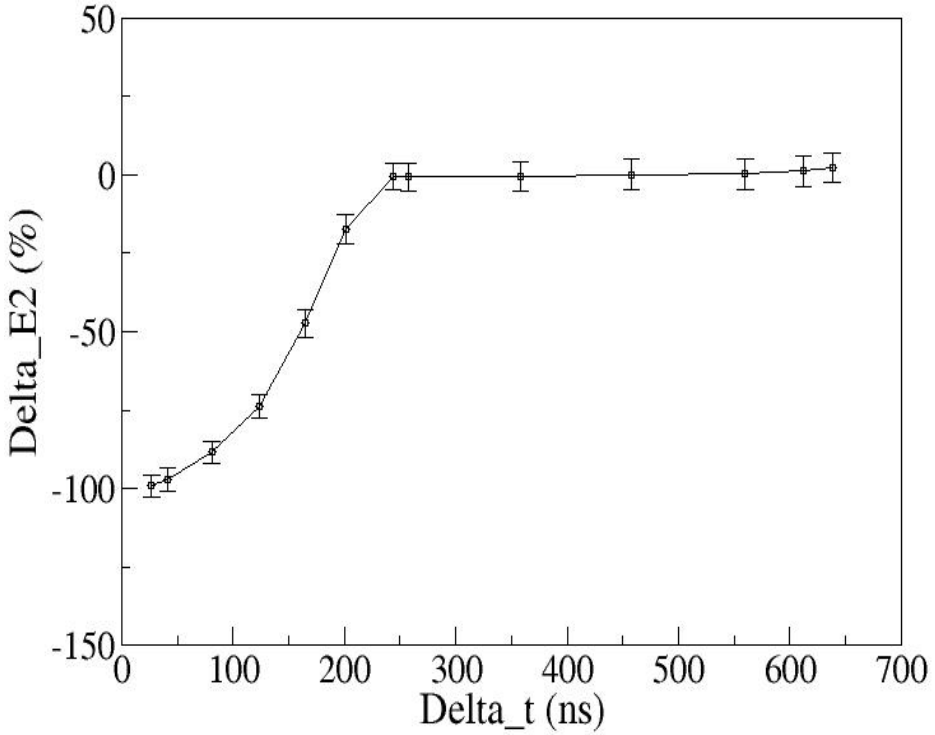
Feature-Extraction
(pile-up recovery)

Varying delay time: (ns) Delta_t



Pileup trace for Delta_t of 560ns

Recovered energy of the second pulse as a function of time distance



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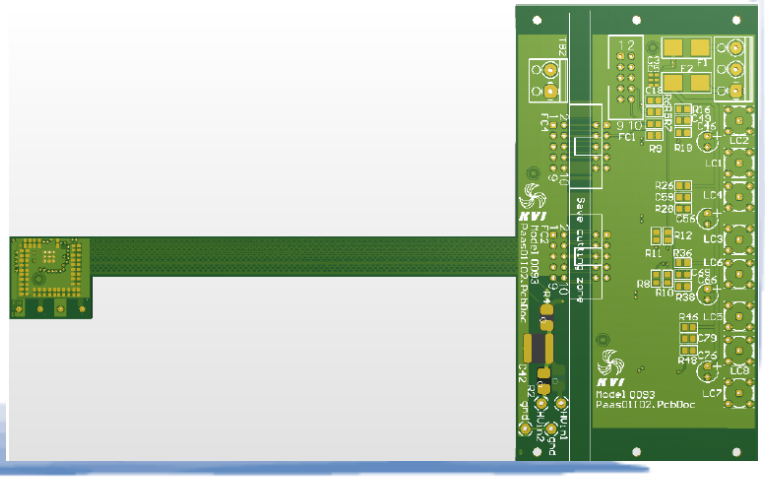
ASIC board

Status

Planing

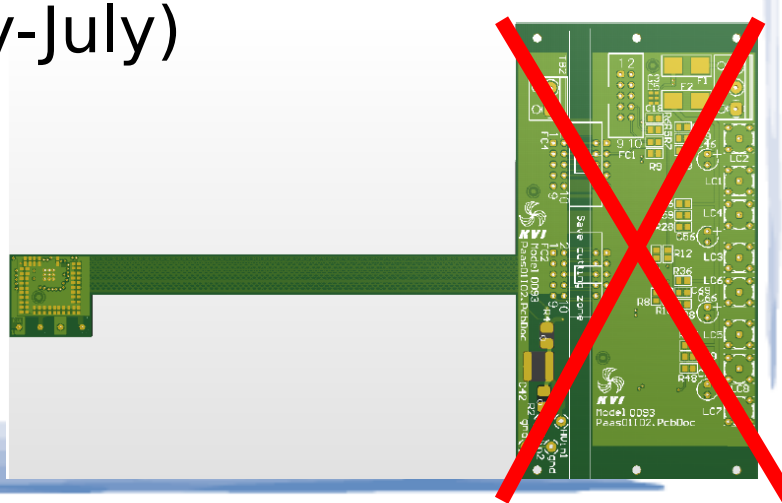
ASIC Board

- **Status:**
  - 10 boards were ordered
  - Expected delivery date – end of March
- **Planing:**
  - Test performance of the current APFEL ASIC with reasonably long Kapton cable (~100 mm)
  - Design of the additional line driver if needed
  - Investigate the effect of additional cable between the ASIC and line driver (in case ASIC can not drive long flat cable)



ASIC Board

- **Planing (after tests):**
  - Make final design
    - Without line driver – long (~40 cm) flex cable + connector for SADC
    - Without line driver – short (~10 cm) flex cable + connectors for twisted pair
    - With line driver
- **Time line:**
    - Tests of produced boards (May-July)
    - Redesign (August-October)
    - Production (end of 2010)



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Thank You!