

# **APFEL Development Status and Time Schedule**

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# Latest Submission

- ASIC design of 3rd iteration of APFEL finished
- First candidate for a final design
- Probably no further MPW runs until mass production
- Until end of January 8 requests for APFEL ASICs

Institute	Project	Number of ASICs
Uni Bochum	Proto 192	50
Uni Mainz	Backward Endcap	50
Uppsala		25
KVI	PCB Prototypes	20
Basel		3
Warsaw	Low Energy Measurements	4
GSI	ASIC Development	20
Uni München	Electron Tests	2
Summ		174

# Latest Submission

- Deadline for ASIC submission was on Feb. 8th
- 200 pieces have been ordered
  - so 26 pieces left, but we have no information about yield
- We expect silicon back beginning of may
- We are talking about untested and naked pieces of silicon
  - Test PCBs
  - Bonding

# Next Steps

- Test and specification of the APFEL ASIC
- If there are any critical bugs: We have to correct these bugs in a forth iteration
- If there are no critical bugs: We need a Design readiness review
- After review: engineering run
  - production of the complete mask set for mass production
  - production of 6 wafers, 2 wafers are assured to be in process specifications
  - ⇒5000 pieces of APFEL
- Setup of wafer test
- Mass production

# Schedule PreAmplifier APFEL

