

The HitDetection ASIC

A Customised IC for PANDA Readout

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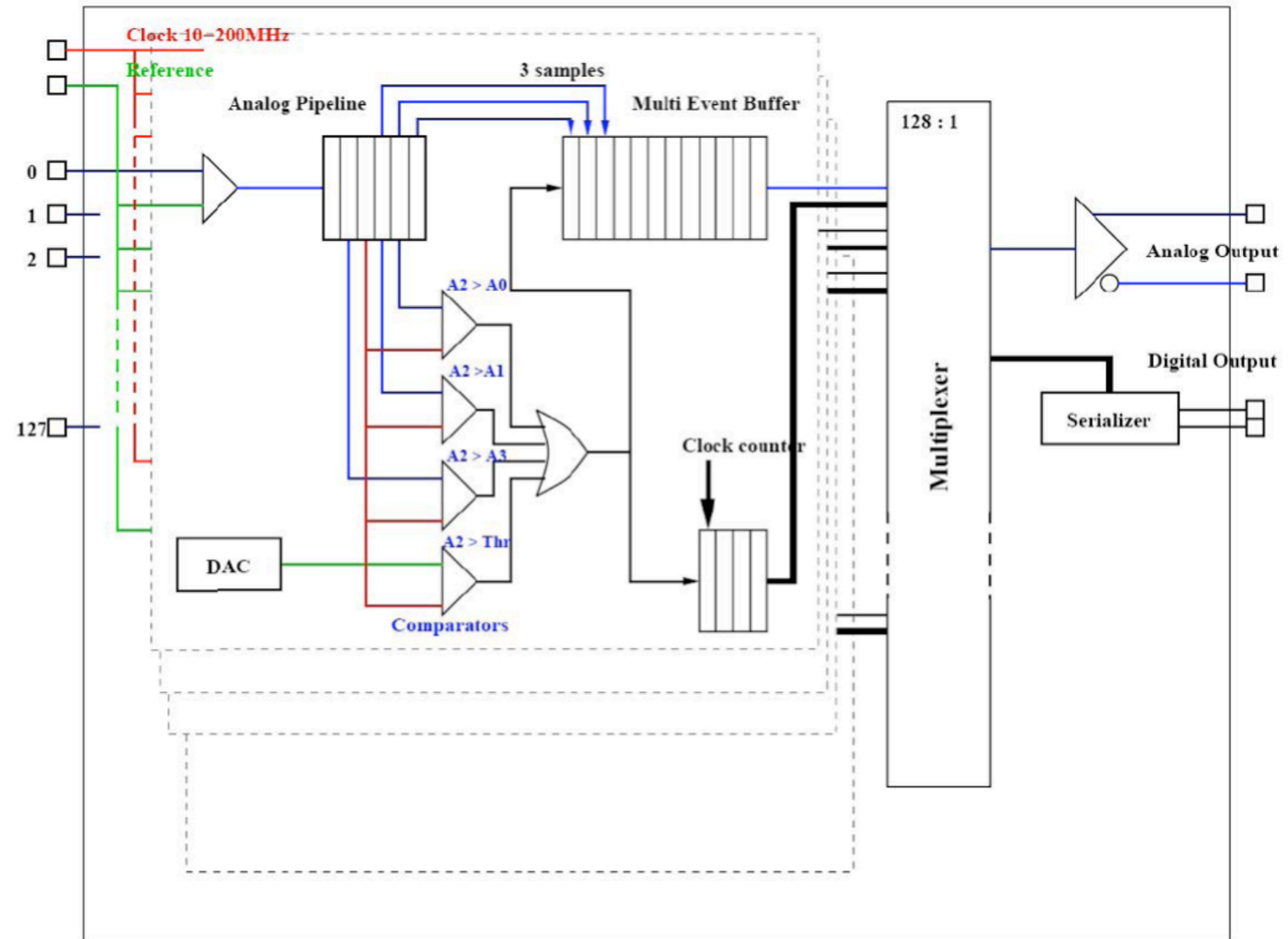
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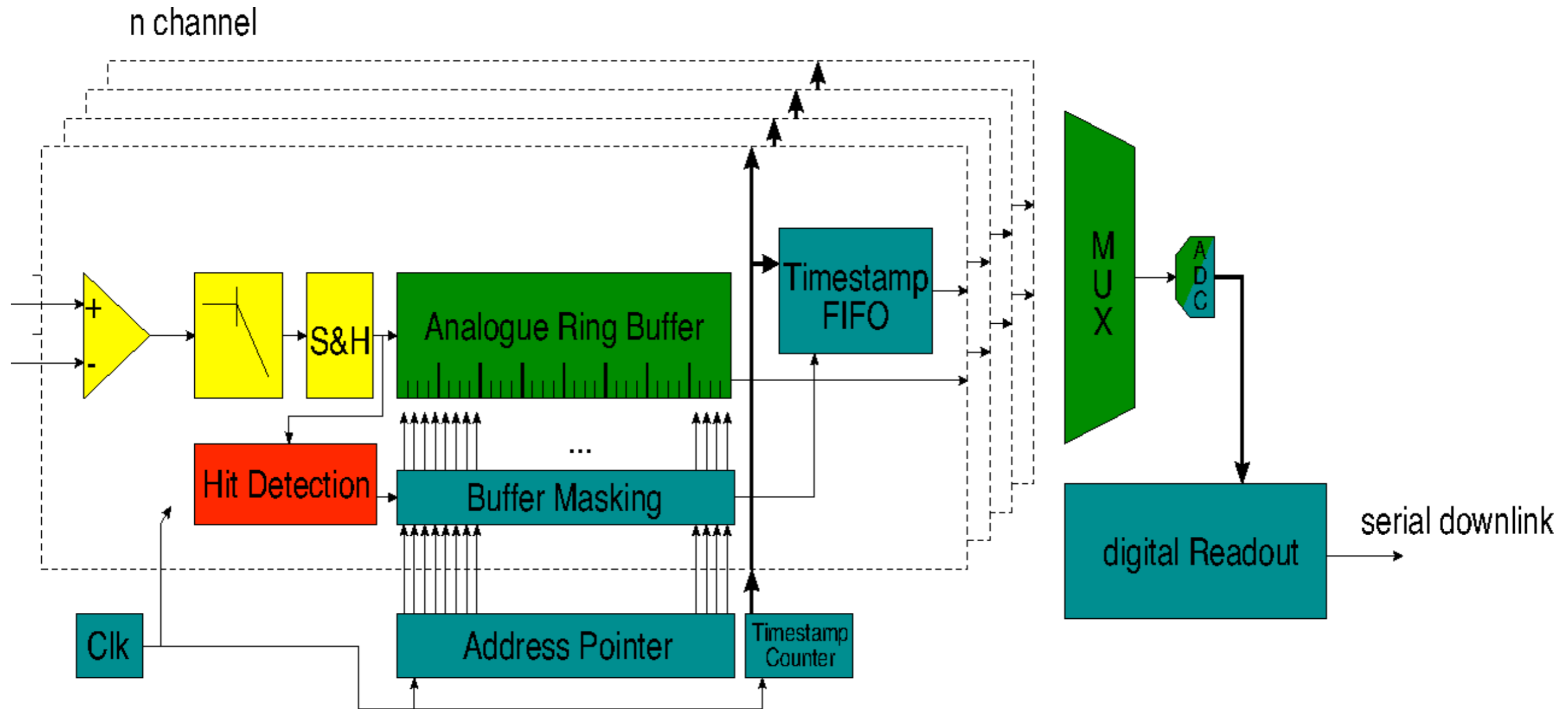
The First Idea

- First idea of this chip in a proposal of Igor Konorov from July 2007
- New initiative for a customised digitising IC for PANDA EMC end of 2009
- Different types of architectures have been discussed
- GSI ASIC design proposed to use the hit detection ASIC architecture



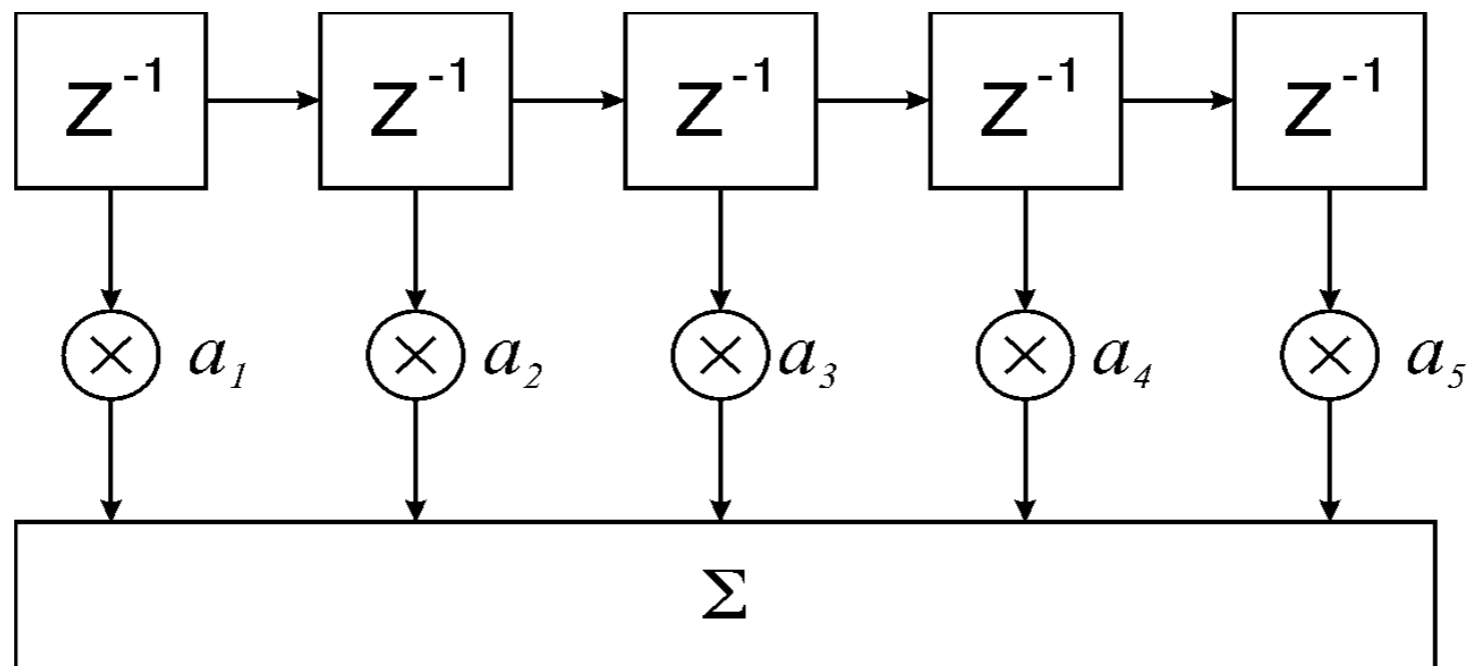
The Hit Detection ASIC Concept

- Self triggered transient recorder
- Configurable sampling rate and record length
- On chip ADC \Rightarrow digital readout



The Hit Detection Unit

- In the proposal of Igor: A FIR Filter (Finite Impulse Respond)
 - A continuous level, discrete time filter
- FIR filter should be able to detect hits in a pile up situation
- Drawback: Very complex circuit
 - Do we really need a FIR filter?
 - Order of this filter
 - Do we need free configurable filter coefficients or are fixed coefficients sufficient?



Integration Level

- Channel Pitch is given by bonding Pads
 - Differential Inputs \Rightarrow 2 Pads / Channel
 - With staggered input Pads \Rightarrow Channel Pitch = 100 μm

Number of channels	size	comments
32	3.2 mm	
64	6.4 mm	
128	12.8 mm	large chip may lead into yield problems / power

Open Questions



- Input specifications
 - Common mode range / dynamic range
 - Sample frequency
 - Anti aliasing filter needed?
- Transient records
 - How many samples are needed?
- Event rates?
- Radiation environment

Time Schedule (rough estimation)



- Hit detection core development:
 - 2010 : First Testchip with analogue buffer teststructures with fast write and slow readout
 - 2011 : Second Testchip with improved components from first testchip
 - 2012 : First prototype?
- ADC development in parallel
 - There is interest from PI Heidelberg to participate at this part