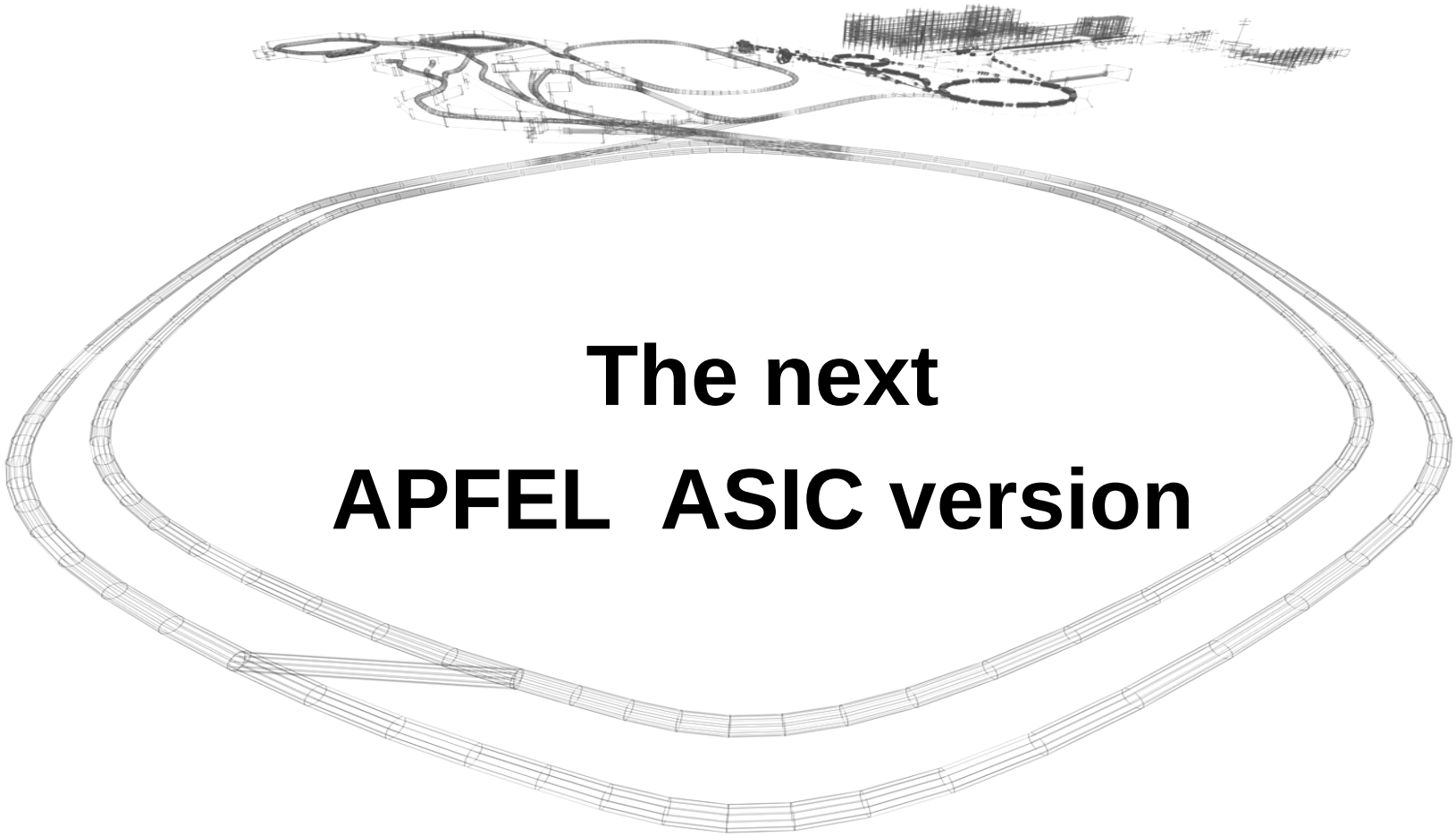
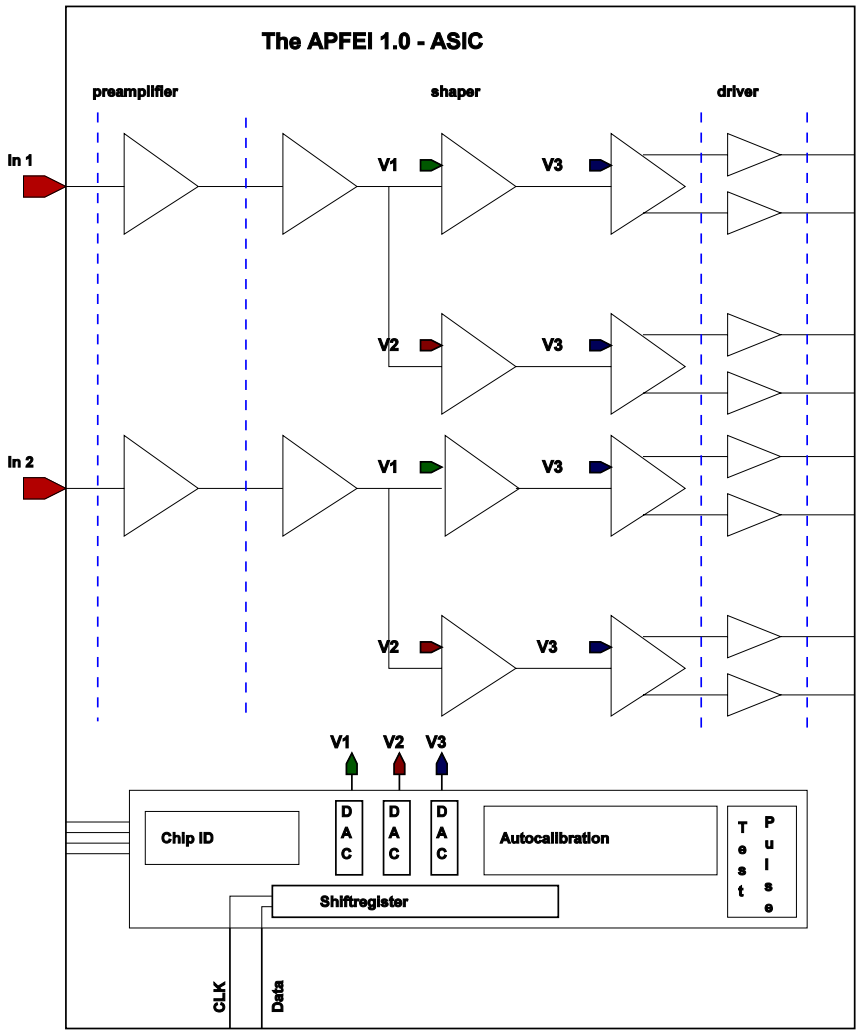


The next
APFEL ASIC version

Overview

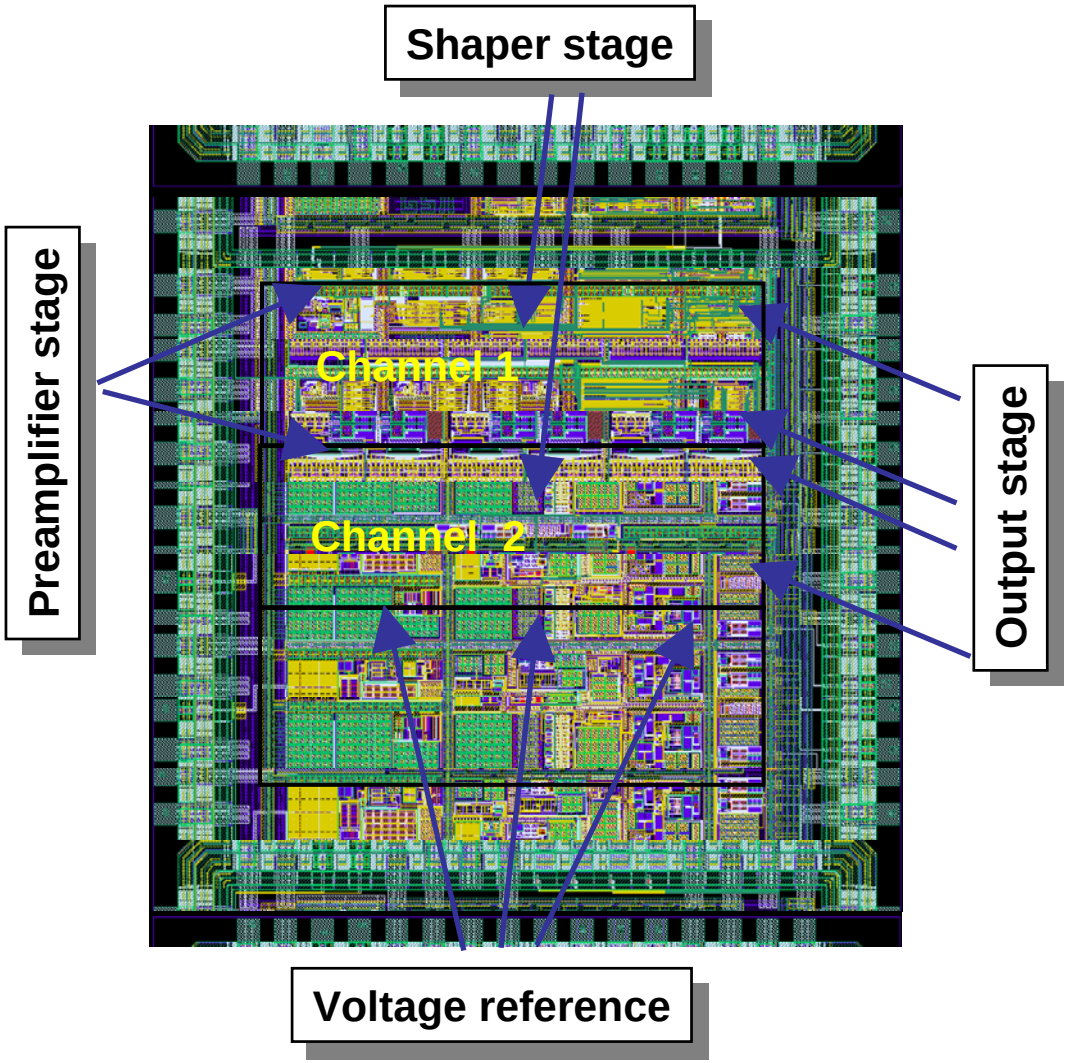
1. **The APFEL – ASIC**
   - **APFEL Design 2010**
   - **Layout Overview**
   - **Simulation Results**
   - **Outlook**

Chip overview



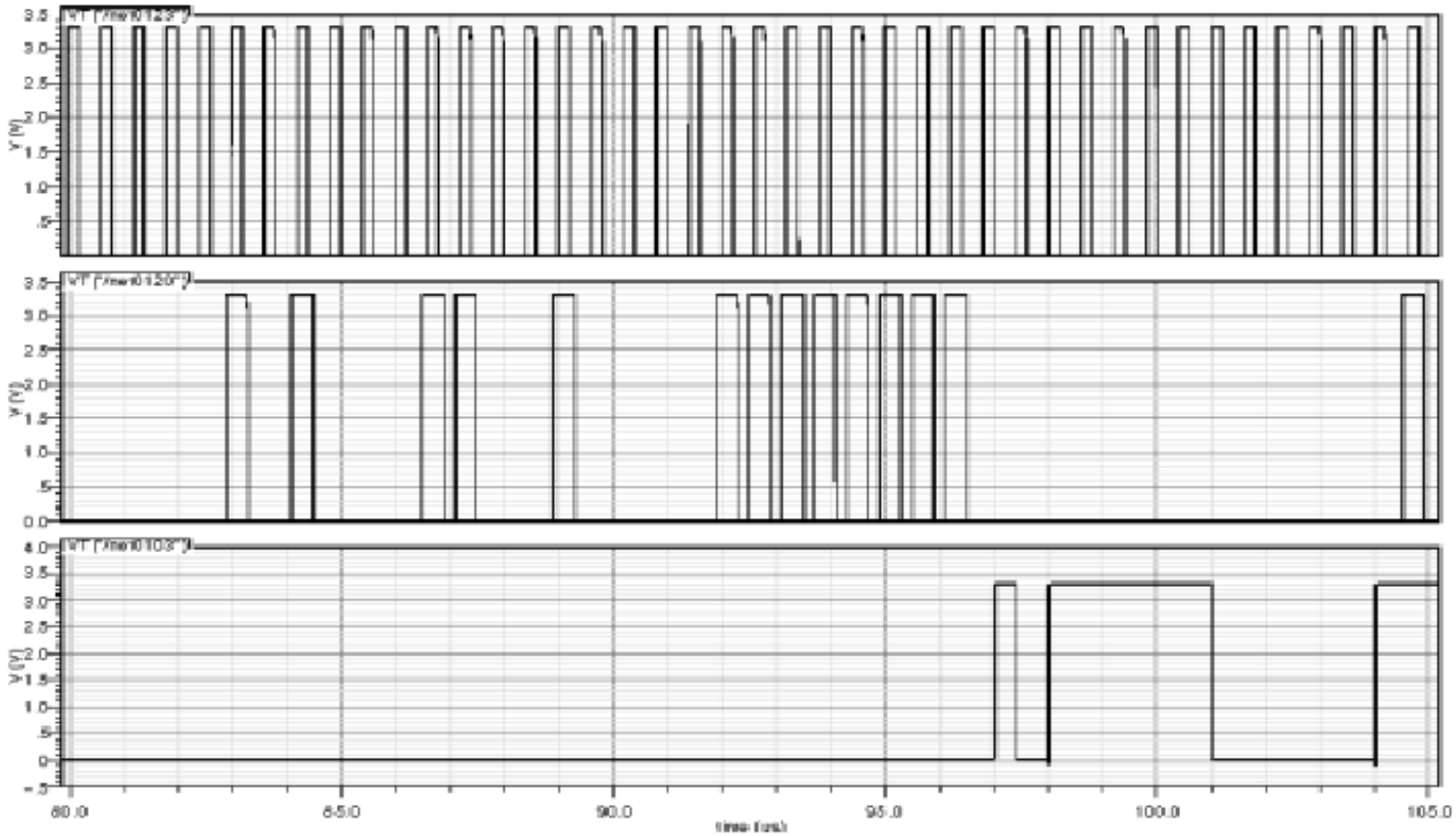
- Two equivalent readout channels
- Serial interface for:
  - programmable voltage references
  - test pulse generation
  - autocalibration
  - data readout
- 4 bit chip ID and DAC is implemented

New APFEL Layout



- Process: 350 nm – CMOS (AMS)
- Dimensions: 3.4 mm x 3.3 mm
- Pad connections: 64

Data Output

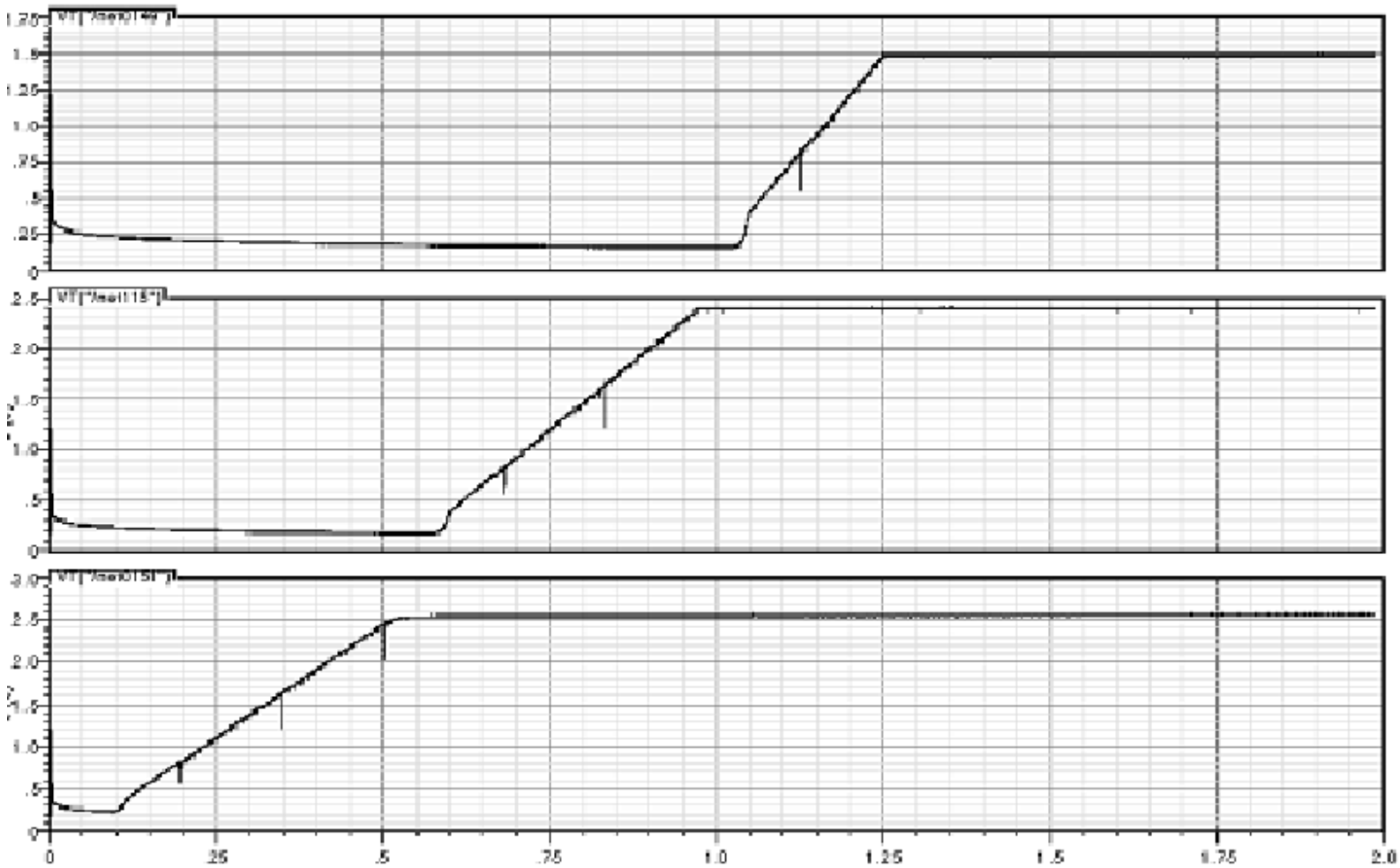


CLK

Data in

Data out from ASIC

Autocalibration



Voltage
DAC1

Voltage
DAC2

Voltage
DAC2

Overview

- **Date of submission: 08.02.2010**
- **3 wafers (200 Chips) have been ordered**
- **Delivery date of ASICs: spring 2010 (Mai)**
- **Next step: development of a test PCB**