PANDA DAQT and FrontEnd Electronics Workshop, Rauischholzhausen Castle

Reporte der Beiträge

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Beitrag ID: **0** Typ: **nicht angegeben**

MVD silicon pixel detector readout architecture and ASIC developments

Mittwoch, 14. April 2010 14:30 (30 Minuten)

The MVD silicon pixel detector readout architecture will be described. Special emphasis will be put on the full custom ASIC development for the front-end electronic.

Autor: Herr MAZZA, Giovanni (INFN Sez. Torino)

Vortragende(r): Herr MAZZA, Giovanni (INFN Sez. Torino)

Sitzung Einordnung: FEE Development

Track Klassifizierung: Front End Electronics

Beitrag ID: **1** Typ: **nicht angegeben**

A Reconfigurable Design Framework for FPGA Adaptive Computing

Freitag, 16. April 2010 11:00 (30 Minuten)

Partial Reconfiguration (PR) offers the possibility to adaptively change part of the FPGA design without stopping the remaining system. Based on PR technology, we present a comprehensive framework for adaptive computing, in which design key points of hardware processes, system interconnections, Operating Systems (OS), device drivers, scheduler software as well as context switching are respectively concerned in different hardware/software layers. Technical perspectives are analyzed and it is foreseen to obtain great benefits with the proposed design framework for DAQ and triggering in nuclear and particle physics experiments.

Autor: Herr LIU, Ming (II. Physik Institut, Uni-Giessen)

Vortragende(r): Herr LIU, Ming (II. Physik Institut, Uni-Giessen)

Sitzung Einordnung: Algorithms

Track Klassifizierung: Trigger

Beitrag ID: **2** Typ: **nicht angegeben**

Development of PANDA EMC Online High Level Trigger Algorithms

Freitag, 16. April 2010 09:00 (30 Minuten)

The PANDA detector is a general purposed hadron spectrum planed to operate at the FAIR facility in Darmstadt, Germany. The PANDA EMC detector provides almost 4pi spatial coverage, good granularity and high energy resolution. A novel self-trigger data push data architecture for the PANDA data acquisition system requiring the data from EMC readout electronics to be processed on the fly to reconstruct electromagnetic shower. Features extracted from the electromagnetic shower combines with information from other detectors such as tracking and Cherenkov detectors in order to discriminate between photons, electron and hadrons. An EMC trigger and data acquisition scheme is proposed employing an FPGA based Compute Node (CN). The CN provides flexible connection with high bandwidth between processing modules, up to 10GByte DDR2 memory per board for data buffering and five high end FPGAs for sophisticated algorithm applications. A cluster finding algorithm is presented. The cluster finder also searches bumps in one cluster and distinguishes overlapped clusters which is essential for $\pi 0$ reconstruction in high momentum and high luminosity experiments. Its energy and spatial resolution is measured. The cluster finding efficiency is studied based on simulation data. Some electromagnetic shower feature extraction algorithms which are usually done in offline trigger and their computing power requirements for FPGA implementation are discussed. The algorithms partition strategy, based on the readout electronics layout and the Compute Node based processing architecture, is also coved in the last part.

Autor: Herr WANG, Qiang (II. Physikalisches Insitut,JLU Gießen)

Vortragende(r): Herr WANG, Qiang (II. Physikalisches Insitut,JLU Gießen)

Sitzung Einordnung: Algorithms

Track Klassifizierung: Algorithms

Beitrag ID: **3** Typ: **nicht angegeben**

A FPGA helix tracking algorithm for PANDA

Freitag, 16. April 2010 09:30 (30 Minuten)

An online track finder for the PANDA experiment at the future FAIR facility was developed and tested.

The central Panda tracking detectors for charged particles will consist of a silicon based micro vertex detector (MVD, 5-7 hits/track) and possibly of a straw tube tracker (STT, 15 double layers of straws). Due to the solenoidal magnetic field, tracks of charged particles can be parametrized by a helix (if neglecting energy loss).

The algorithm works in several steps. Perpendicular to the beam direction the projection of the tracks is equivalent to a circle. Thus, first a conformal transformation will be used to convert the circles to straight lines. Second, a Hough transform is used to find the straight lines by a peak finding algorithm. Along the beam direction, a different Hough transformation is used. A peak finder returns all needed parameters to describe the helix track.

As the algorithm was developed for an FPGA, it uses lookup tables. Results with simulations will be presented. Possible FPGA implementation will be discussed.

Autor: MÜNCHOW, David (II. Physikalisches Institut, Universität Gießen)

Co-Autoren: Dr. SPRUCK, Björn (II. Physikalisches Institut, Universität Gießen); Dr. LANGE, Jens Sören (II. Physikalisches Institut, Universität Gießen); GALUSKA, Martin (II. Physikalisches Institut, Universität Gießen); LIU, Ming (II. Physikalisches Institut, Universität Gießen); GESSLER, Thomas (II. Physikalisches Institut, Universität Gießen); Prof. KÜHN, Wolfgang (II. Physikalisches Institut, Universität Gießen); Dr. LIANG, Yutie (II. Physikalisches Institut, Universität Gießen)

Vortragende(r): MÜNCHOW, David (II. Physikalisches Institut, Universität Gießen)

Sitzung Einordnung: Algorithms

Track Klassifizierung: Algorithms

Beitrag ID: **4** Typ: **nicht angegeben**

Status of the forward shashlyk readout

Mittwoch, 14. April 2010 15:00 (30 Minuten)

Report on the IHEP Protvino group forward shashlyk readout electronics activity: photodetector selection, monitoring system test, PMT HV control.

Autor: Dr. SEMENOV, Pavel (IHEP Protvino)

Vortragende(r): Dr. SEMENOV, Pavel (IHEP Protvino)

Sitzung Einordnung: FEE Development

Track Klassifizierung: Front End Electronics

Beitrag ID: **5** Typ: **nicht angegeben**

Thoughts on analysing photon hit patterns from Disc DIRC detectors

Freitag, 16. April 2010 10:00 (30 Minuten)

DIRC detectors in the PANDA experiment will give a high photon hit rate. Be it the current algorithms or new ones, they need to be adapted to run on the FFE systems and optimised for speed. And as the mechanical designs are not yet frozen, some minor changes that do not affect the detector performance may significantly ease the burden on the compute nodes.

Autor: Dr. FÖHL, Klaus (Universität Gießen)

Vortragende(r): Dr. FÖHL, Klaus (Universität Gießen)

Sitzung Einordnung: Algorithms

Beitrag ID: **6** Typ: **nicht angegeben**

Feature-extraction algorithms for the EMC

Mittwoch, 14. April 2010 17:00 (30 Minuten)

The feature-extraction algorithms for the EMC will be presented. During the presentation I will discuss digital filtering used for the signal processing, which resolution can be achieved by the EMC and what the resolution degradation at high rates.

Autor: Dr. KAVATSYUK, Myroslav (KVI, University of Groningen)

Vortragende(r): Dr. KAVATSYUK, Myroslav (KVI, University of Groningen)

Sitzung Einordnung: FEE Development

Beitrag ID: **7** Typ: **nicht angegeben**

High-Resolution 32 Channel TDC (< 10 ps RMS) Implemented in a FPGA.

Donnerstag, 15. April 2010 09:00 (30 Minuten)

Time to Digital Converters (TDCs) are widely used in many scientific applications. At GSI high-resolution ASIC-TDCs and commercial modules will be utilized in Time-of-Flight detectors for the upcoming FAIR experiments. The time-stretching methods used in high-resolution applications, e.g. the Vernier and the tapped delay lines (TDL) method, have also been successfully implemented in FPGA-Technology. The best recently known implementation achieves a RMS of 10 picoseconds (ps) with a reduced number of channels and an increased dead time in an Altera-FPGA.
The advantage of a FPGA implementation is the less expensive and less time consuming design process as well as the flexibility and adaptability of the FPGA-TDC design to special needs of the current application. These facts motivated us to explore the achievable performance of a TDC implementation in a FPGA.
We implemented a 32-channel, low dead time TDC based on the TDL method in a Virtex-4 FPGA. In this method standard chain structures in a FPGA –the carry chains –are used as a delay chain for time stretching purposes. The achievable time-resolution of the interpolation is determined by the intrinsic delay of a cell in the chain. In our implementation we used special techniques to improve the time resolution of the TDC beyond its cell delay.
The TDC was tested by measuring the time between rising edges of the original and the delayed signal on different TDC channels. We measured delays in the range from 40 ps to 1 us. At small delays 9 ps RMS was achieved, additional 2 ps were induced by the limited accuracy of the system clock at 1 us delay. Thus the achieved resolution of a TDC channel is 6 ps ($9/\sqrt{2}$).
Additional measurements were performed to characterize the influence of the temperature and supply voltage variations on the measured RMS value. The results of these measurements and the architecture of the FPGA-TDC will be presented.

Autor: BAYER, Eugen (Johann Wolfgang Goethe - Universität)

Co-Autor: Dr. TRAXLER, Michael (GSI)

Vortragende(r): BAYER, Eugen (Johann Wolfgang Goethe - Universität)

Sitzung Einordnung: FEE Development II

Track Klassifizierung: Front End Electronics

Beitrag ID: **8** Typ: **nicht angegeben**

PWO Crystal Matrix Measurements @ GSI

Mittwoch, 14. April 2010 15:30 (30 Minuten)

Presentation of the first PWO matrix measurements with ASIC readout.

Autor: Dr. WIECZOREK, Peter (GSI)

Vortragende(r): Dr. WIECZOREK, Peter (GSI)

Sitzung Einordnung: FEE Development

Track Klassifizierung: Front End Electronics

Beitrag ID: **9** Typ: **nicht angegeben**

Status Report of the GET4 TDC

Donnerstag, 15. April 2010 09:30 (30 Minuten)

This talk will give a brief information concerning the status of the GET4 TDC developement.

Autor: Herr DEPPE, Harald (GSI Darmstadt)

Vortragende(r): Herr DEPPE, Harald (GSI Darmstadt)

Sitzung Einordnung: FEE Development II

Track Klassifizierung: Front End Electronics

Beitrag ID: **10** Typ: **nicht angegeben**

Summary of the March 29th/30th Orsay meeting on PANDA EMC electronics

Mittwoch, 14. April 2010 16:30 (30 Minuten)

A summary of the Orsay meeting on the PANDA EMC electronics will be presented. We will go through the VFE implemented in the cold part and discuss the outlines of the digitization and concentration, the so-called "Multiplexing stage". We will try to give some ideas about the integration of this electronics within the Calorimeter Barrel. We will briefly present the prototypes under development and their associated tests. At the end, we will try to summarize the most relevant pending questions.

Autor: Dr. CHAMBERT, Valerie (Institut de Physique Nucleaire Orsay)

Vortragende(r): Dr. CHAMBERT, Valerie (Institut de Physique Nucleaire Orsay)

Sitzung Einordnung: FEE Development

Track Klassifizierung: Front End Electronics

Beitrag ID: **11** Typ: **nicht angegeben**

Gigabit Ethernet implementation on Lattice FPGAs

Freitag, 16. April 2010 16:30 (30 Minuten)

Implementation of Gigabit Ethernet on TRB Addon boards is a cheap and efficient way to transport large amount of data from front-end electronics to event builders, and is a solution already used and being tested in HADES experiment in GSI, Darmstadt. The process of gathering data, constructing packets and finally transport them will be covered by my presentation.

Autor: Herr KORCYL, Grzegorz (Jagiellonian University)

Vortragende(r): Herr KORCYL, Grzegorz (Jagiellonian University)

Sitzung Einordnung: Trigger and Data Acquisition II

Track Klassifizierung: Data Acquisition

Beitrag ID: **12** Typ: **nicht angegeben**

96-channel 10-bit 50 MSPS ADC board with Gb output

Donnerstag, 15. April 2010 10:00 (30 Minuten)

96-channel ADC board based on 10-bit 50 MSPS AD9212 chip will be presented. The board is one of the "AddOn" series for the TRB board and is used to collect data from the Shower detector at HADES experiment. The board provides Gb Ethernet output and can export data using UDP datagrams.

Autor: Dr. KORCYL, Krzysztof (IFJ PAN)

Vortragende(r): Dr. KORCYL, Krzysztof (IFJ PAN)

Sitzung Einordnung: FEE Development II

Track Klassifizierung: Front End Electronics

Beitrag ID: **13** Typ: **nicht angegeben**

A Digital Trigger for the Electromagnetic Calorimeter at the COMPASS Experiment

Freitag, 16. April 2010 17:00 (30 Minuten)

The COMPASS experiment at CERN-SPS performed during the 2009 run a measurement of the Primakoff effect. This effect is characterized by high energetic photons in forward direction, which due to a very small angle respectively to the incident beam direction hit only the Electromagnetic Calorimeter in the second spectrometer stage(ECAL2). In order to efficiently detect those events the ECAL2 digital trigger system was developed. The trigger logic was integrated into the existing readout electronics, taking advantage of the flexible FPGA based sampling ADC modules, employed in the COMPASS experiment. The logic combined 512 calorimeter cells and calculated the total energy at every point of time on a bases of extracted signal amplitudes and temporal information. The single channel time resolution was measured to be in the order of 1 ns. The digital realization of the trigger logic allows to correct the time as well as the energy response of every calorimeter channel, and to monitor the system parameters. For the Primakoff run the trigger logic was configured to process 132 central calorimeter cells to identify events where the energy exceeds 50 GeV/c and 70 GeV/c. The 50GeV/c trigger was prescaled by a factor of 2 while all events with more than 70GeV/c were acquired. The total trigger rate was about 30 kHz.
In this talk the functionality of the system as well as the system performance during the Primakoff run in 2009 will be presented.

Autor: Herr HUBER, Stefan (TU Munich)

Vortragende(r): Herr HUBER, Stefan (TU Munich)

Sitzung Einordnung: Trigger and Data Acquisition II

Track Klassifizierung: Trigger

Beitrag ID: **14** Typ: **nicht angegeben**

The APFEL ASIC Project – Next Steps

Donnerstag, 15. April 2010 11:30 (30 Minuten)

In february the tape out of the third iteration of the APFEL preamplifier and shaper ASIC took place. From early summer 200 ASICs will be available for detector tests. So from the ASIC designers point of view the development is completed.
We now need to decide which tests have to be integrated into a design readyness review and how much time will be spend on these tests. After the design readyness review there are stil several upcoming steps including production, testing and assembly.
The talk will give an overview of the tests foreseen to be done by our group and the upcoming steps and its time requirements. In the end the project time schedule will be discussed.

Autor: Dr. FLEMMING, Holger (Gesellschaft für Schwerionenforschung)

Vortragende(r): Dr. FLEMMING, Holger (Gesellschaft für Schwerionenforschung)

Sitzung Einordnung: FEE Development II

Track Klassifizierung: Front End Electronics

Beitrag ID: **15** Typ: **nicht angegeben**

The HitDetection ASIC – A self triggered transient recorder

Donnerstag, 15. April 2010 11:00 (30 Minuten)

Up to now the digitisation part of the FEE and DAQ chain should be realised with COTS components. Espcially for the EMC readout where the digitisation unit has to be placed inside the magnet an application specific highly integrated solution would have some advatages.
In this talk the concept for the HitDetection ASIC will be presented. The HitDetection ASIC is a self triggered transient recoder and digitiser well fitted to the needs of the PANDA readout.

Autor: Dr. FLEMMING, Holger (Gesellschaft für Schwerionenforschung)

Vortragende(r): Dr. FLEMMING, Holger (Gesellschaft für Schwerionenforschung)

Sitzung Einordnung: FEE Development II

Track Klassifizierung: Front End Electronics

Beitrag ID: **16** Typ: **nicht angegeben**

Present Read Out Chain for the PANDA barrel DIRC

Mittwoch, 14. April 2010 17:30 (30 Minuten)

A protoype of the PANDAbarrel DIRC was tested wit a proton beam in September 2009. The readout of the 256 MCP-PMT channels were done with HADES Trigger Readout Boards (TRP) and NINO discriminator boards as addons. The results and experience from this beam times will be presented.

Autor: SCHWARZ, Carsten (GSI Helmholtzzentrum für Schwerionenforschung GmbH)

Vortragende(r): SCHWARZ, Carsten (GSI Helmholtzzentrum für Schwerionenforschung GmbH)

Sitzung Einordnung: FEE Development

Track Klassifizierung: Front End Electronics

Beitrag ID: **17** Typ: **nicht angegeben**

MicroTCA experiences and developments at Forschungszentrum Juelich

Donnerstag, 15. April 2010 14:30 (30 Minuten)

Because of the complexity and the high startup cost of ATCA, initial PANDA DAQ development activities in Forschungszentrum Juelich concentrate on MicroTCA. MicroTCA provides a smooth path to ATCA, since MicroTCA boards can be reused in ATCA shelves by means of AMC carriers and all essential technological challenges, e.g. Management and high speed serial communication links on the backplane, can be studied in MicroTCA systems, too.
As a starting point a multivendor system of crates, MCHs, CPUs and peripheral boards from several companies was set up in oder to establish a development platform and in order to investigate functionality and interoperability issues.
The talk presents first experiences with MicroTCA and reports on the status of the ongoing AMC module developments.

Autoren: Herr KLEINES, Harald (Forschungszentrum Juelich); Dr. DROCHNER, Matthias (Forschungszentrum Juelich)

Vortragende: Herr KLEINES, Harald (Forschungszentrum Juelich); Dr. DROCHNER, Matthias (Forschungszentrum Juelich)

Sitzung Einordnung: Trigger and Data Acquisition

Track Klassifizierung: Data Acquisition

Beitrag ID: **19** Typ: **nicht angegeben**

Standardization of PANDA serial links between front-end electronics and DAQ

Donnerstag, 15. April 2010 16:30 (30 Minuten)

Few options for implementation of serial links are presented. One option is based on FPGA built-in serial links and another one is a current CERN development of radiation hard serial link called GBT.
Proposal for PANDA serial link protocols is presented.

Autor: KONOROV, Igor (Technical University Munich)

Vortragende(r): KONOROV, Igor (Technical University Munich)

Sitzung Einordnung: Discussion Session

Track Klassifizierung: Front End Electronics

Beitrag ID: **20** Typ: **nicht angegeben**

An IPM Controller for the PANDA Compute Node

Donnerstag, 15. April 2010 15:00 (30 Minuten)

An ATCA telecommunication shelf provides power, cooling and high-speed interconnections to up to 14 PANDA Compute Nodes. A single Shelf Manager supervises the installed boards and regulates the power distribution and temperature inside the shelf. The Shelf Manager relies on a local controller on each Compute Node to relay sensor alerts, provide hardware information and power requirements etc. An IPM Controller based on an Atmel microcontroller was designed for this purpose, and a prototype was produced.

The neccessary firmware is being developed to allow local communication with the components of the Compute Node and remote communication with the Shelf Manager conform to the ATCA specification. An overview of the intended functions of the IPM Controller and a status report will be given.

Autor: Herr GESSLER, Thomas (II. Physikalisches Institut, JLU Giessen)

Vortragende(r): Herr GESSLER, Thomas (II. Physikalisches Institut, JLU Giessen)

Sitzung Einordnung: Trigger and Data Acquisition

Track Klassifizierung: Trigger

Beitrag ID: **21** Typ: **nicht angegeben**

Discussion Buffer

Mittwoch, 14. April 2010 18:30 (30 Minuten)

Sitzung Einordnung: FEE Development

Beitrag ID: **22** Typ: **nicht angegeben**

GPU's for event reconstruction

Freitag, 16. April 2010 11:30 (30 Minuten)

The use of graphics processor units (GPUs) for event reconstruction in FairRoot will be presented. CUDA (Nvidia's Compute Unified Device Architecture) development tools are in use for few months now. New features and technologies has arrived at the market from NVIDIA itself (pinned memory) and others companies (OpenCL). In this work, the use of some of these features, pro and contras will be presented.

Autor: Dr. AL TURANY, Mohammad (GSI)

Vortragende(r): Dr. AL TURANY, Mohammad (GSI)

Sitzung Einordnung: Algorithms

Track Klassifizierung: Trigger

Beitrag ID: **23** Typ: **nicht angegeben**

Discussion Session A

Topic A
Topic B

Beitrag ID: **24** Typ: **nicht angegeben**

Discussion Buffer

Freitag, 16. April 2010 12:00 (30 Minuten)

Sitzung Einordnung: Algorithms

Beitrag ID: **25** Typ: **nicht angegeben**

Discussion on Online Computing

Freitag, 16. April 2010 14:30 (1 Stunde)

Sitzung Einordnung: Algorithms

Beitrag ID: **26** Typ: **nicht angegeben**

Discussion buffer

Freitag, 16. April 2010 17:30 (1 Stunde)

Sitzung Einordnung: Trigger and Data Acquisition II

Beitrag ID: **27** Typ: **nicht angegeben**

PANDA STT - front-end electronics requirements for particle identification

Mittwoch, 14. April 2010 18:00 (30 Minuten)

The ongoing investigation of the particle identification using dE/dx method.
with STT setup together with resulting requirements for front-end electronics
will be presented..

Autor: KULESSA, Pawel

Vortragende(r): KULESSA, Pawel

Sitzung Einordnung: FEE Development

Track Klassifizierung: Front End Electronics

Beitrag ID: **28** Typ: **nicht angegeben**

AMC Based Upgrade of the Compute Node

Donnerstag, 15. April 2010 15:30 (30 Minuten)

Vortragende(r): Dr. XU, Hao (IHEP,Beijing)

Sitzung Einordnung: Trigger and Data Acquisition

Beitrag ID: **29** Typ: **nicht angegeben**

Discussion on Detector Rates

Donnerstag, 15. April 2010 17:00 (1 Stunde)

Sitzung Einordnung: Discussion Session

Beitrag ID: **30** Typ: **nicht angegeben**

Discussion on event timing

Donnerstag, 15. April 2010 18:00 (1 Stunde)

Sitzung Einordnung: Discussion Session