The APFEL ASIC Project
Next Steps

Holger Flemming, GSI, EE-ASIC

Where we are

- Development since 2005 with three prototype iterations
- 2nd iteration already fullfills the given requirements for the preamplifier and shaper
- 3rd iteration with identical analouge part
  - 200 ASICs available for detector tests
  - delivery on April 7th

Comparison of 2nd and 3rd Iteration

2nd Iteration	3rd Iteration
Well specified analouge part fulfils all known requirements	No changes in analogue part; identical layout
High and low gain output are not usable simultaniously due to mismatch in DC-Level	Additional reference voltage generated by a third DAC to adjust DC levels of both outputs independantly
Some experience needed to find correct DAC settings	Autocalibration
	Digital readout of DAC settings
3.3 x 3.3 mm^2, 64 Bondpads	3.3 x 3.4 mm^2, 64 Bondpads Pinout differs from 2nd Iteration !

APFEL Test Status

- 2nd Iteration
  - Lab-measurements:
    - Noise (as function of temperatur and detector capacitance)
    - Power consumption (as function of temperatur and hit rate)
    - Shaping time
    - Dynamic range
    - ...
  - Tests at KVI
    - Time resolution
  - Matrix of 16 crystals with sampling ADC readout
    - Successful cosmic test at -20°C
    - Testsetup available for beam tests
  - 10 ASICs at KVI for test with the PC board prototype
- 3rd Iteration: Just delivered...

APFEL - 3rd Iteration

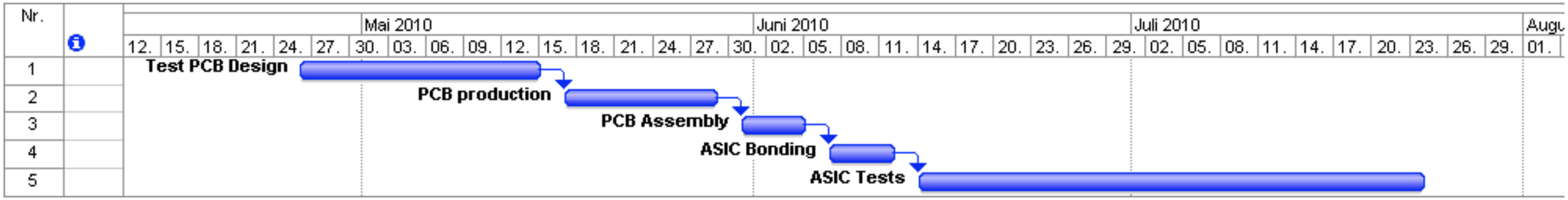
- APFEL Order:

Insitute	Project	Number of ASICs
Uni Bochum	Proto 192	50
Uni Mainz	Backward Endcap	50
Uppsala		25
KVI	PCB Prototypes	20
Basel		3
Warsaw	Low Energy Measurements	4
GSI	ASIC Development	20
Uni München	Electronic Tests	2
Summ		174

APFEL - 3rd Iteration

- Support from GSI ASIC-Design
  - Documentation
  - Packaging (only for few pieces (< 5))
  - PCB development
    - Design rules for PCB footprint
    - Coating specification for bond process
    - If applicable design of a common use test PCB

The Next Steps



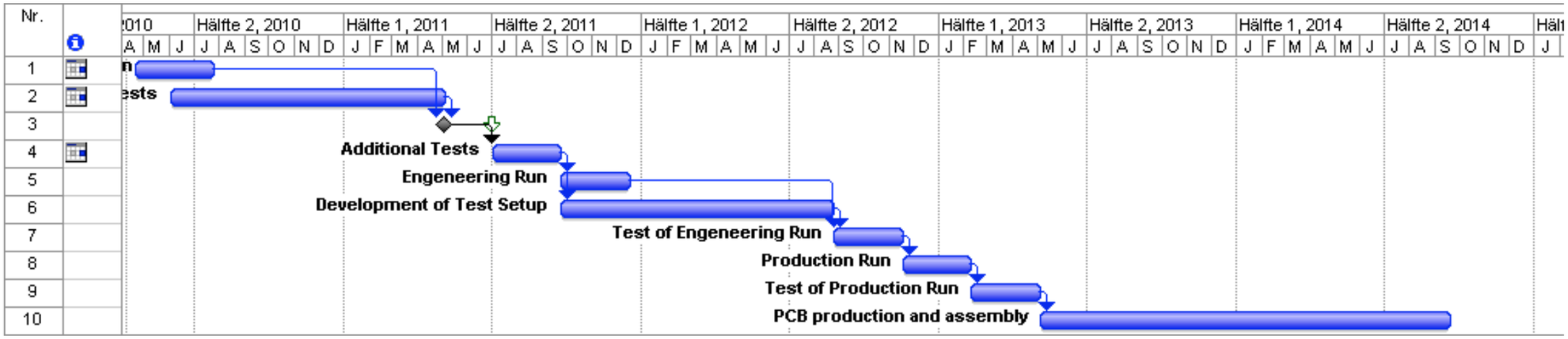
- 3rd iteration has to be tested and specified

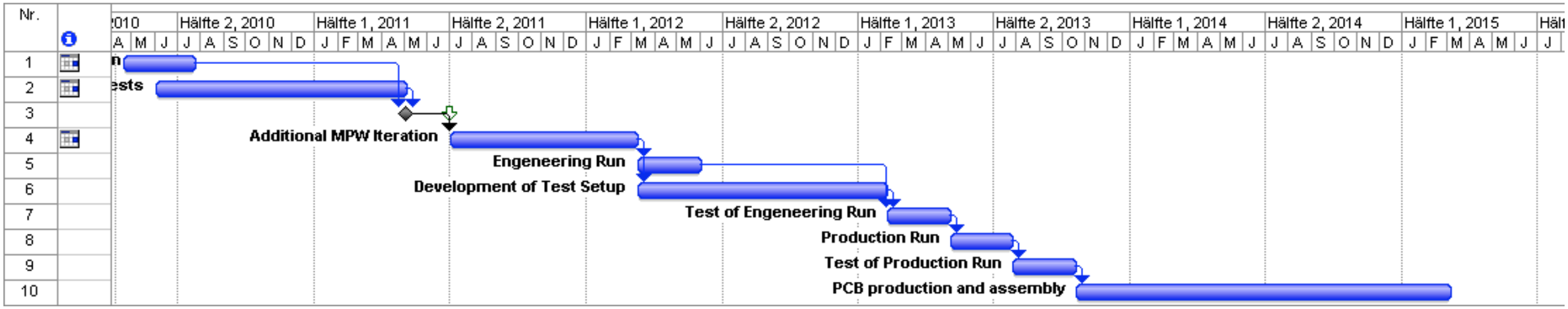
- Time estimation:

  - First test results in June

  - Complete ASIC specification end of July

Schedule for Production





- Design readyness review midyear 2011
  - more than 12 months for detector tests
- Readout electronics ready for detector integration: 2014 - 2015