The HitDetection ASIC
A Self Triggered Transient Recorder

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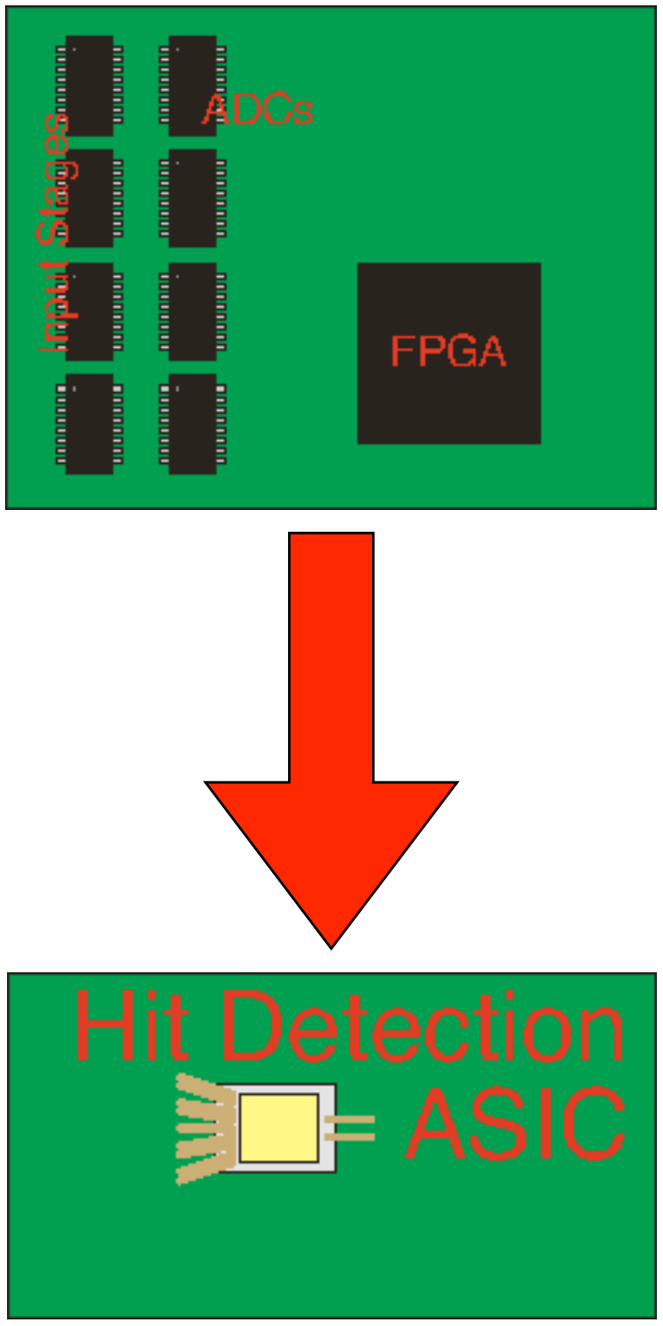
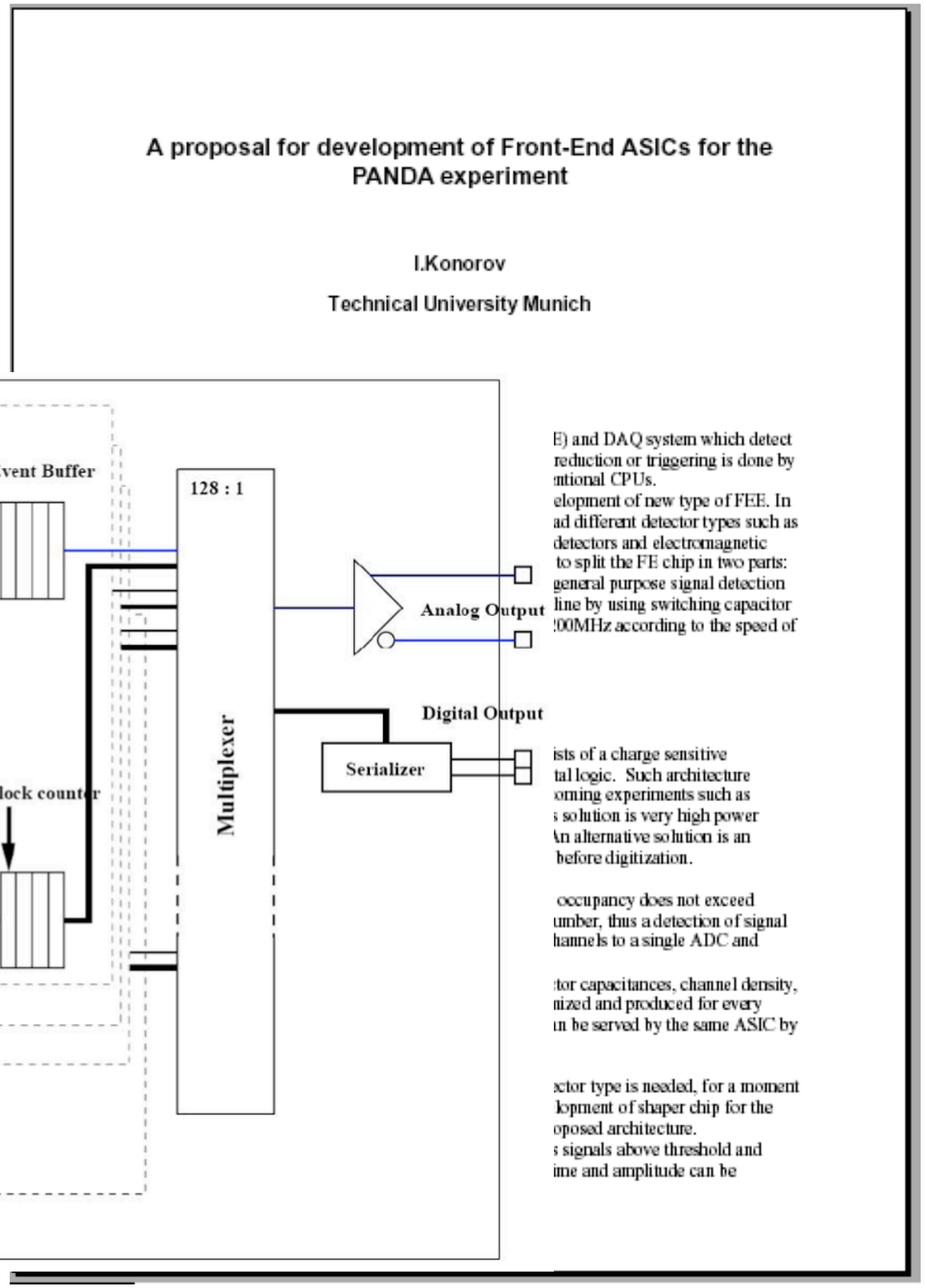
Motivation

- Highly integrated digitisation ASIC
- Less components
  - higher reliability (limited access inside detector)
  - lower power consumption
  - lower number of supply voltages
  - cost reduction
- Radiation tolerance
  - SEUs in FPGA configuration SRAM
- End of 2009: Discussion of different solutions
  - Super-ALTRO
  - New chip with ADCs and DSP
  - HitDetection concept by Igor Konorov



The HitDetection ASIC Concept

- Self triggered transient recorder
- Configurable sampling rate and record length
- Analogue signal storage and derandomisation
- Multiplexed ADC
- Timestamping



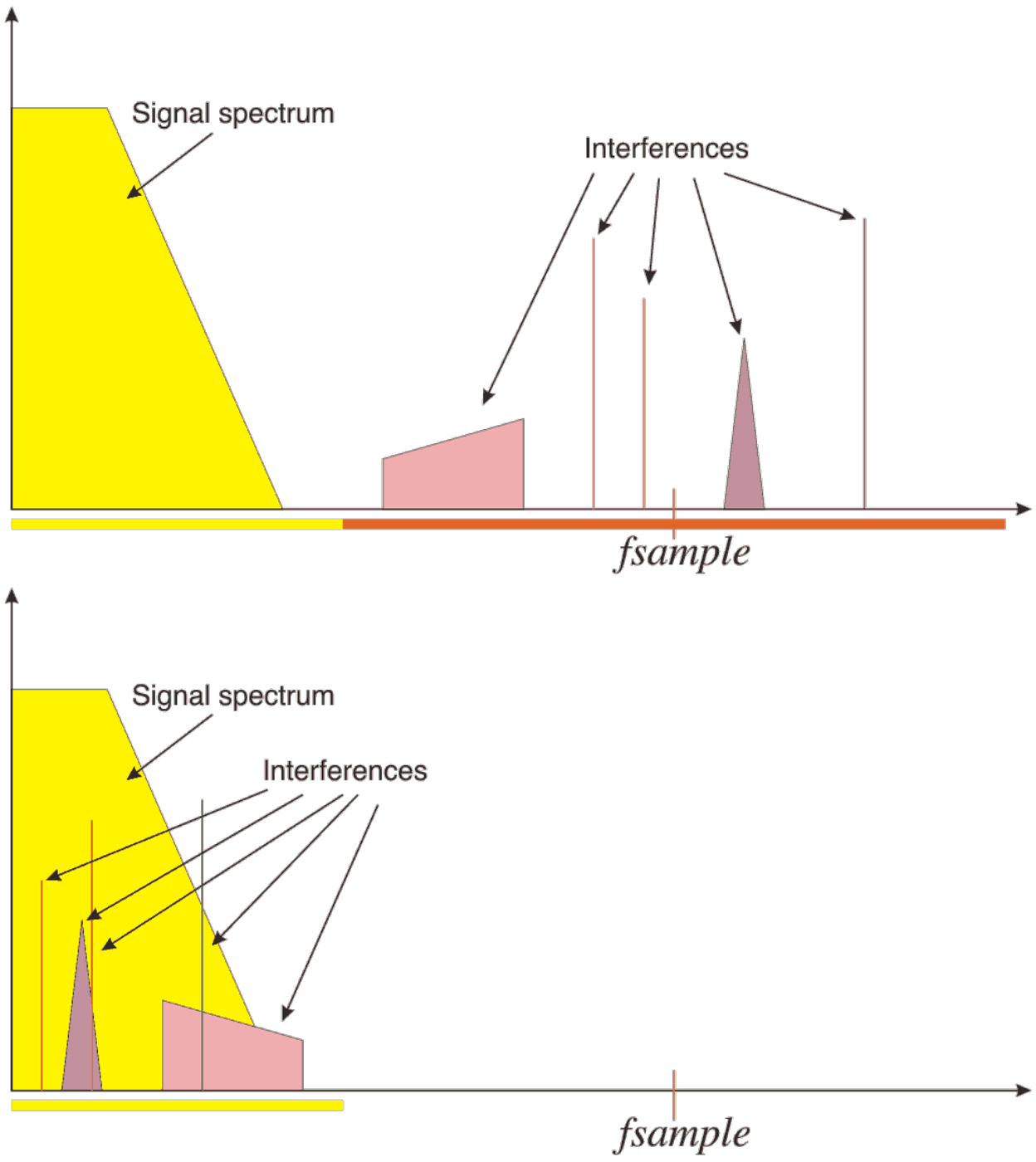
Input Stage

- Currently only requirements from EMC readout
  - High impedance differential inputs
  - Common mode voltage: 1.5 V
  - Range: -1 V ... + 1V
  - - 3 dB Bandwidth: ~ 5 MHz

- ASIC should also be usable for other subdetectors
  - Additional requirements still needed

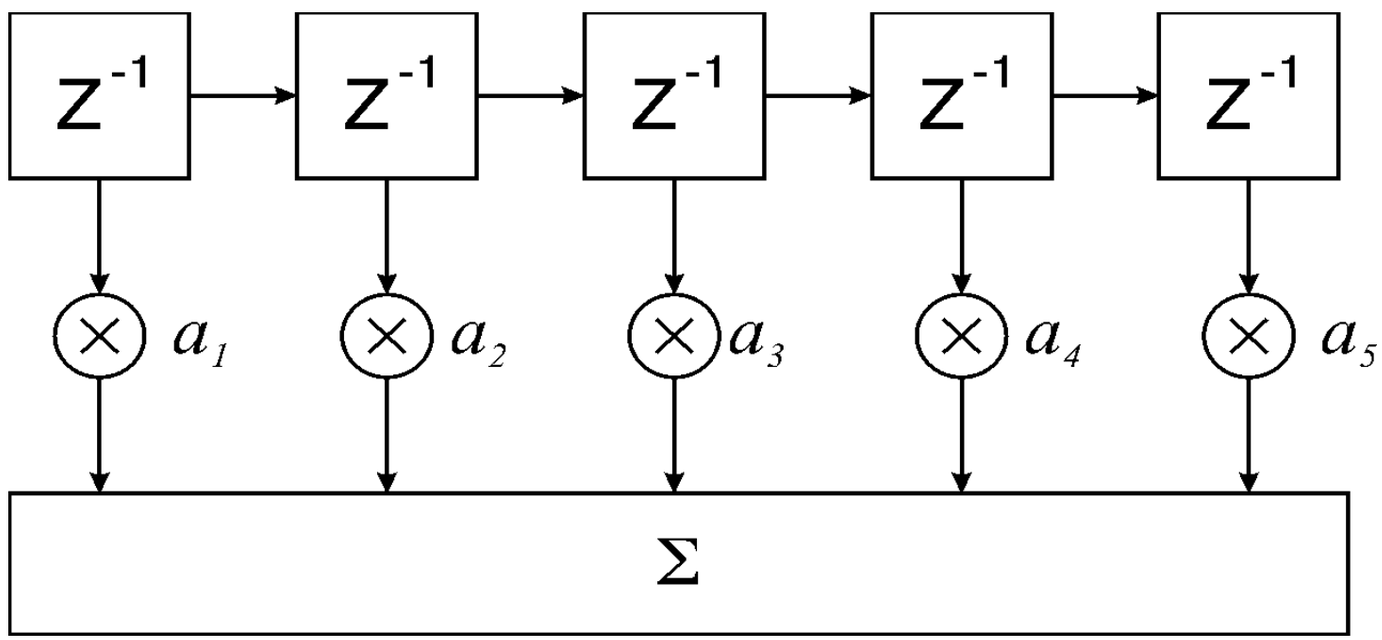
Input Stage -- Anti-Aliasing Filter

- APFEL output signal has limited signal spectrum due to shaping filter
- But:
  - Interferences from pick-up noise?
  - Other front ends?
- Oversampling & digital filtering
  - Increases data rate
  - Increases power consumption
- Analogue anti-aliasing filter
  - Has to be configurable for different sampling rates
  - Good group delay behaviour required



The Hit Detection Unit

- In the proposal of Igor: A FIR filter (Finite Impulse Respond)
  - A continous level, discrete time filter
- FIR filter should be able to detect hits in a pile-up situation
- Drawback: Very complex circuit
  - Do we really need a FIR filter?
  - Order of this filter?
  - Do we need free configurable filter coefficients or are fixed coefficients sufficient?



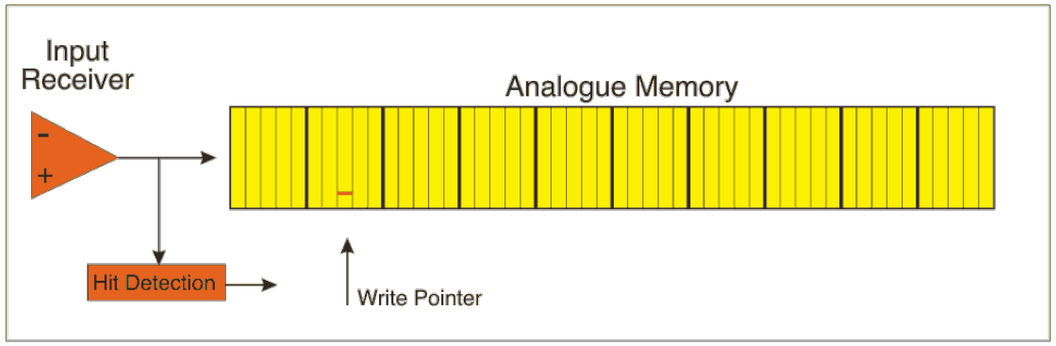
Integration Level

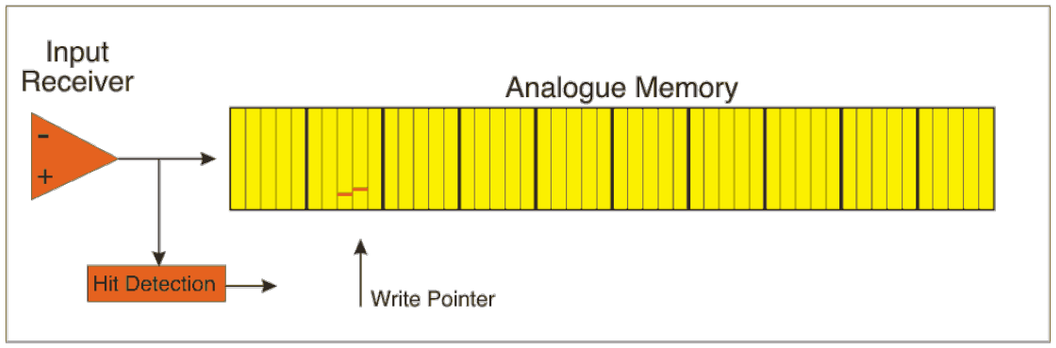
- Channel pitch is given by bonding pads
  - Differential inputs ⇒ 2 Pads / Channel
  - With staggered input pads ⇒ Channel pitch = 100 µm
- Data rate assuming 200 kHz/ch, 8 Samples/Event, 10 bit ADC, 20 bit timestamp

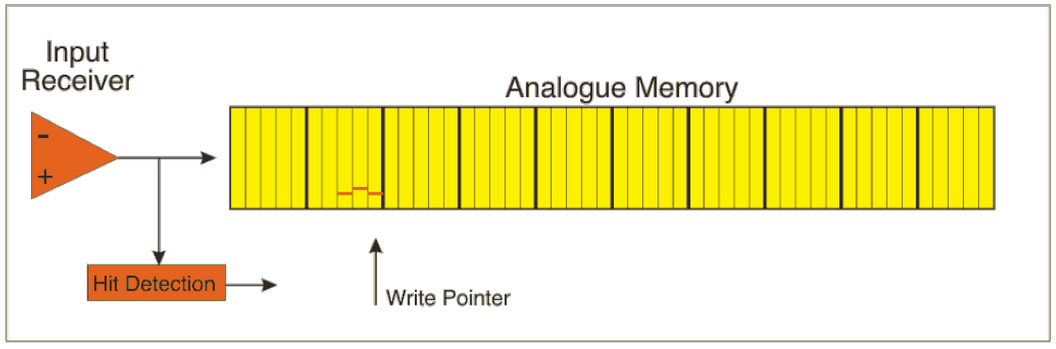
Number of channels	size	Data rate	comments
32	3.2 mm	640 Mbit/s	
64	6.4 mm	1.28 Gbit/s	
128	12.8 mm	2.56 Gbit/s	large chip may lead into yield problems / power

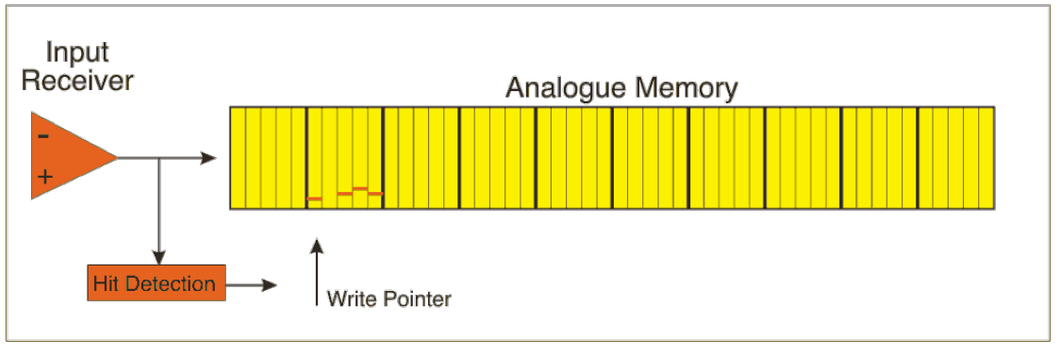
Analogue Signal Storage and Derandomisation

- Capacitor Array used as analogue memory
- Analogue memory is divided into blocks
- Block size might by configurable
- Signals from input receiver are sampled and stored at the position of the write pointer
- Write pointer circles inside of one block
- Circular buffer



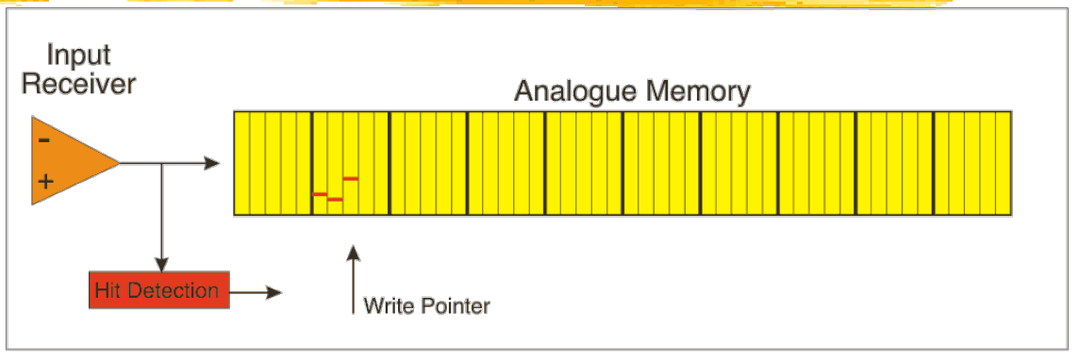


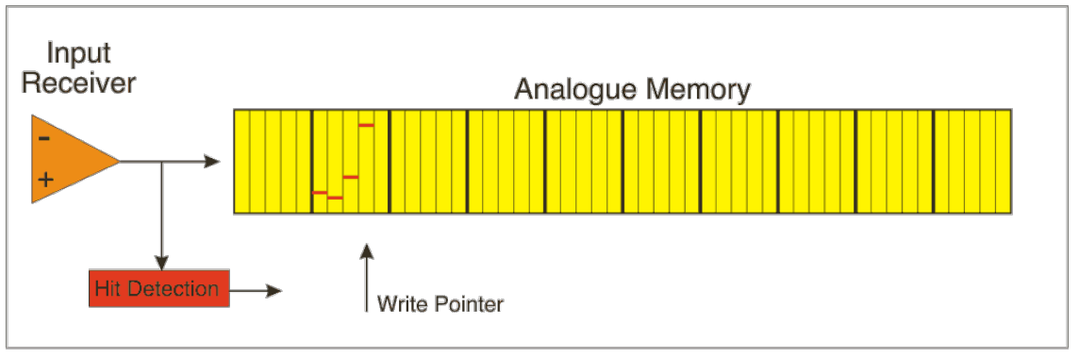


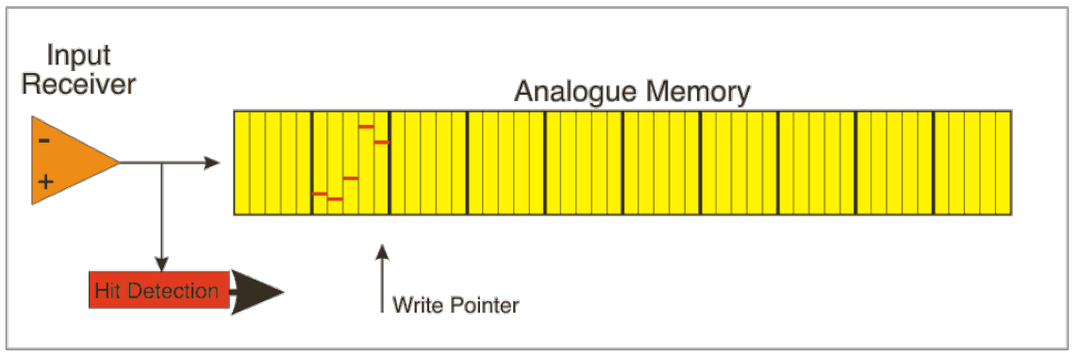


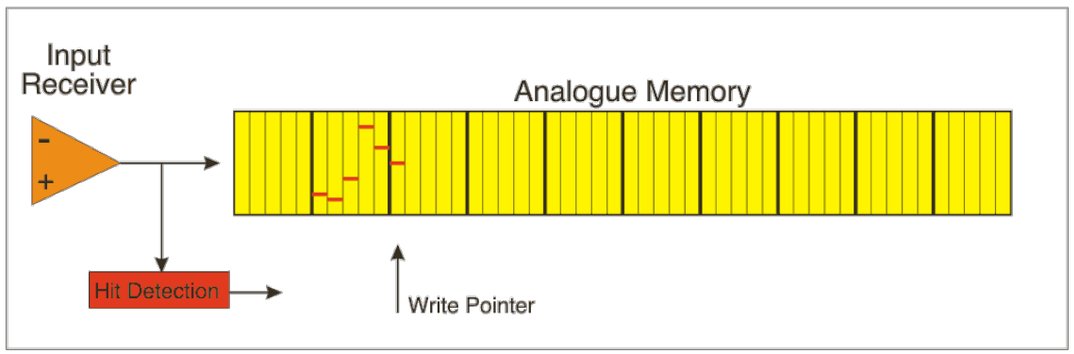
Analogue Signal Storage and Derandomisation

- Signals from particle energy deposits are detected by the hit detection unit
- Write pointer switches to the next memory block
- Signal transient is stored in the previous block
- Analogue readout when multiplexing ADC is available
- Block is available again for signal storage after ADC readout



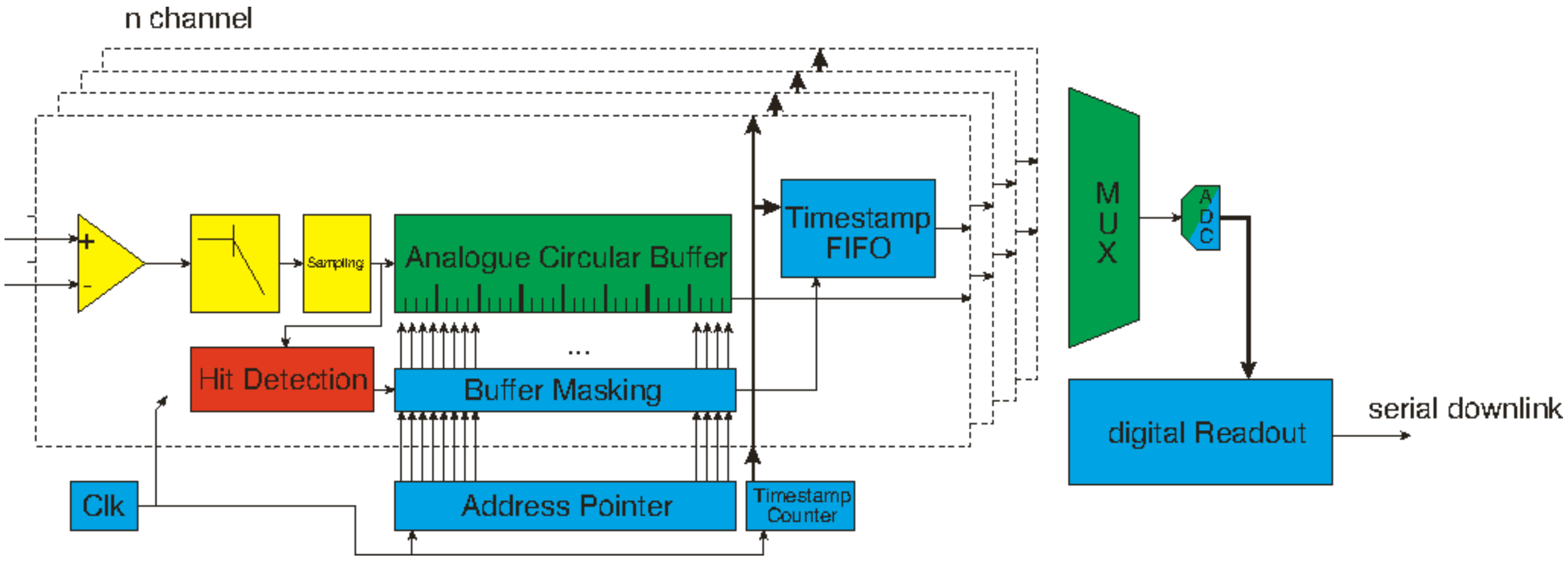






The HitDetection ASIC Concept

- Clock counter for time stamping of detected hits
- Analogue multiplexer for one or more ADCs
- On chip ADC ⇒ digital readout



First Teststructure

- Aim: Design for a first testchip end of this year
- First simulations concerning memory cell behaviour done
- Different conceptional ideas of memory organisation
- Testchip should contain:
  - Input receiver
  - Analogue memory (different architecures)
  - Write pointer logic
  - Slow analogue readout
- Issues to be addressed:
  - Feasable dynamic range
  - Feasable sampling rate
  - Best analogue memory architecture, organisation of storage and read access

Open Questions

- Input specifications
  - Common mode range / dynamic range
  - Sample frequency
  - ...
- Requirements for the feature extraction
  - How many samples are needed?
- Realisation of the hit detection
  - what are the signatures of “hits”
  - how to find them in an analogue way
- …