Status Report of the GET4 TDC

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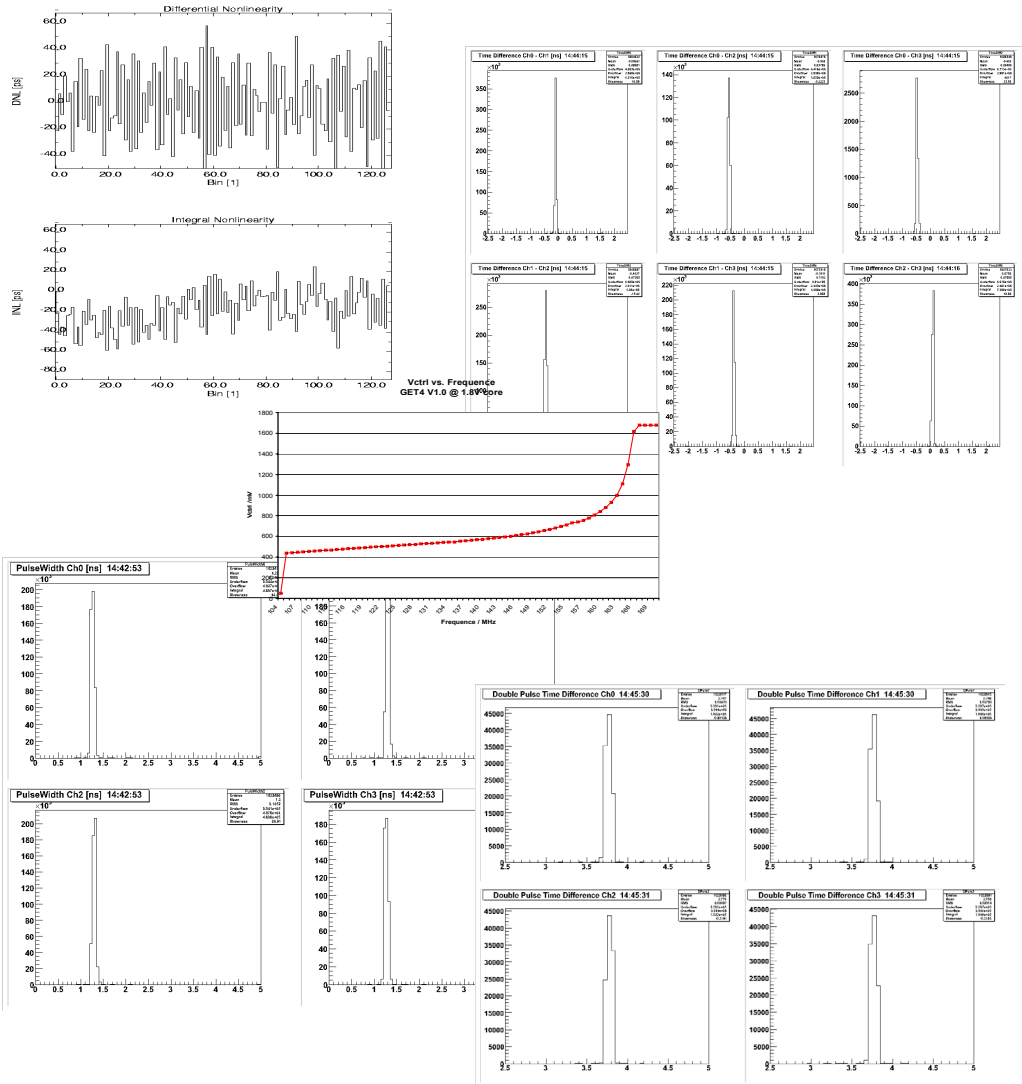
Requirements (Reminder)

- 4 channel DLL based TDC
- High time resolution < 25ps
- Double hit resolution < 5ns
- Event rate up to 100 kHz per channel
- Capability to measure time over threshold
- Low power consumption < 30 mW per channel
- Number of channels: ~ 65.000
- Triggerless operation:
  - Each event combined with a timestamp
  - Epoche event on timestamp counter overflow
- Timestamp counters of all chips have to run synchronously

Measurements and Results GET4

- Clock frequency: 156.25 MHz
- DLL lock range: 110-165 MHz
- Power consumption: 27mW/ Ch.
- Double pulse resolution: < 3.2ns
- Time resolution: < 25ps
- Linearity:
  - DNL = +/- 1.2 LSB
  - INL = +/- 1.5 LSB



FEET-TDC1 Board for Detektor Tests

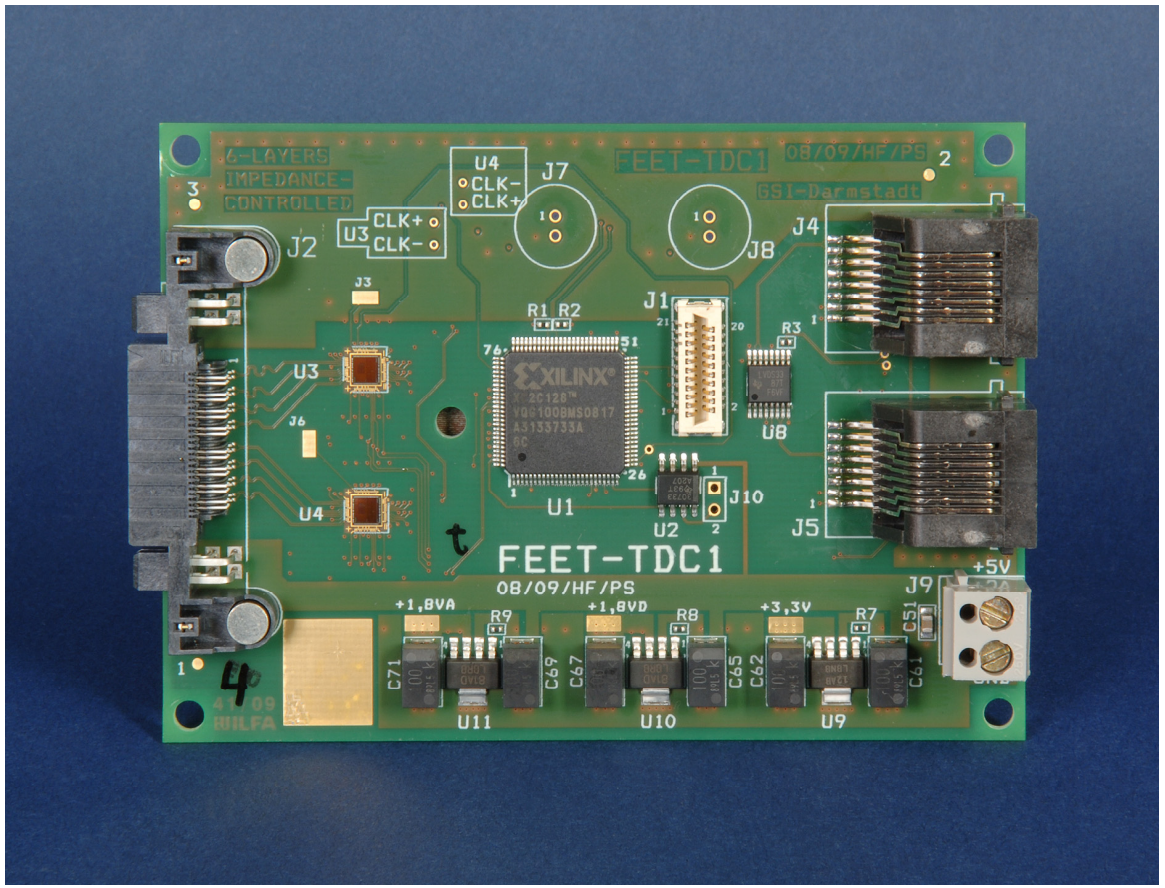
- For first tests on an RPC demonstrator module

  FEET TDC1 boards are produced and assembled

- Each FEET TDC1 board consists of 2 GET4 chips

  (8 channel/board)

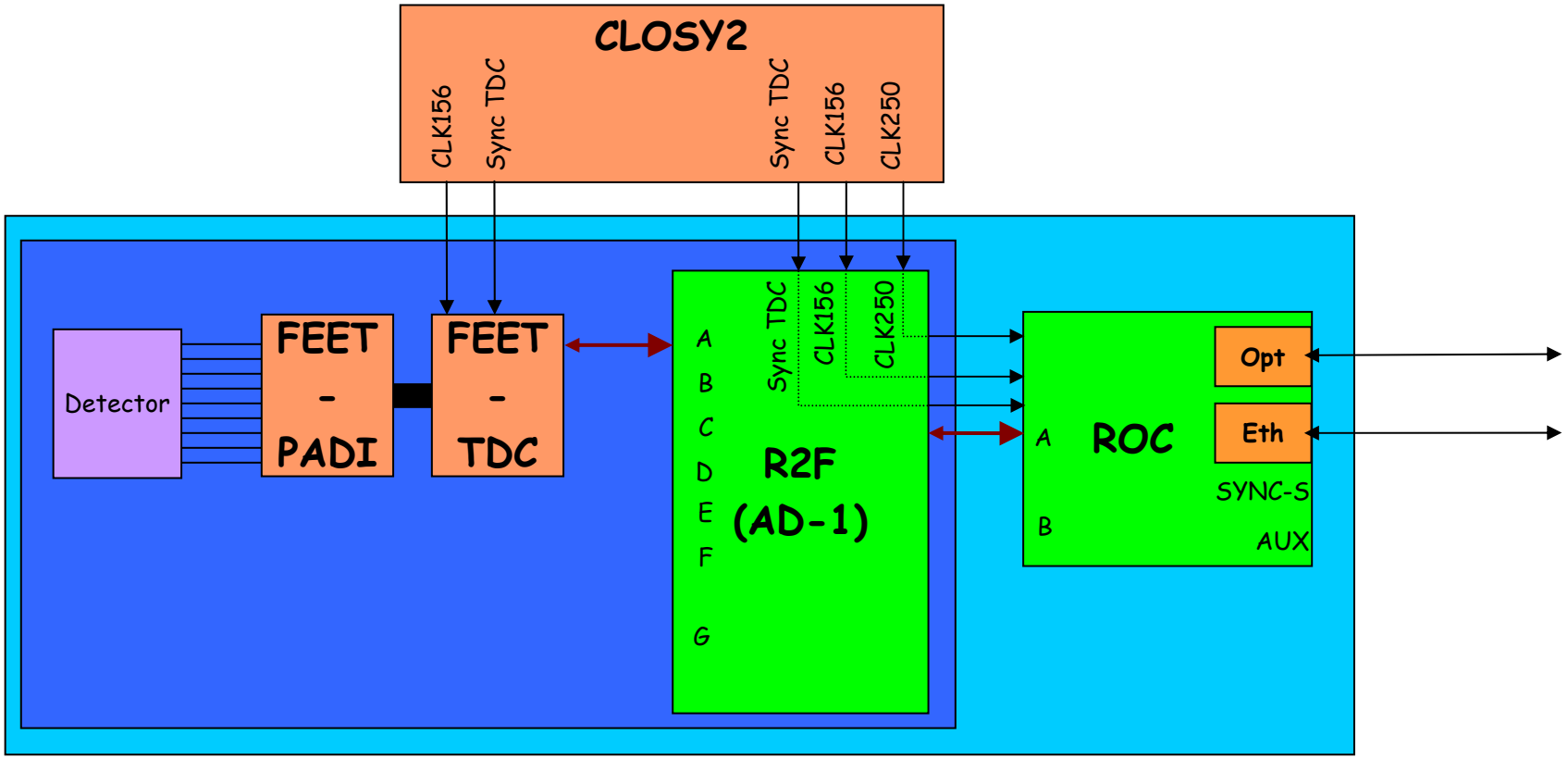
- 4 FEET TDC1 boards are available for tests @ PANDA



Current Activities .....

CLOSY @ GSI and ROC @ Heidelberg

Connection Scheme:



Data Format and Data Rates GET4

- Data format 24 bit
  - 2 x 24 bit for leading and trailing edge
  - => 48 bit / Event
- Maximum RClk = 312 .5 MHz
  - Data rate: 312 .5 Mbit/s
  - => 1.6 MHz Event rate / Channel

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Event Typ		Ch		Ed.	12bit Timestamp												7bit FineTime						

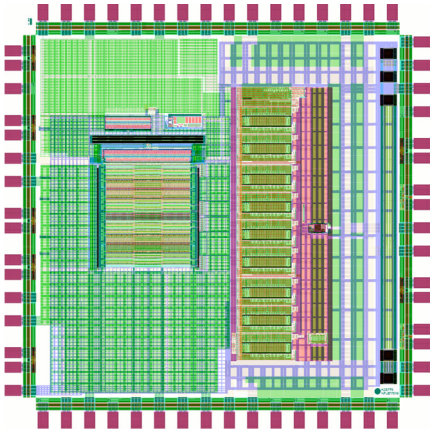
Future Data Format

- Data format 32 bit
  - 1 x 32 bit for leading edge and ToT
  - => 32 bit / Event
- Maximum RClk = 312 .5 MHz
  - Data rate: 312 .5 Mbit/s
  - => 2.4 MHz Event rate / Channel

31	30	29	28	27	---	16	15	-	9	8	-	2	1	0
Event Typ		Ch		12 bit Timestamp			7bit FineTime			7bit ToT			Spare	

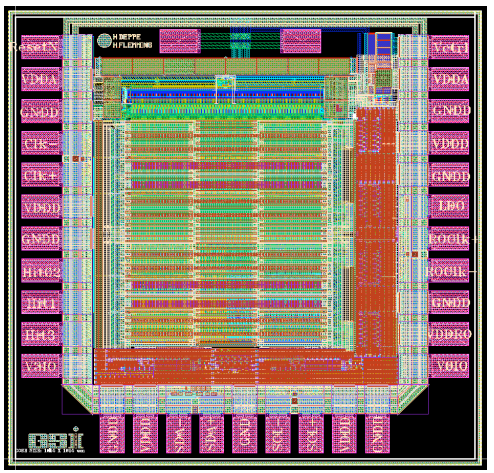
Measurements & Design Activities

- Measurements on the DNLImprov Mini-ASIC to check out the best layout strategies and D-FlipsFlops to be used in next iterations



- Design of 10bit DAC and comparator

- Design of serial slow control uplink



Summary

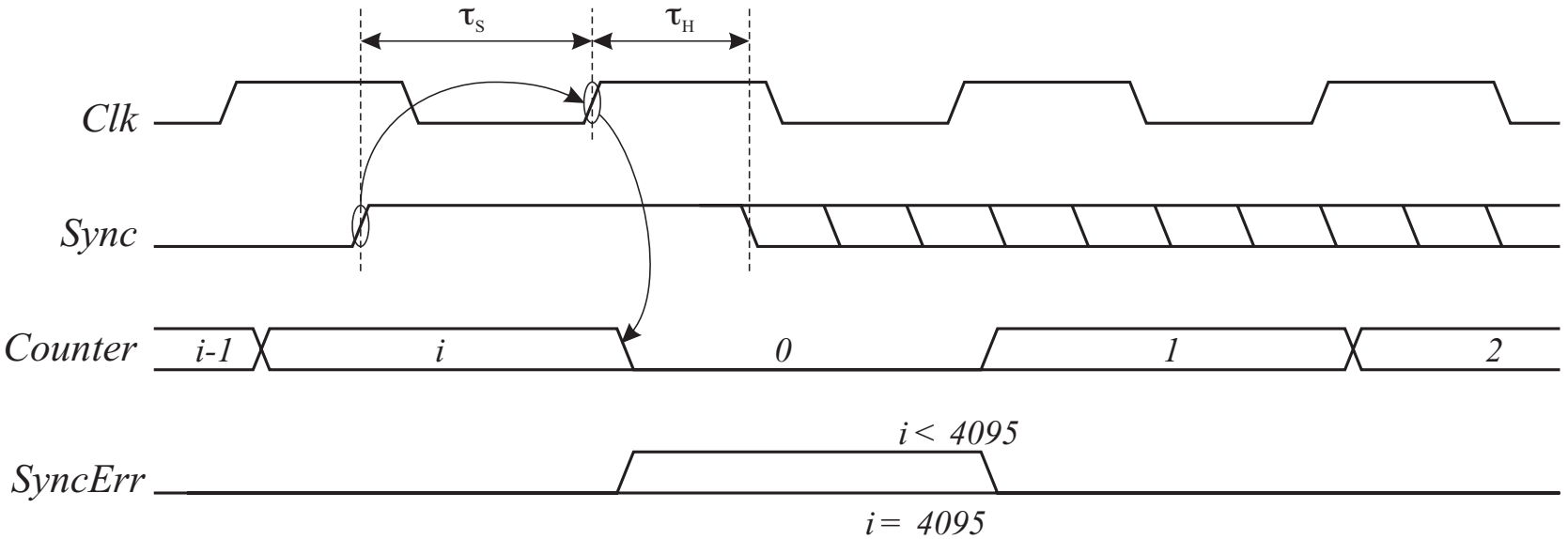
- FEET-TDC1 boards are available
- ROC and DAQ are under development
- Data format on the next GET4 iteration will be changed
  - => Event rates up to 2.4 MHz possible
- Measurements concerning linearity improvement
  - => Improve the resolution
- Current design activities :
  - 10 Bit DAC & Comparator
  - Seriel Slow Control uplink
  - OnChip ToT calculation

Thanks .....

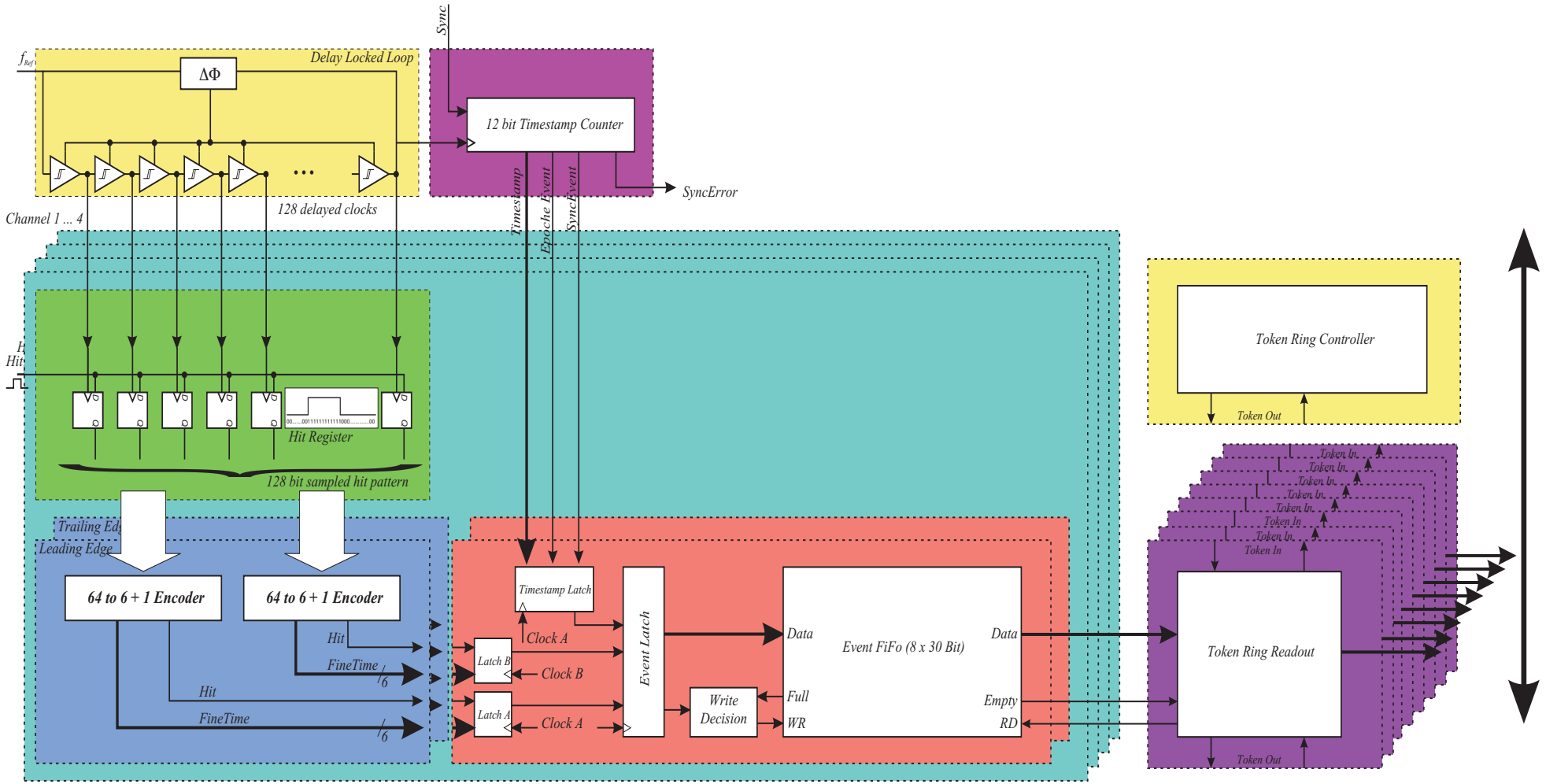
- ..... for your attention

Timestamp Synchronization

- External Sync signal
- Synchronization on next leading edge of clock after leading edge of Sync signal
- Flagging of Epoche and Sync events



Schematic Overview of GET4 Prototype

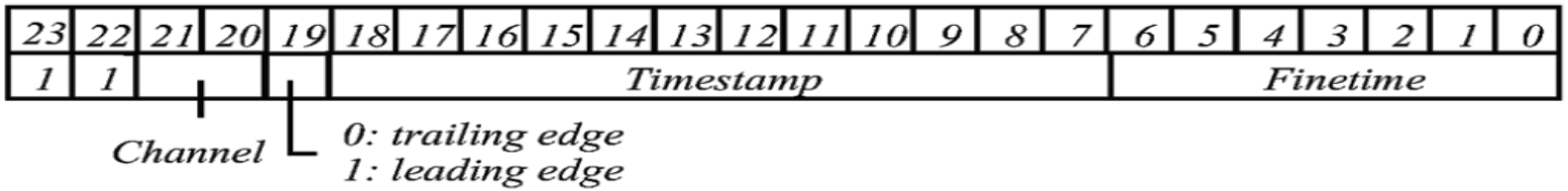


29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Epoche				Time Stamp													Fine Time B							Fine Time A					

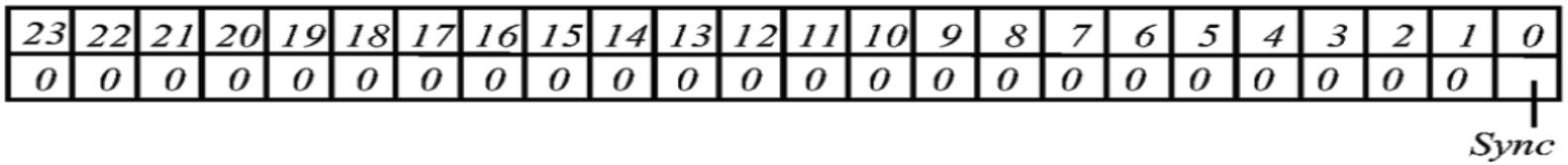
Sync Hit B Hit A

Event Format

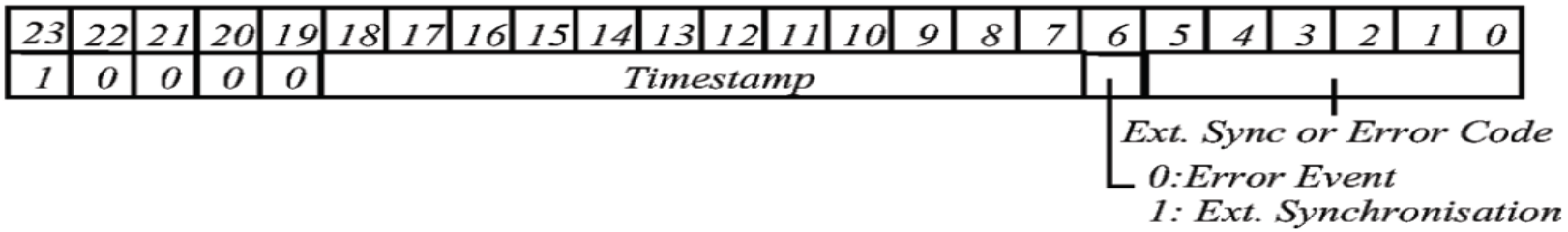
Data Events



Epoche Event

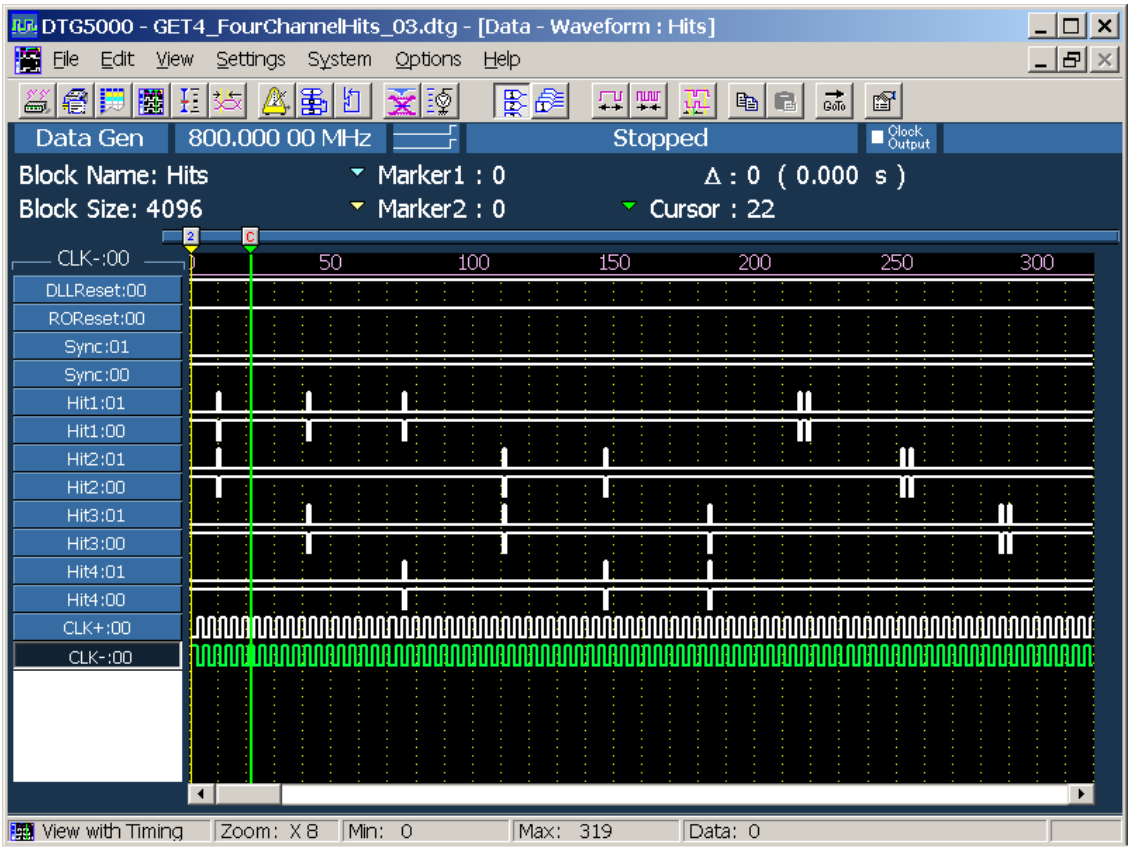


Ext. Sync and Error Event



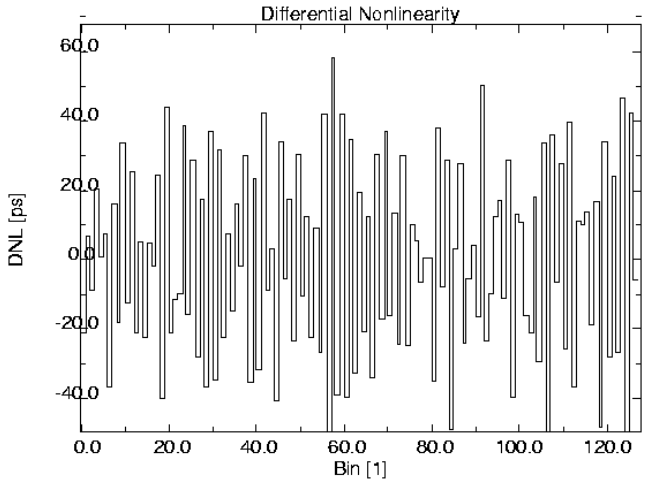
Test Setup: Hit Signal Stimulus

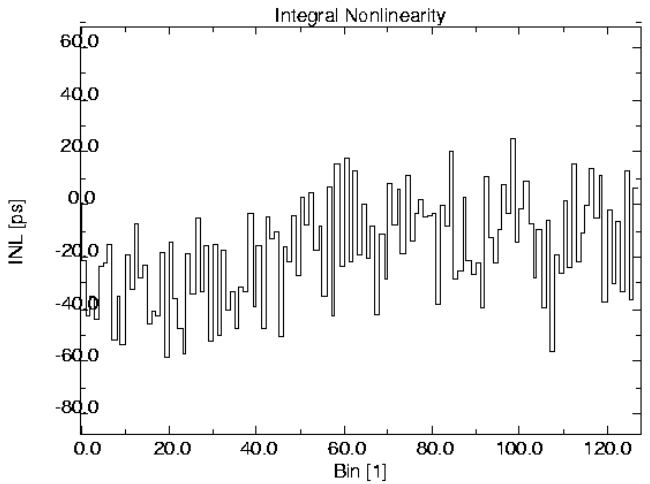
- Puls Width: 1.25 ns
- Synchronous Pulses on two channels
- Double Pulses, 3.75 ns puls spacing



Measurements and Results GET4

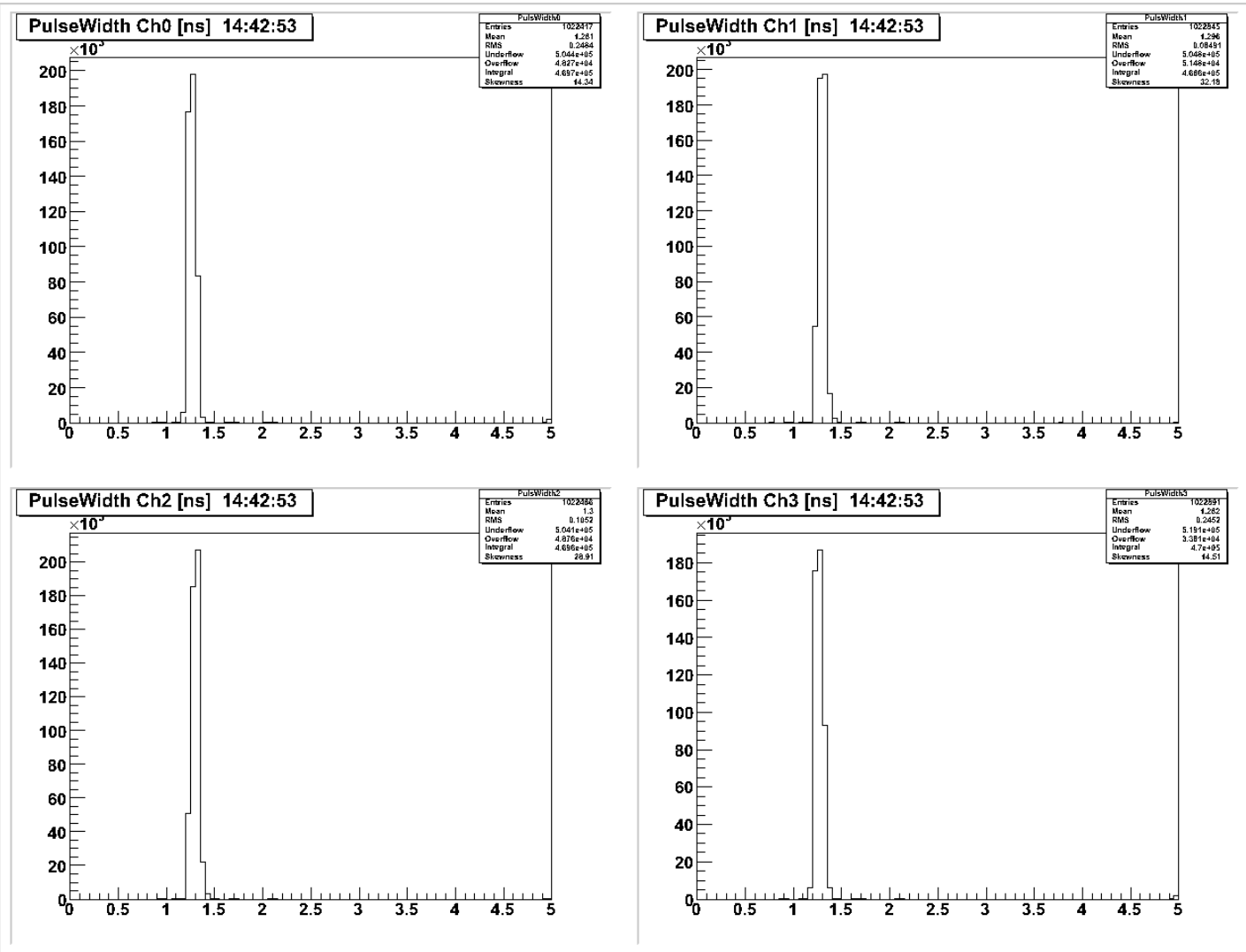
- Linearity:
  - DNL < +/- 60 ps = +/- 1.2 LSB
  - INL < +/- 80 ps = +/- 1.5 LSB
- In comparison to DANTE:
  - DNL: +/- 0.4 LSB
  - INL: +/- 0.5 LSB
- Reasons for Nonlinearity are still under investigation





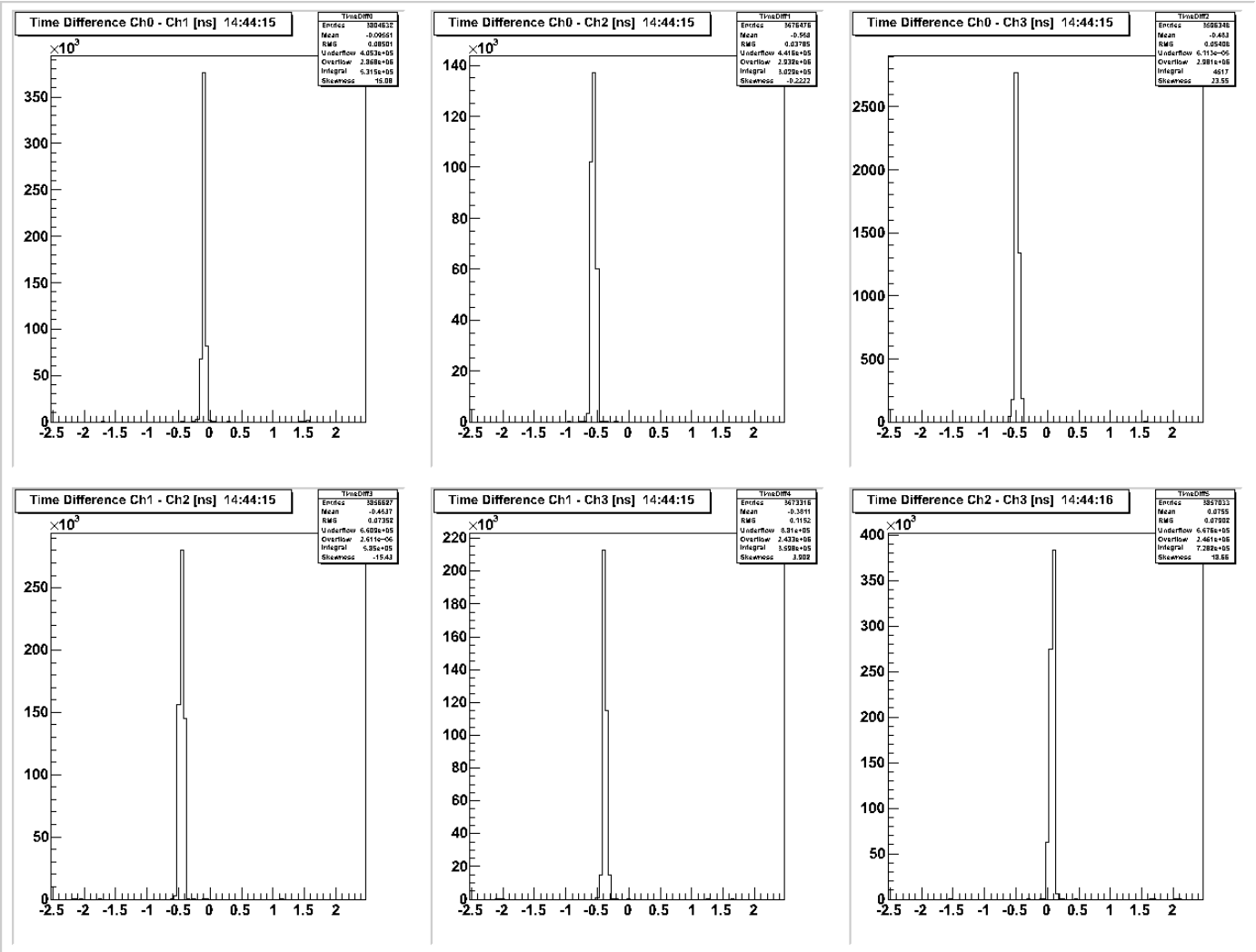
Measurements and Results GET4

- Puls Width Measurements
- μ : 1.283 ns
- σ : 36.7 ps
- Uncorrelated Resolution: 25.9 ps



Measurements and Results GET4

- Time Difference
- σ : 29.1 ps
- Uncorrelated Resolution: 20.6 ps



Measurements and Results GET4

- Puls spacing Measurements
- μ : 3.766 ns
- σ : 33.5 ps
- Uncorrelated Resolution: 23.7 ps