

Feature-Extraction Algorithms for the PANDA Electromagnetic Calorimeter

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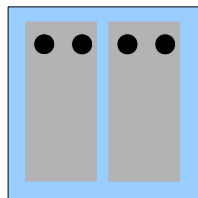
for the PANDA collaboration

KVI, University of Groningen, Groningen, The Netherlands

- **Sampling ADC readout**
- **On-line data processing**
- **Precise energy/time of the pulse**

Electromagnetic Calorimeter (EMC)

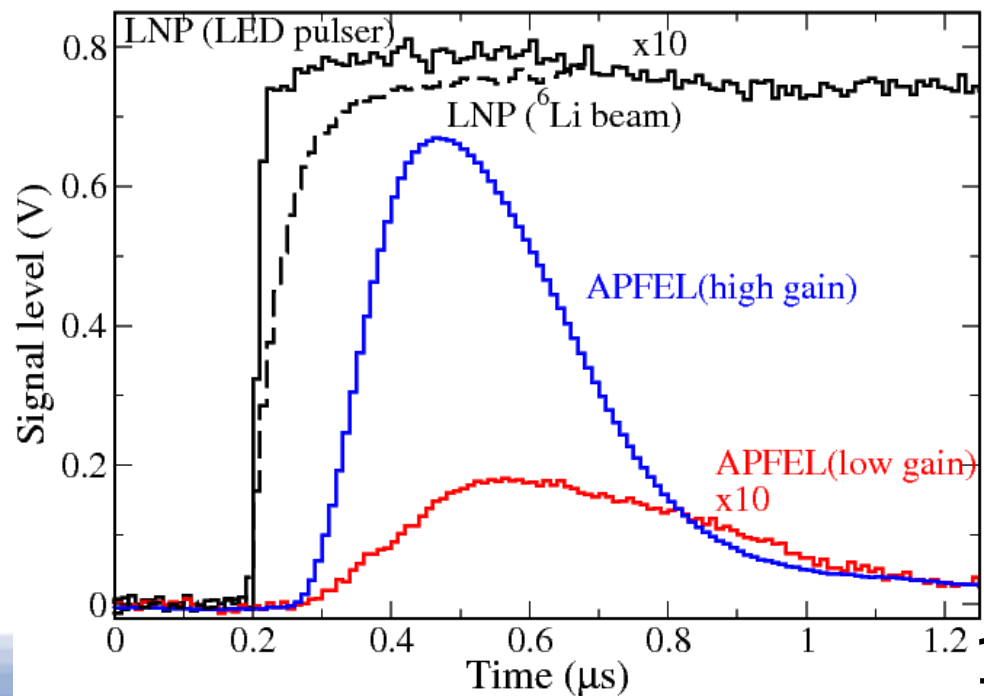
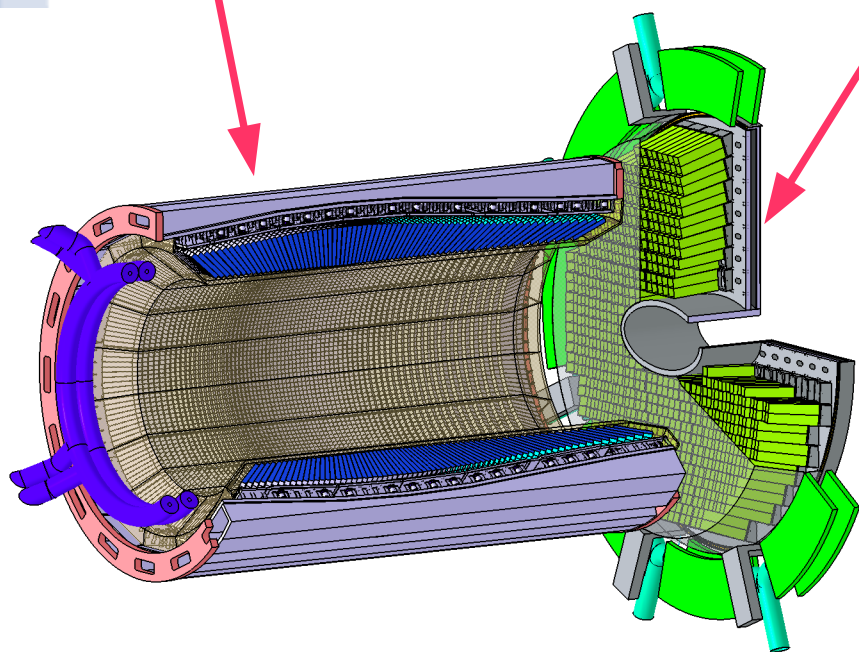
Barrel:



- 2 LAAPD per crystal
- APFEL ASIC preamp. (GSI):
 - two independent channels
 - two ranges per channel
 - built-in shaper

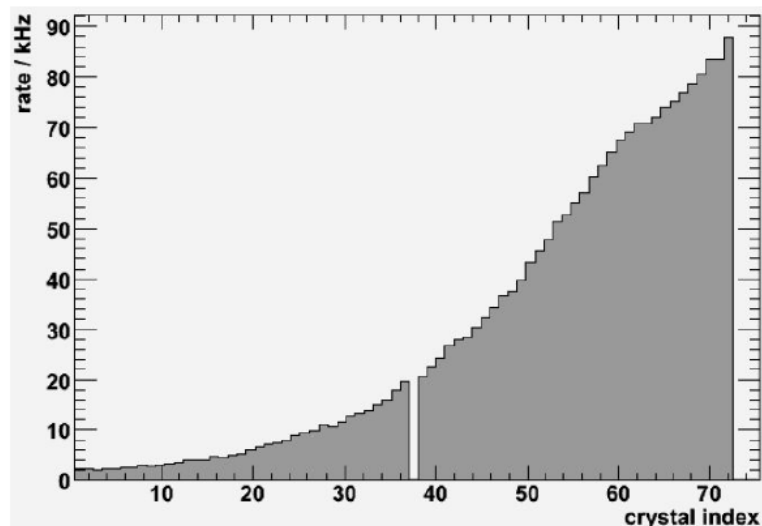
End-cap:

- One VPT per crystal
- Discrete-component LNP preamp. (Basel)
 - Single range
 - no shaper (25 μ s time constant)
 - build-in 50 Ω line driver



Expected Single-Crystal Rates (EMC TDR)

Barrel



Max. rate:

100 kHz

150 kHz

250 kHz



Max. rate:

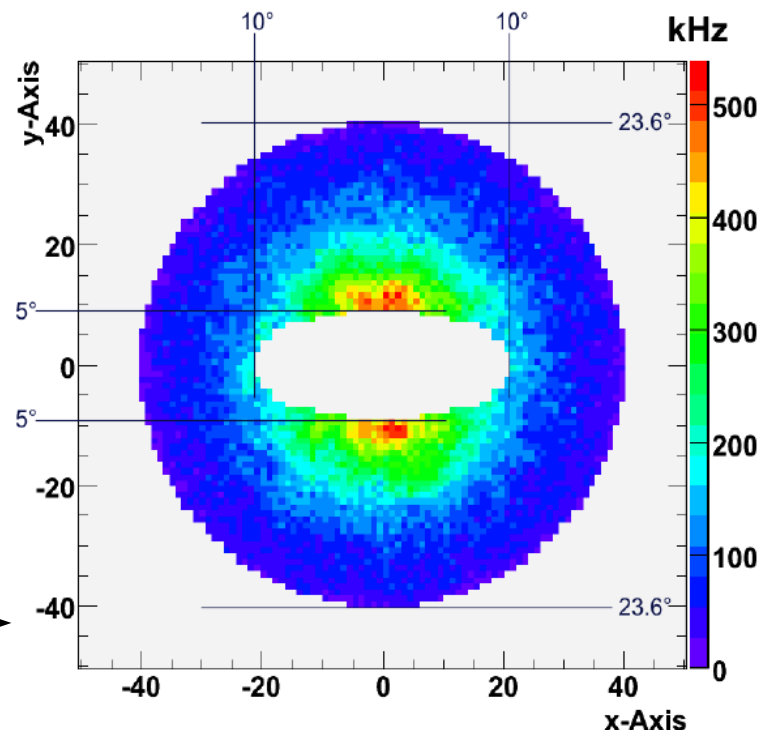
500 kHz

750 kHz

1.25 MHz



End-cap

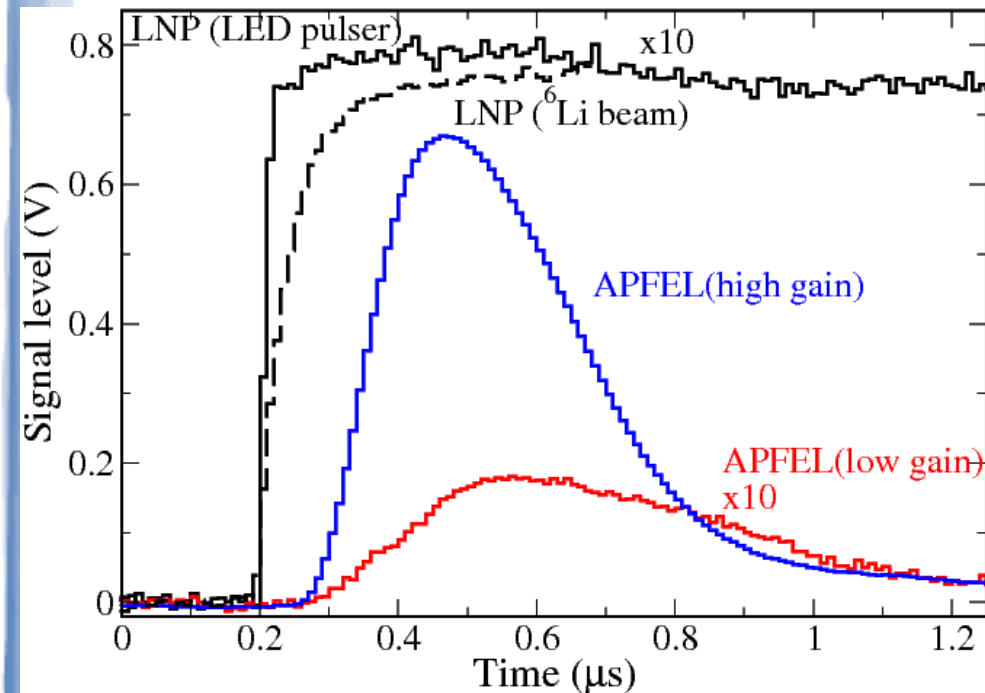


Rates in TDR are estimated for
20 MHz interaction rate.

Electronics should be prepared
for 30/50 MHz!

Optimal signal shaping:

- Optimize energy resolution / dynamic range
- Minimize pile-up probability
- shorten the pulse-length



LNP preamplifier:

- Shaper is required:
 - Analogue
 - Digital
- Shaper optimization for:
 - Energy/Time resolution
 - Hit-rate capability

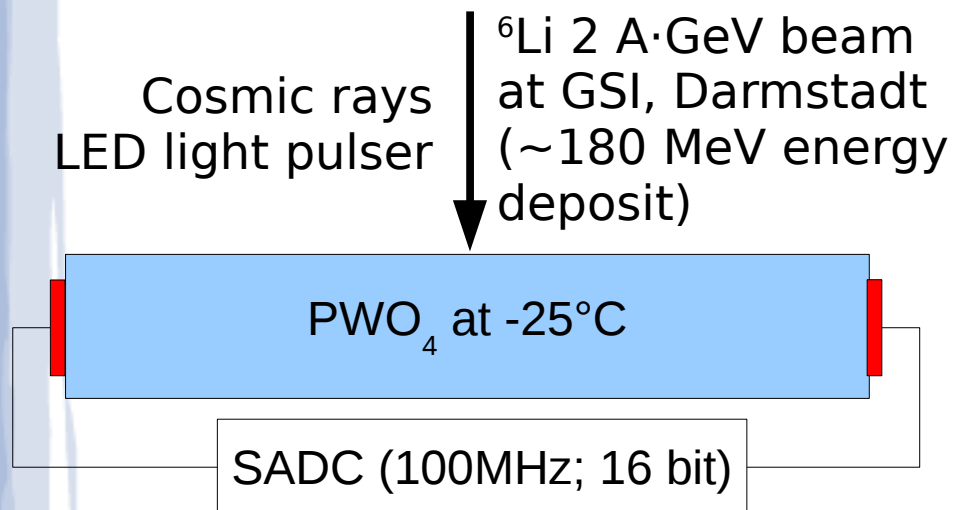
ASIC preamplifier:

- Shaper is optimized for energy resolution/dynamic range
- Pile-up treatment is mandatory

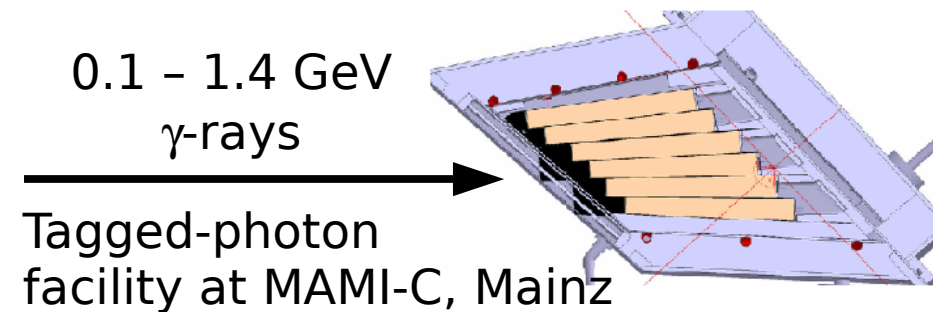


- Measurements are done using **SADC (16 bit, 100 MHz)** directly coupled to the preamplifier
- 10 μ s long traces are stored for each event
- Traces are analysed in software
- VHDL implementation is ready

Single-crystal setup

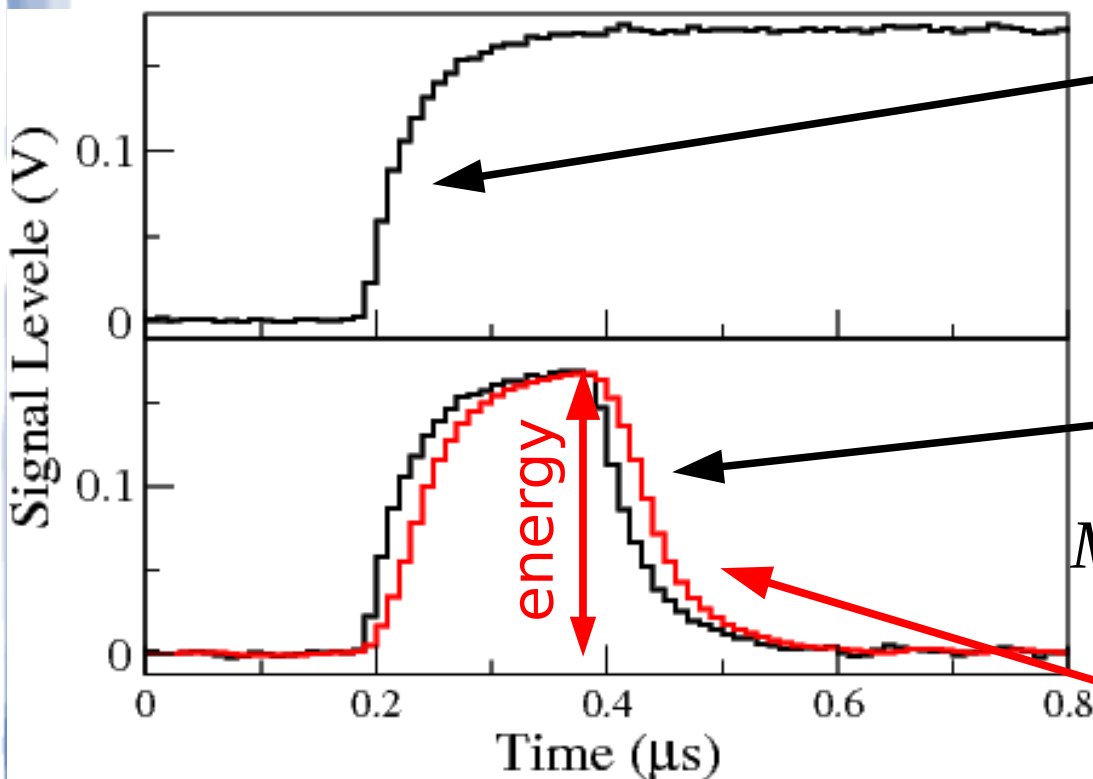


“Proto60” – EMC prototype of 60 crystals (**SADC readout of 3×3 crystals matrix**)



LNP Preamplifier Signal Treatment

Pulse Processing (Triggering and Energy)



Raw Trace
 $\tau = 25 \mu\text{s}$ - decay constant

Moving Window Deconvolution¹
- differentiation + PZC
(MWD) filtering:

$$MWD_M(n) = x_n - x_{n-M} + \frac{\ln 2}{\tau} \sum_{i=n-M}^{n-1} x_i$$

Smoothed MWD signal
integration

(moving averaging, MA)

This signals is used for the
triggering and **energy** readout

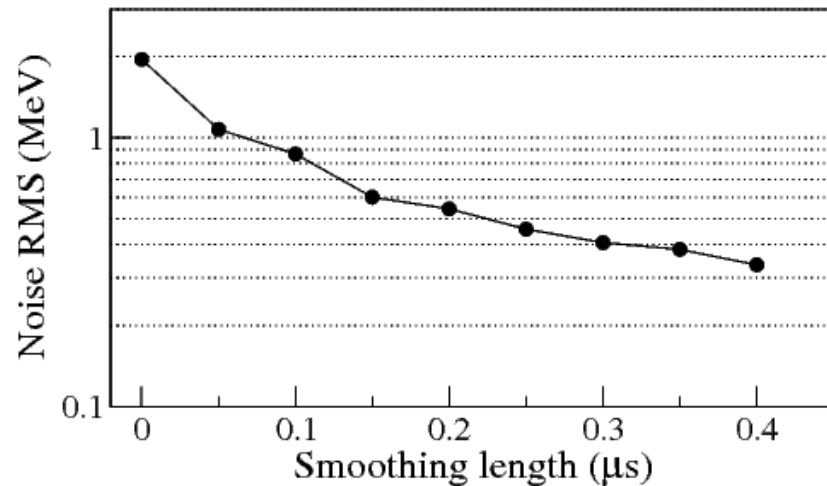
Energy resolution and noise level depends only on the smoothing length

1. A. Georgiev, W. Gast, IEEE Trans. Nucl. Sci. NS-40 (1993) 770; J. Stein *et al.*, Nucl. Instr. Meth. B 113 (1994) 141.



Triggering Threshold and Energy Resolution

Noise level as a function of the smoothing length

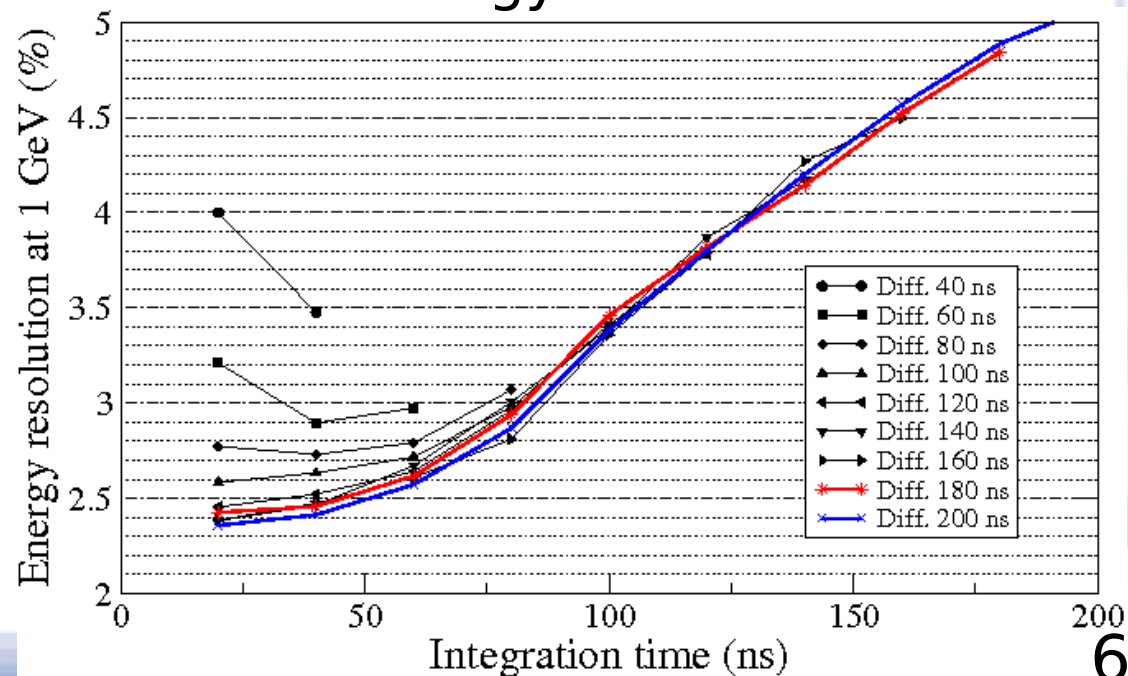


Smoothing:

- decreases noise level
- increases pulse length – pileup correction needed

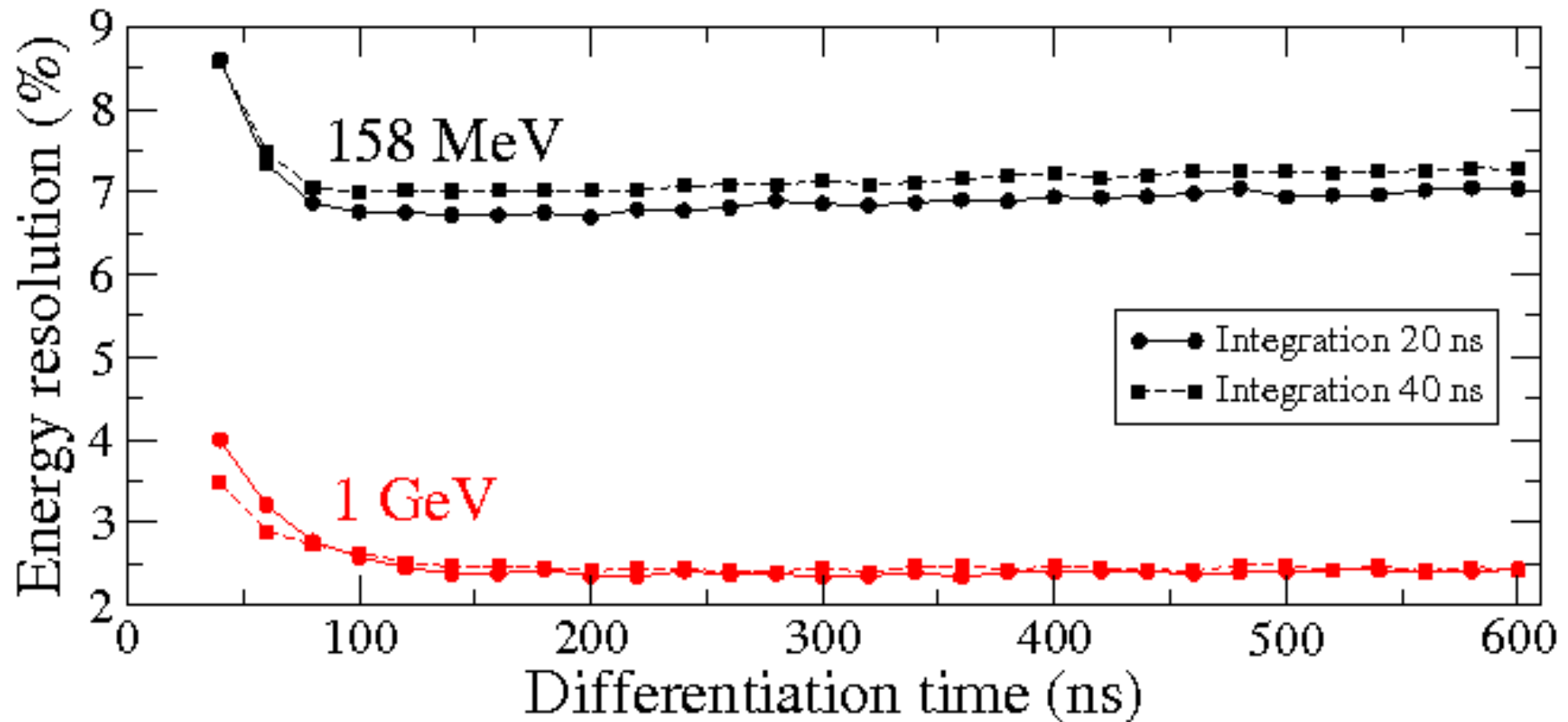
At low diff. time constants additional integration reduces the resolution!

Effect of filtering on the energy resolution

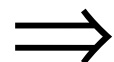


Forward End-Cap LNP preamplifier

Scan of the differentiation parameter



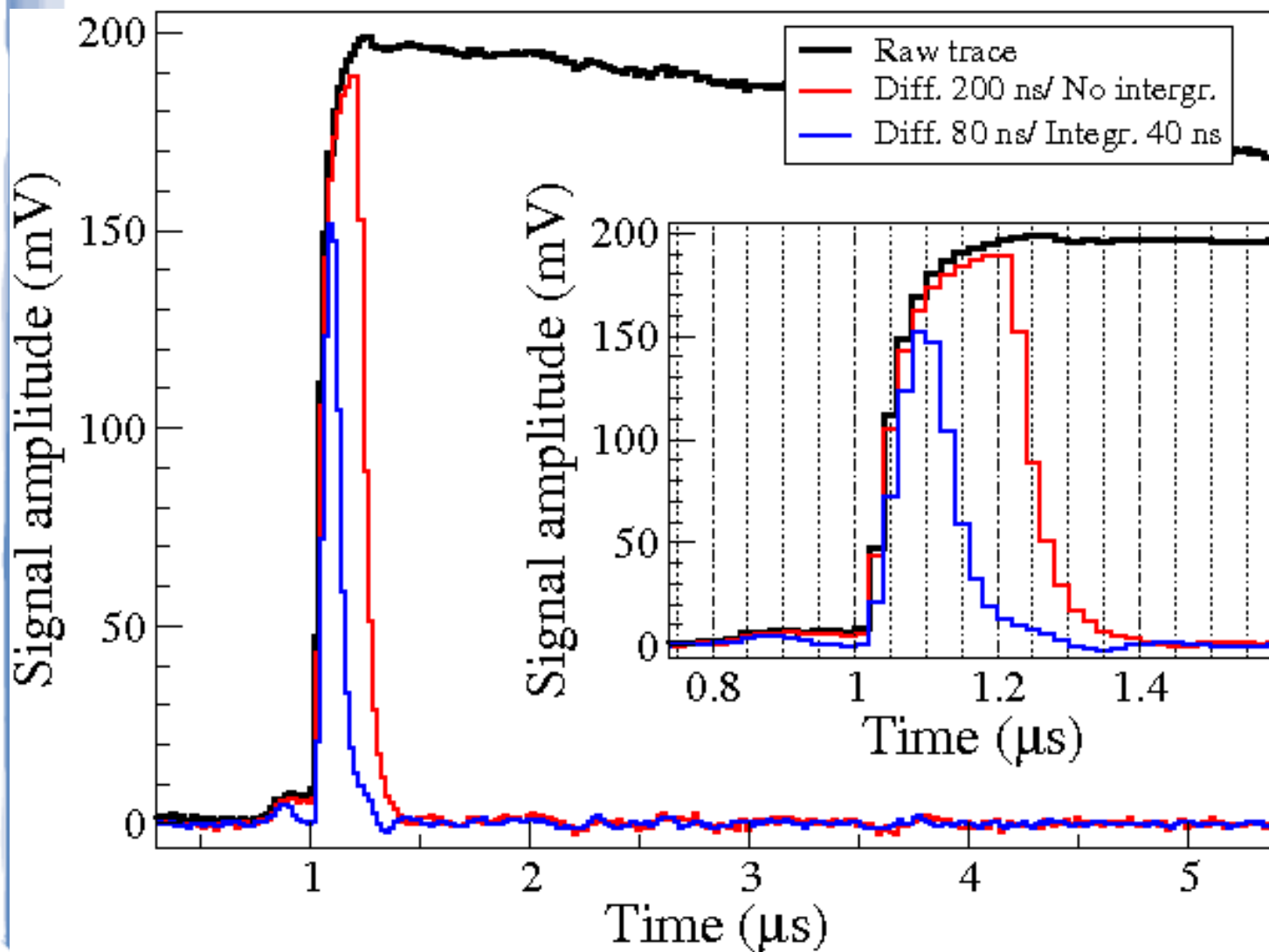
Resolution
saturates at
about 200 ns



The rise-time of the signal
(with slow component) is
about **200 ns**

Forward End-Cap LNP preamplifier

Pulse shapes



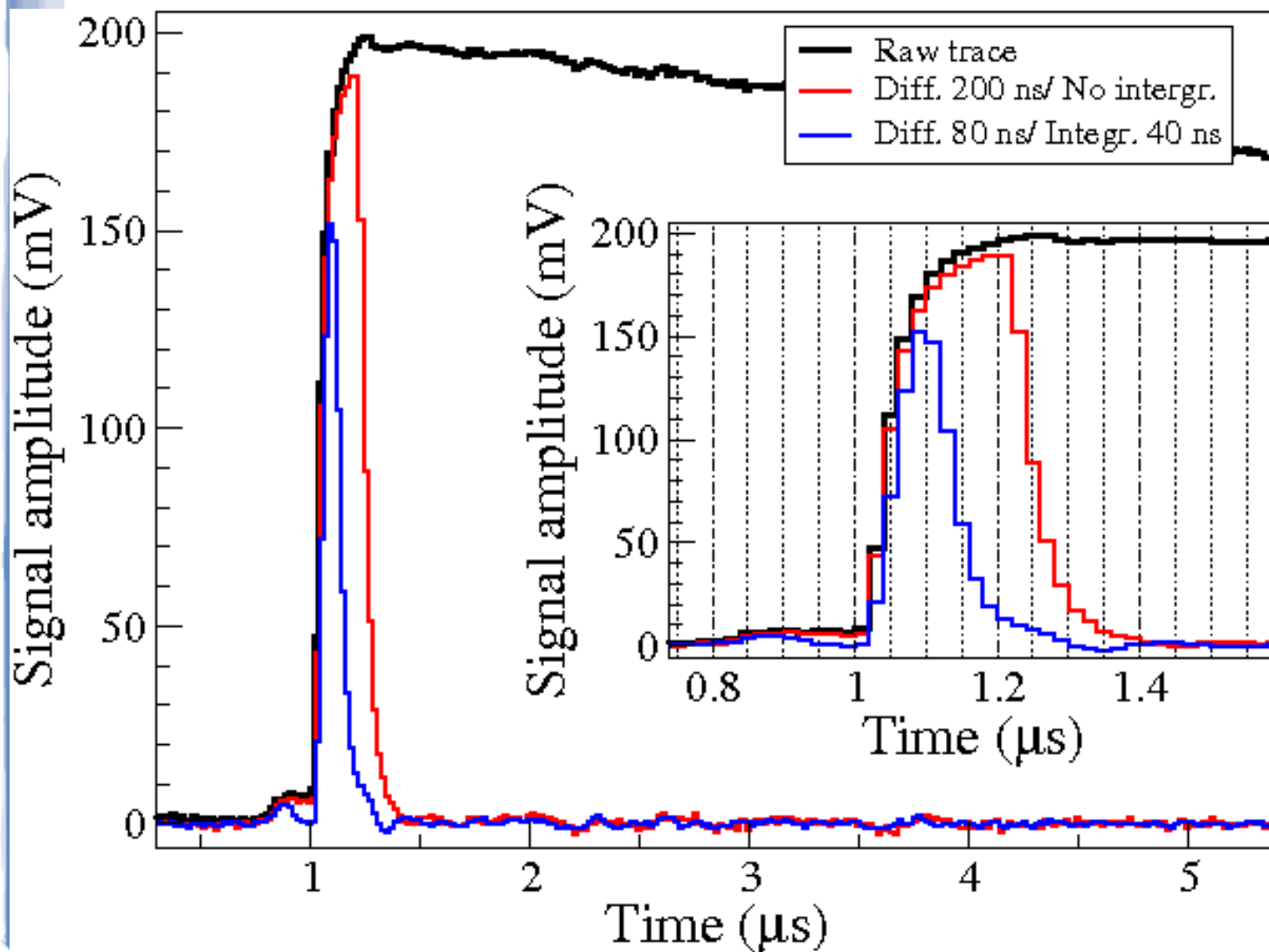
Long rise-time
with slow
component **never**
observed with
LED light pulser
(same
LAAPD+preamp)



Feature of PWO?

Forward End-Cap LNP preamplifier

Pulse shapes



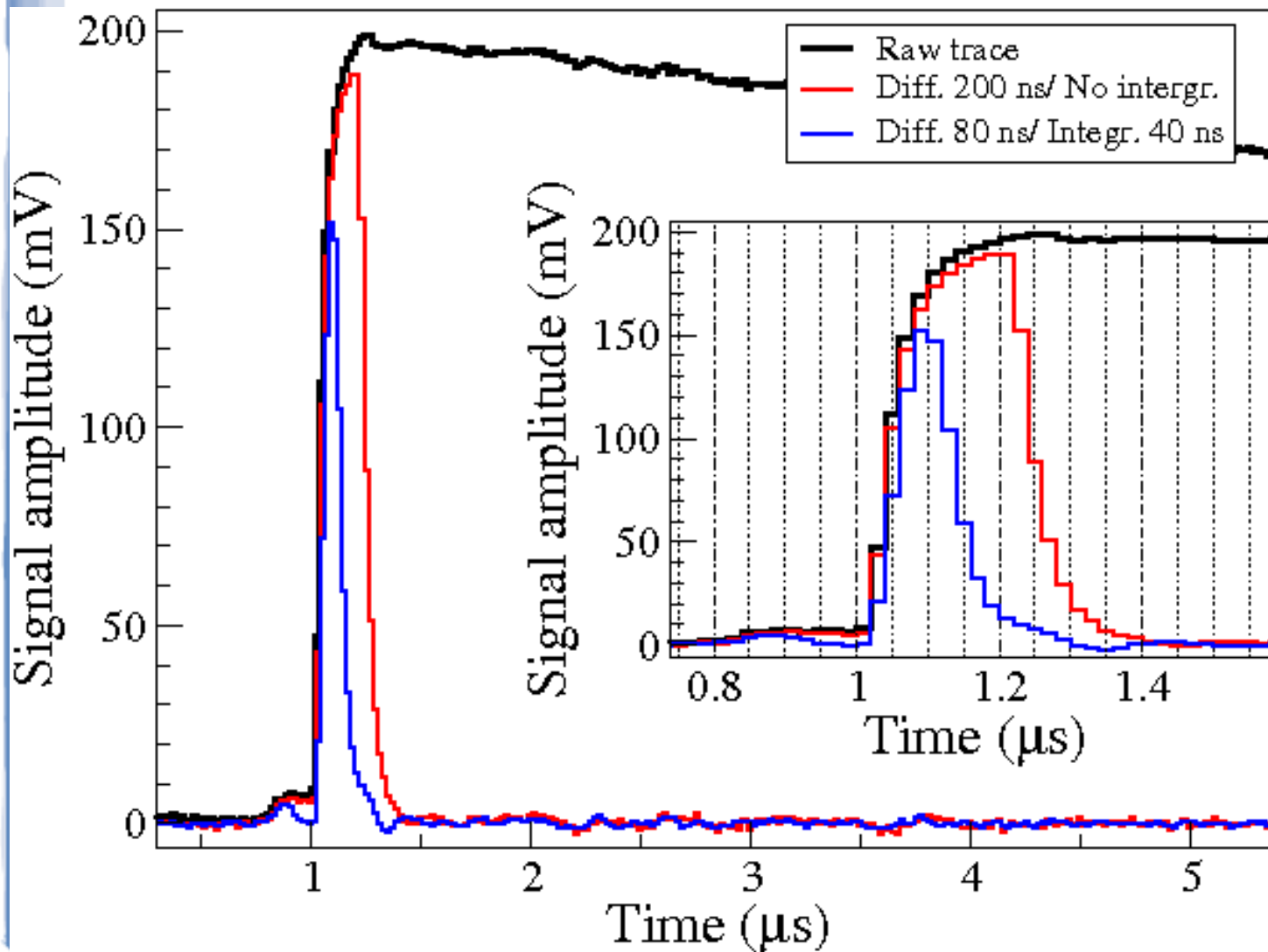
Short diff. time
does not allow to
avoid pile-up but
reduces
resolution



Pulses close than
400 ns require
**pile-up
treatment**

Forward End-Cap LNP preamplifier

Pulse shapes



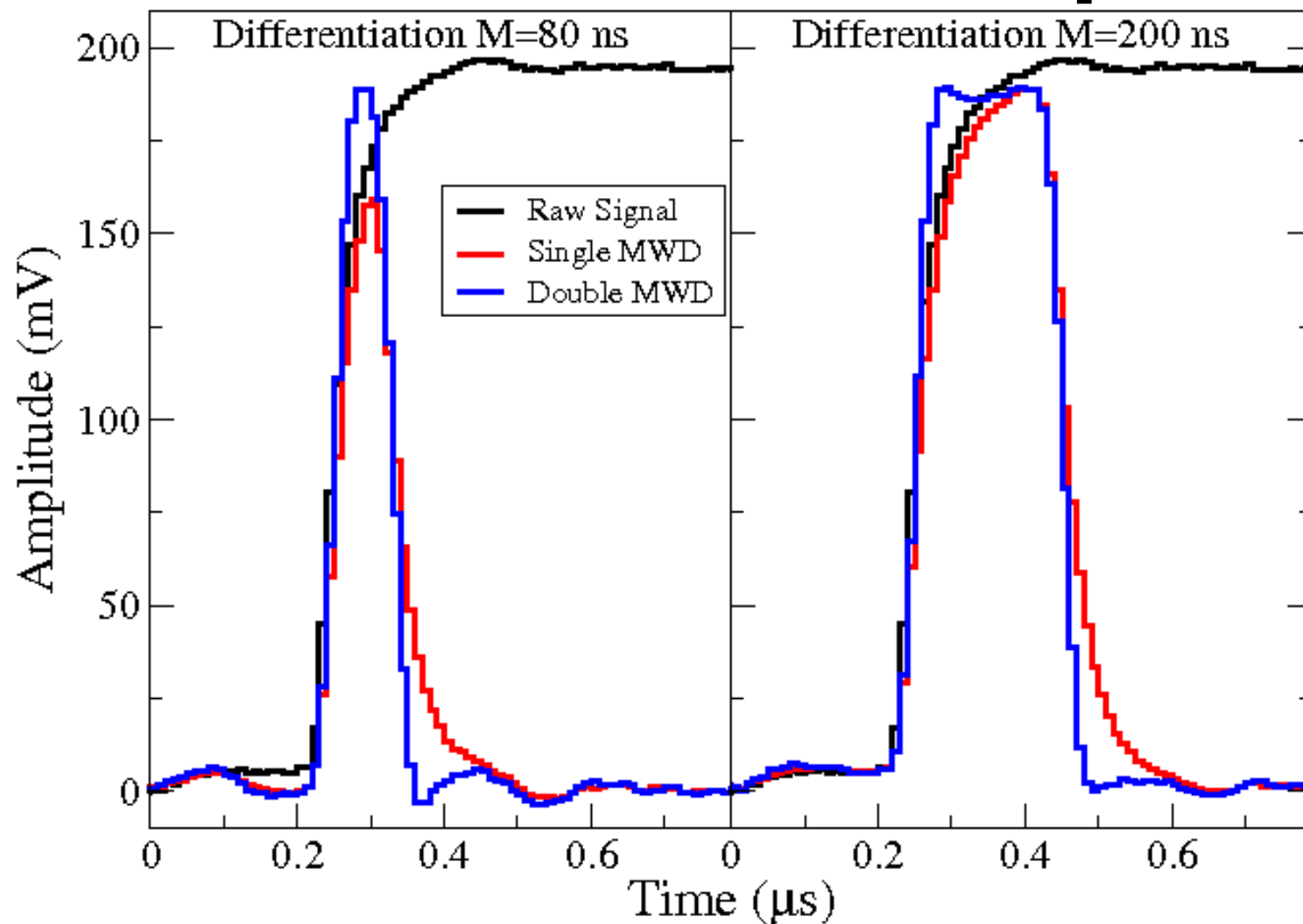
Another way of treatment:

The tail has **exponential** behaviour



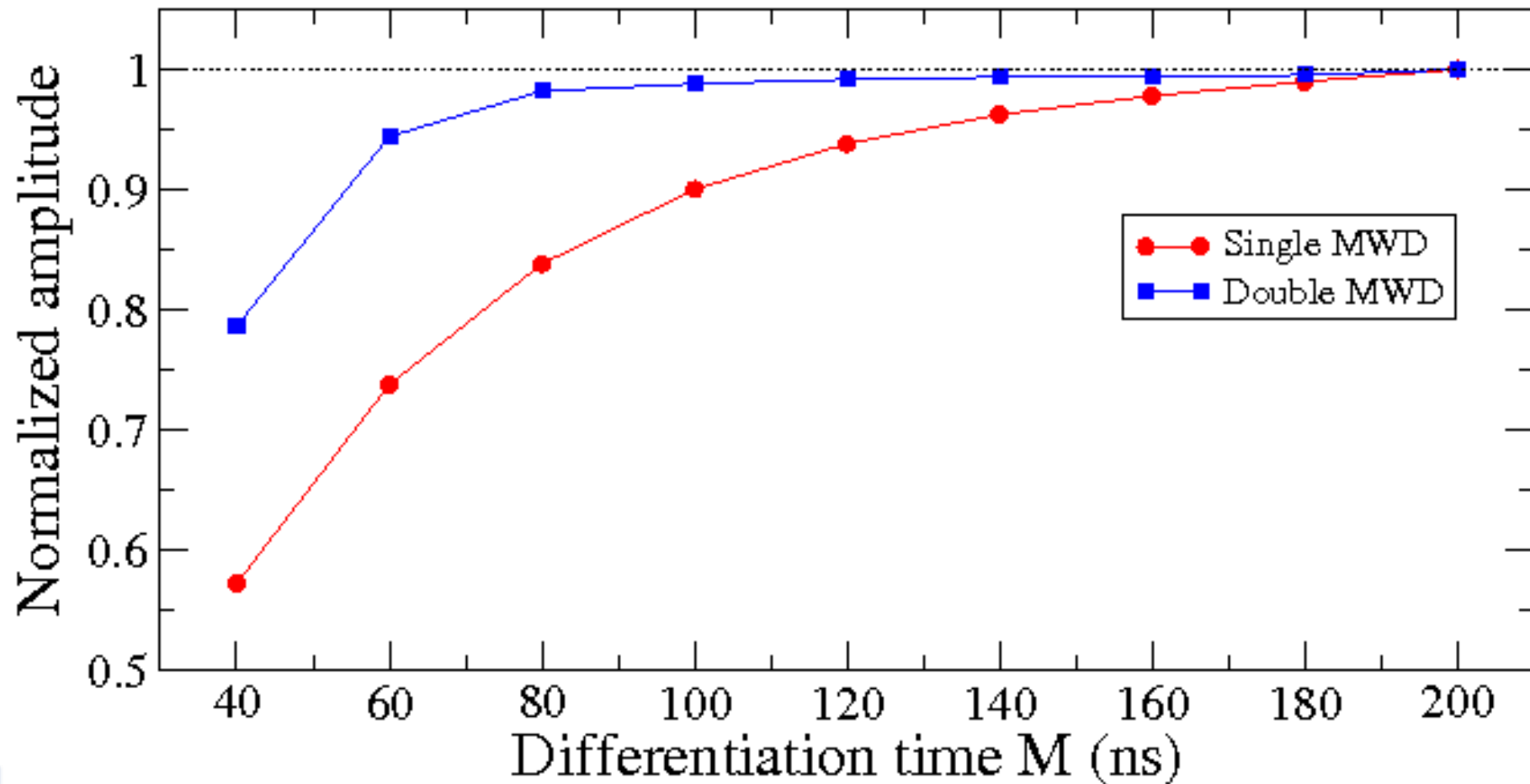
Can be corrected by additional **MWD** filter

Effect of Second MWD on the Pulse Shape



- The slow component of the signal can be compensated!
- Does this effect the pulse detection threshold and energy resolution?

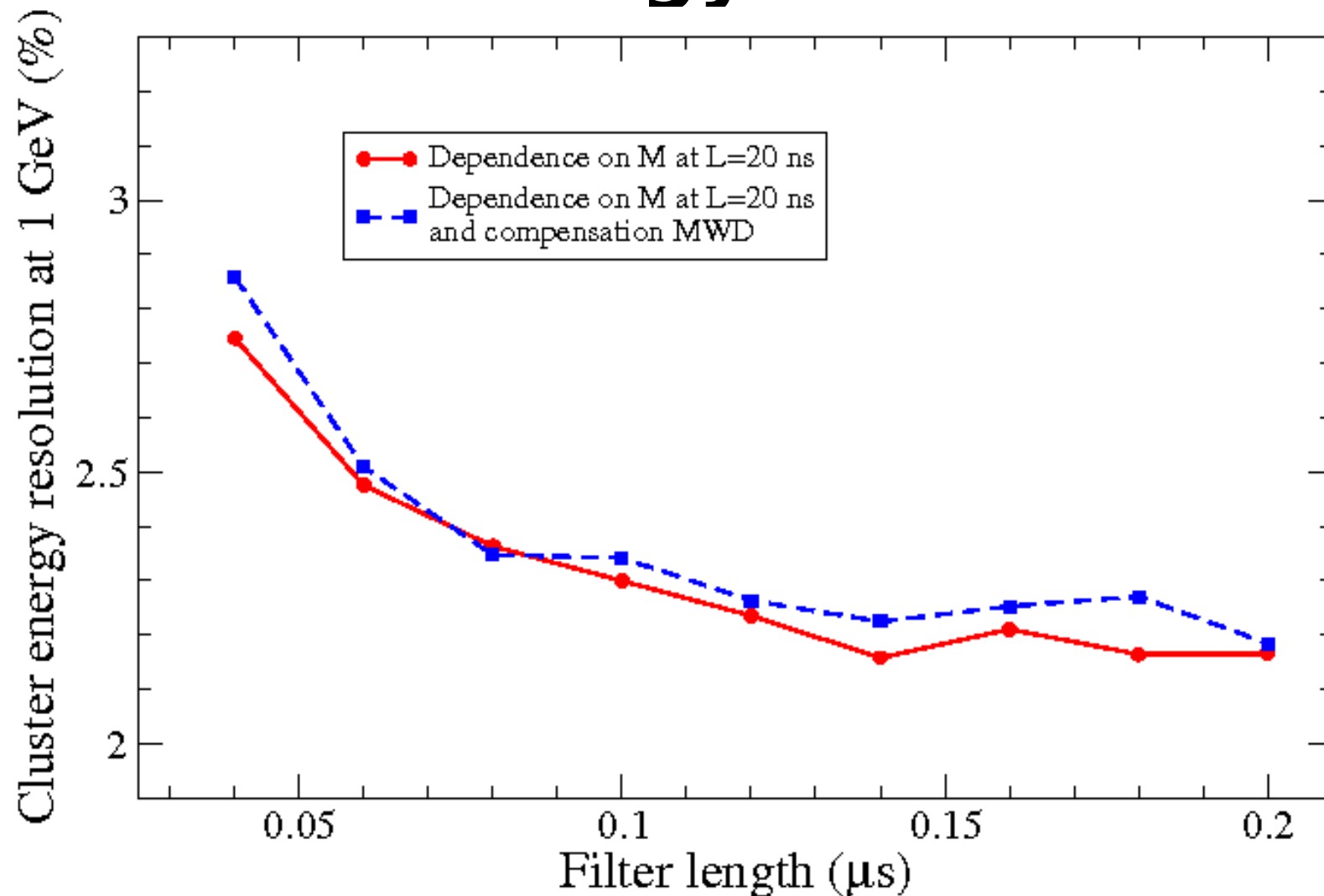
Effect of Second MWD on the Pulse Amplitude



- The noise level is not changed by the second MWD.
- Second MWD filter does allow to recover the pulse amplitude – improves effective triggering threshold



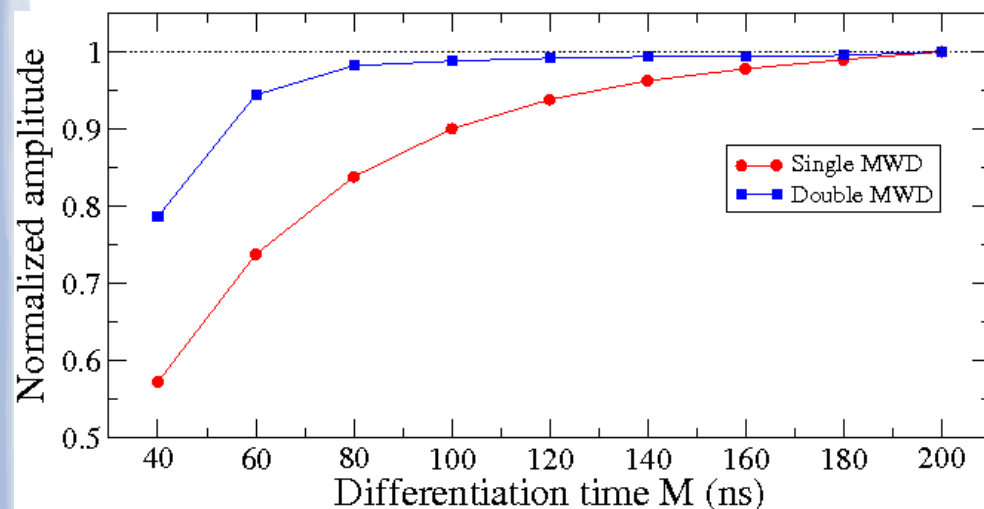
Effect of Second MWD on the Energy Resolution



- The noise level is not changed by the second MWD.
- Second MWD filter does allow to recover the pulse amplitude – improves effective triggering threshold

Effect of Second MWD on the Pile-up

(20 MHz interaction rate)

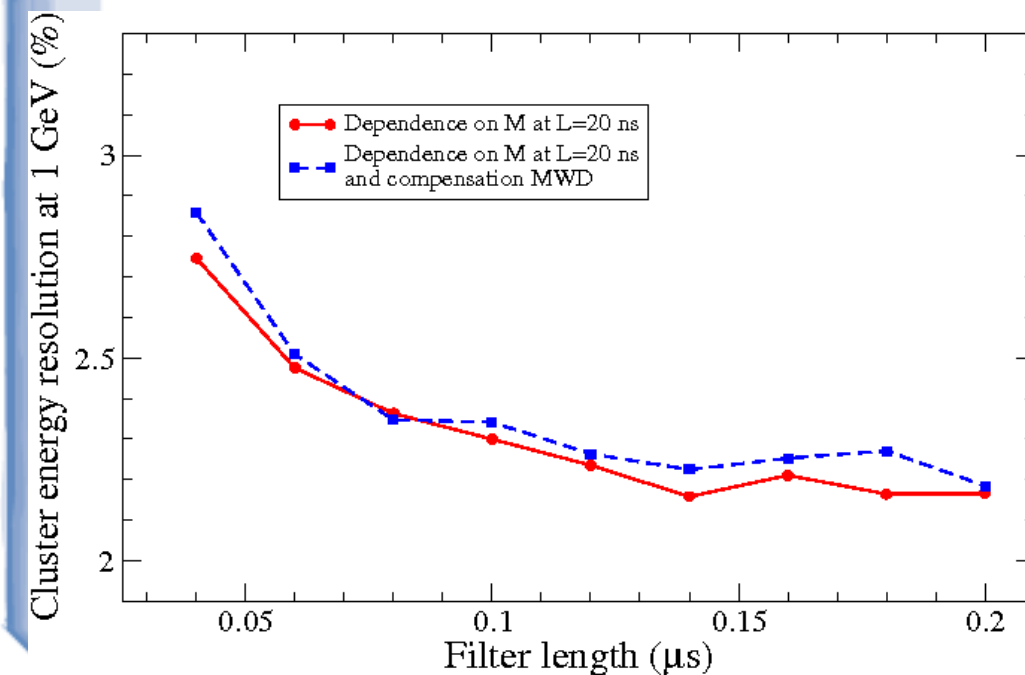


Due to the long component pulse width ~ 400 ns = 18% pile-up

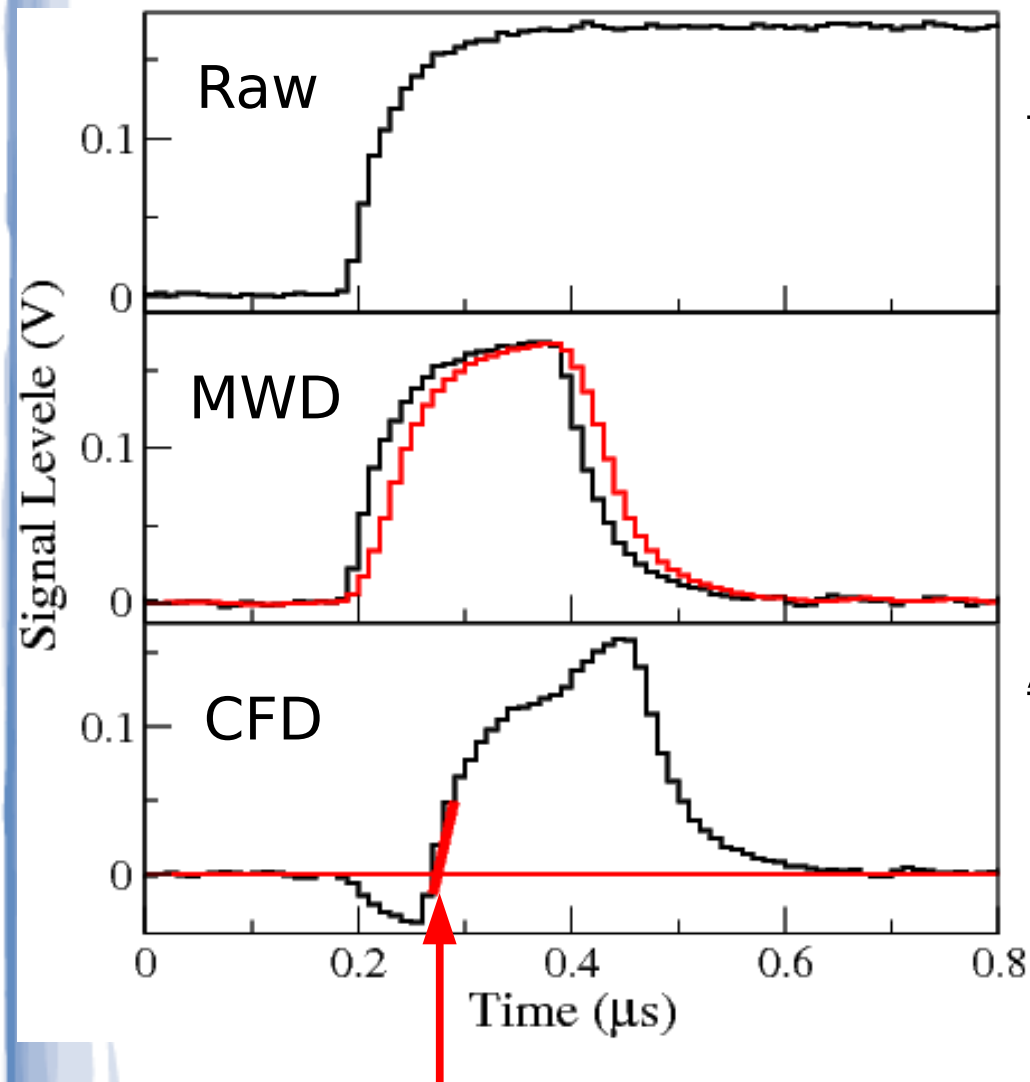
Double MWD filtering:

- M ~ 80 (60) ns
- E-res ~ 2.4 (2.5) %
- Pile-up ~ 7.8 (5.8) %
- Triggering: 98 (95) pulse amplitude restored

Additional treatment may allow to reduce effective pile-up at the cost of energy and time resolution



Pulse Processing (Precise Timing)



Time stamp: zero-crossing
(linear regression)

Precise timing:

- **more accurate** than the SADC sampling rate
- **Constant Fraction Discrimination (CFD)** is used

Analogue-like implementation:

$$CFD(n) = MWD(n-d) - R \cdot MWD(n)$$

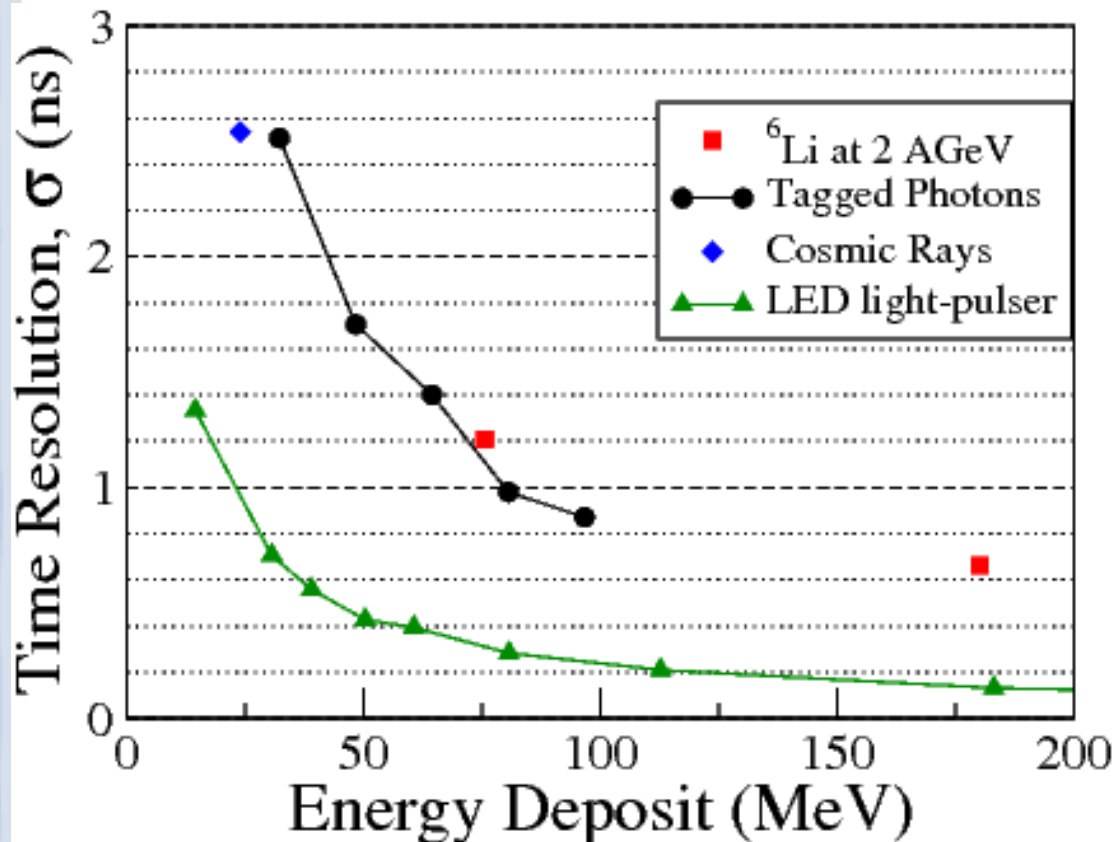
- Delay d = signal rise time
- Fraction R - to select most linear part of the signal leading edge
- ★ N - number for the linear regression
- ★ **Symmetry around zero level**



Time Resolution

(Used sampling rate 100/50 MHz)

Time resolution as a function
of energy deposit



Limiting factor:

- Long rise time of the signal ~ 70 ns (LED light-pulser rise-time ~ 10 ns)

It is possible to achieve time resolution much ($\times 20$) higher than SADC sampling rate

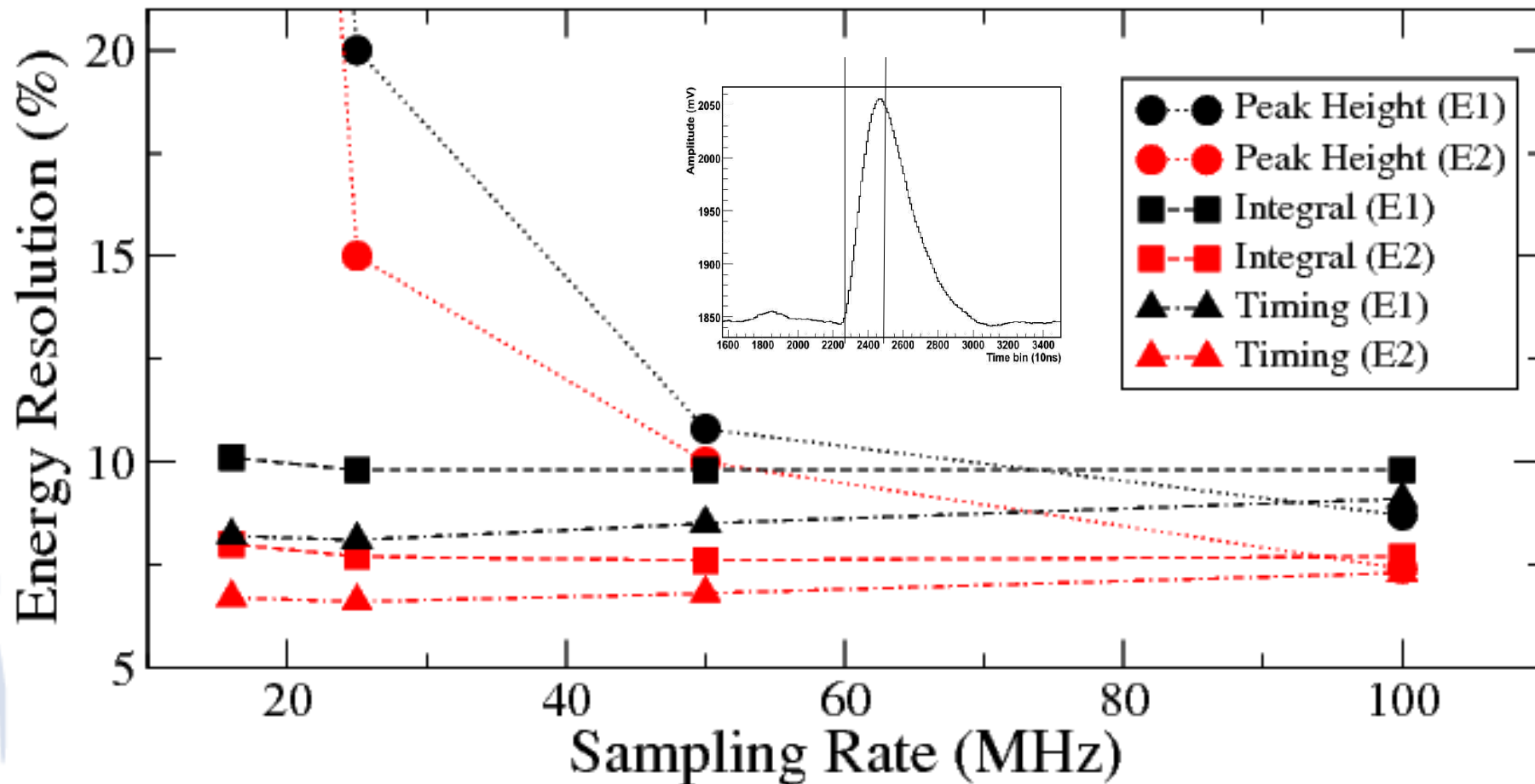
An dedicated measurement with PROTO60 is done last week \rightarrow more precise test



Time Resolution

(Used to measure pulse height)

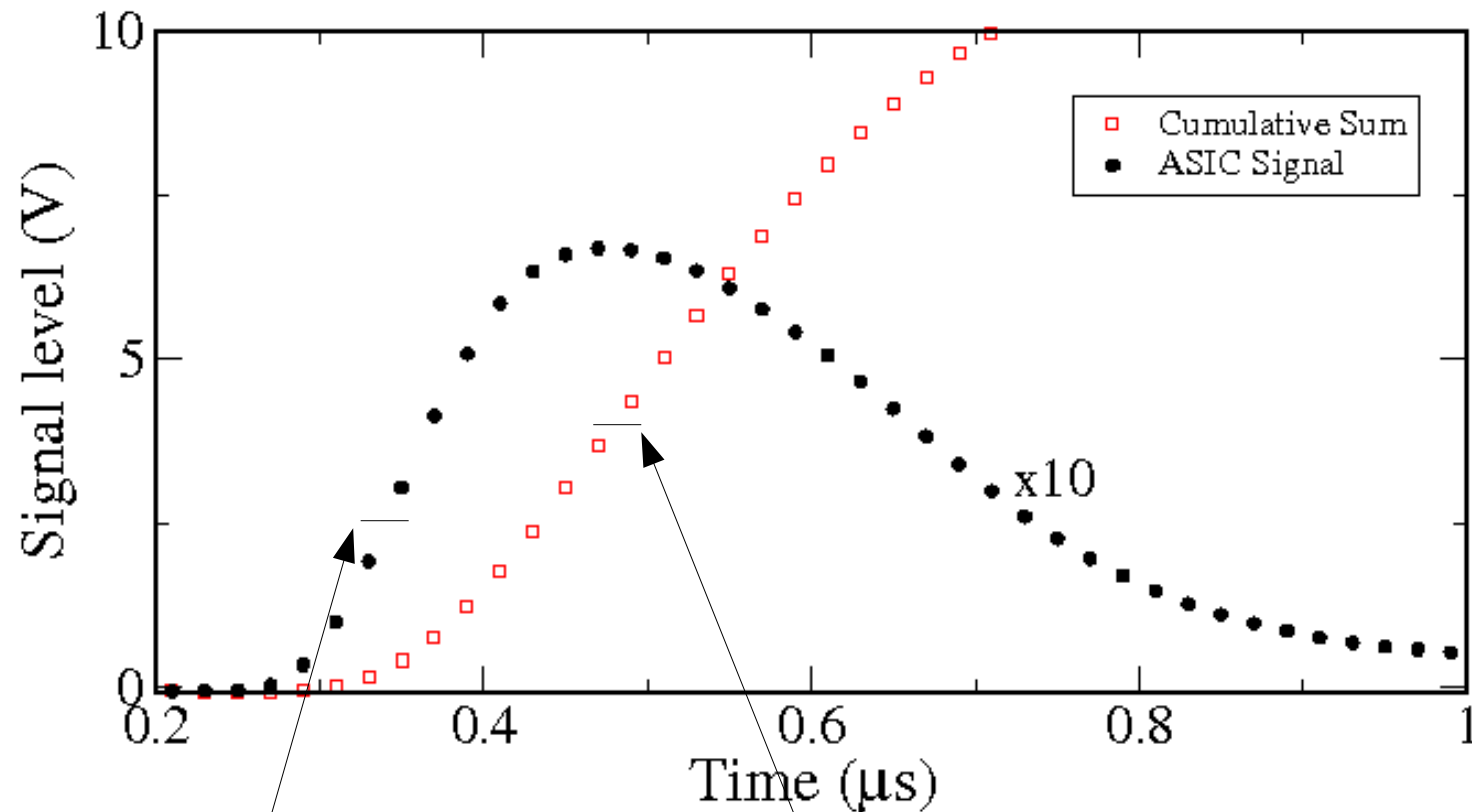
Extraction of the energy information from the digitized pulse:
(Energy resolution as a function of SADC sampling rate)



Time Resolution

Used to measure pulse height

Method explanation

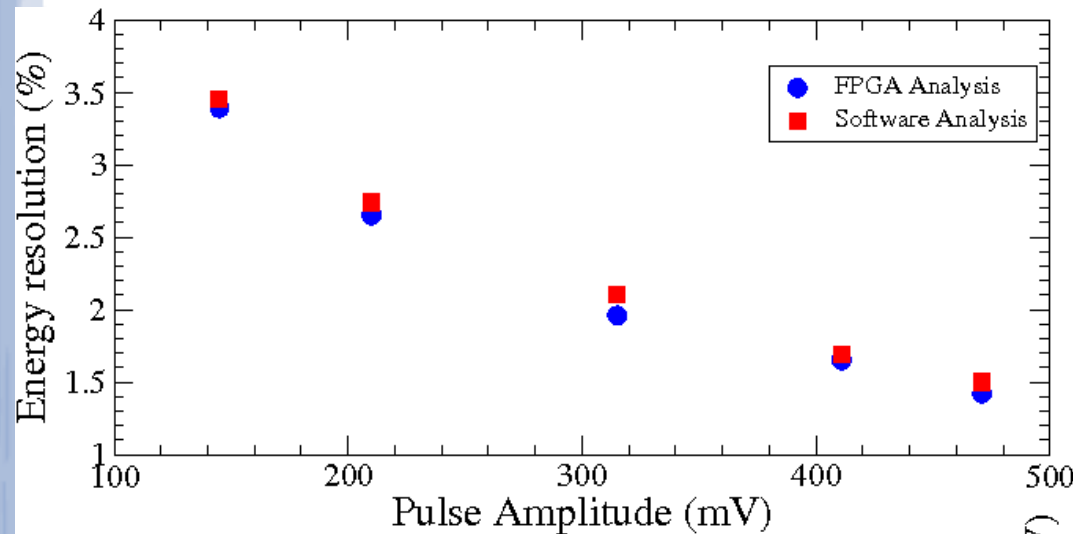


Fraction known from
the CFD method

The **Fraction** (from CFD)
used for linear interpolation
of the cumulative sum



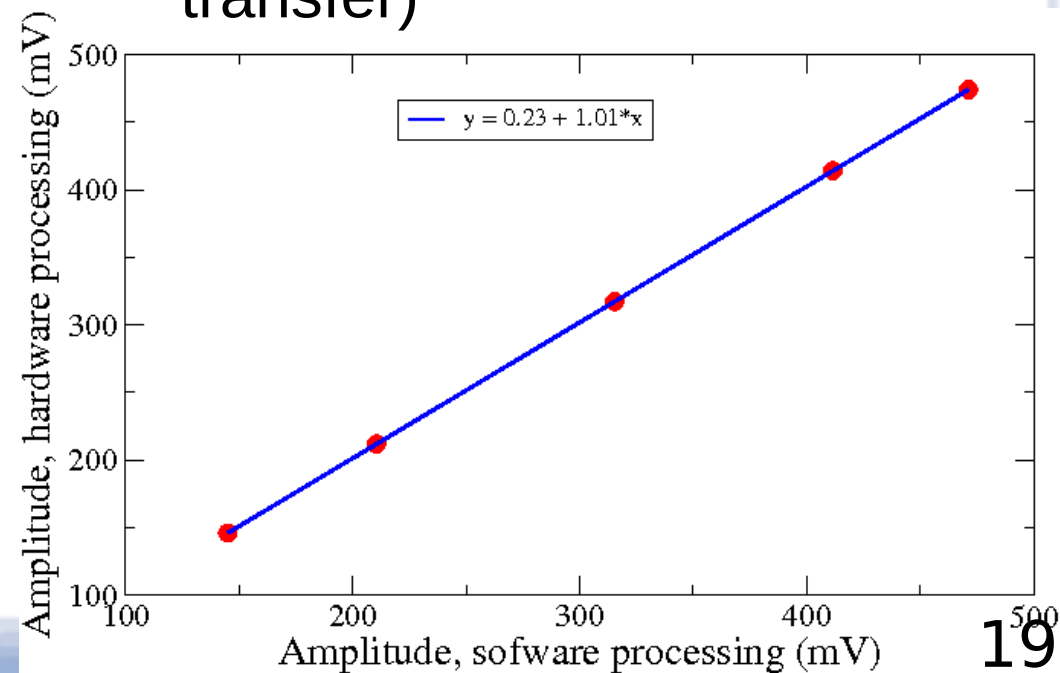
Energy



The VHDL implementation is working.

Next step – port to existing SADC
(in progress)

- Data taken with LED light-pulser
- Measurements done with 100 MHz 16 bit SADC
- Analysis performed in:
 - Software
 - Hardware (Xilins Spartan FPGA demo board, serial data transfer)

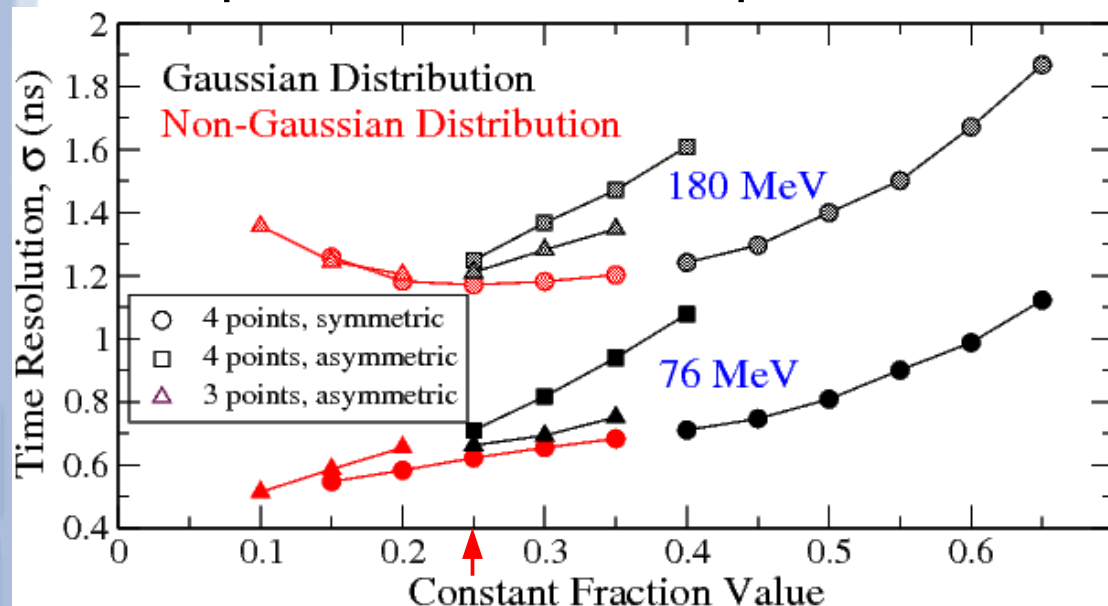




- Digital filtering allows to accept higher rates for the EMC end-cap
 - The performance of the analogue shaper has to be investigated
- The “digital CFD” produces time stamps with much higher precision than SADC sampling rate
- The precise timing allows precise measurement of the pulse amplitude at lower sampling rate
- The VHDL implementation of presented feature-extraction algorithms is ready
- Development of simple pile-up correction algorithms is in advanced stage

Timing (Parameters Tuning)

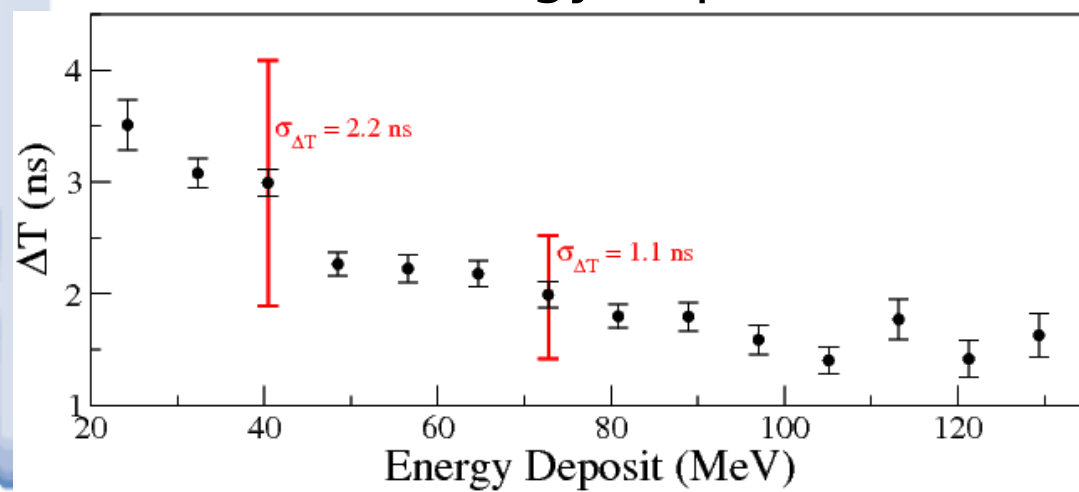
Dependence on the parameters



Best results achieved for:

- $R=1/4$ (easy to implement in FPGA)
- 3-point linear regression

Time-stamp position dependence on energy deposit



Digital implementation of CFD is not completely free from the “Walk” effect – can be corrected in the analysis