Beitrag ID: **7** Typ: **nicht angegeben**

High-Resolution 32 Channel TDC (< 10 ps RMS) Implemented in a FPGA.

Donnerstag, 15. April 2010 09:00 (30 Minuten)

Time to Digital Converters (TDCs) are widely used in many scientific applications. At GSI high-resolution ASIC-TDCs and commercial modules will be utilized in Time-of-Flight detectors for the upcoming FAIR experiments. The time-stretching methods used in high-resolution applications, e.g. the Vernier and the tapped delay lines (TDL) method, have also been successfully implemented in FPGA-Technology. The best recently known implementation achieves a RMS of 10 picoseconds (ps) with a reduced number of channels and an increased dead time in an Altera-FPGA.
The advantage of a FPGA implementation is the less expensive and less time consuming design process as well as the flexibility and adaptability of the FPGA-TDC design to special needs of the current application. These facts motivated us to explore the achievable performance of a TDC implementation in a FPGA.
We implemented a 32-channel, low dead time TDC based on the TDL method in a Virtex-4 FPGA. In this method standard chain structures in a FPGA –the carry chains –are used as a delay chain for time stretching purposes. The achievable time-resolution of the interpolation is determined by the intrinsic delay of a cell in the chain. In our implementation we used special techniques to improve the time resolution of the TDC beyond its cell delay.
The TDC was tested by measuring the time between rising edges of the original and the delayed signal on different TDC channels. We measured delays in the range from 40 ps to 1 us. At small delays 9 ps RMS was achieved, additional 2 ps were induced by the limited accuracy of the system clock at 1 us delay. Thus the achieved resolution of a TDC channel is 6 ps ($9/\sqrt{2}$).
Additional measurements were performed to characterize the influence of the temperature and supply voltage variations on the measured RMS value. The results of these measurements and the architecture of the FPGA-TDC will be presented.

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Sitzung Einordnung: FEE Development II

Track Klassifizierung: Front End Electronics