PANDA FEE/DAQ Workshop

Sezione di Torino

MVD silicon pixel detector : readout architecture and ASIC developments

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PANDA MVD

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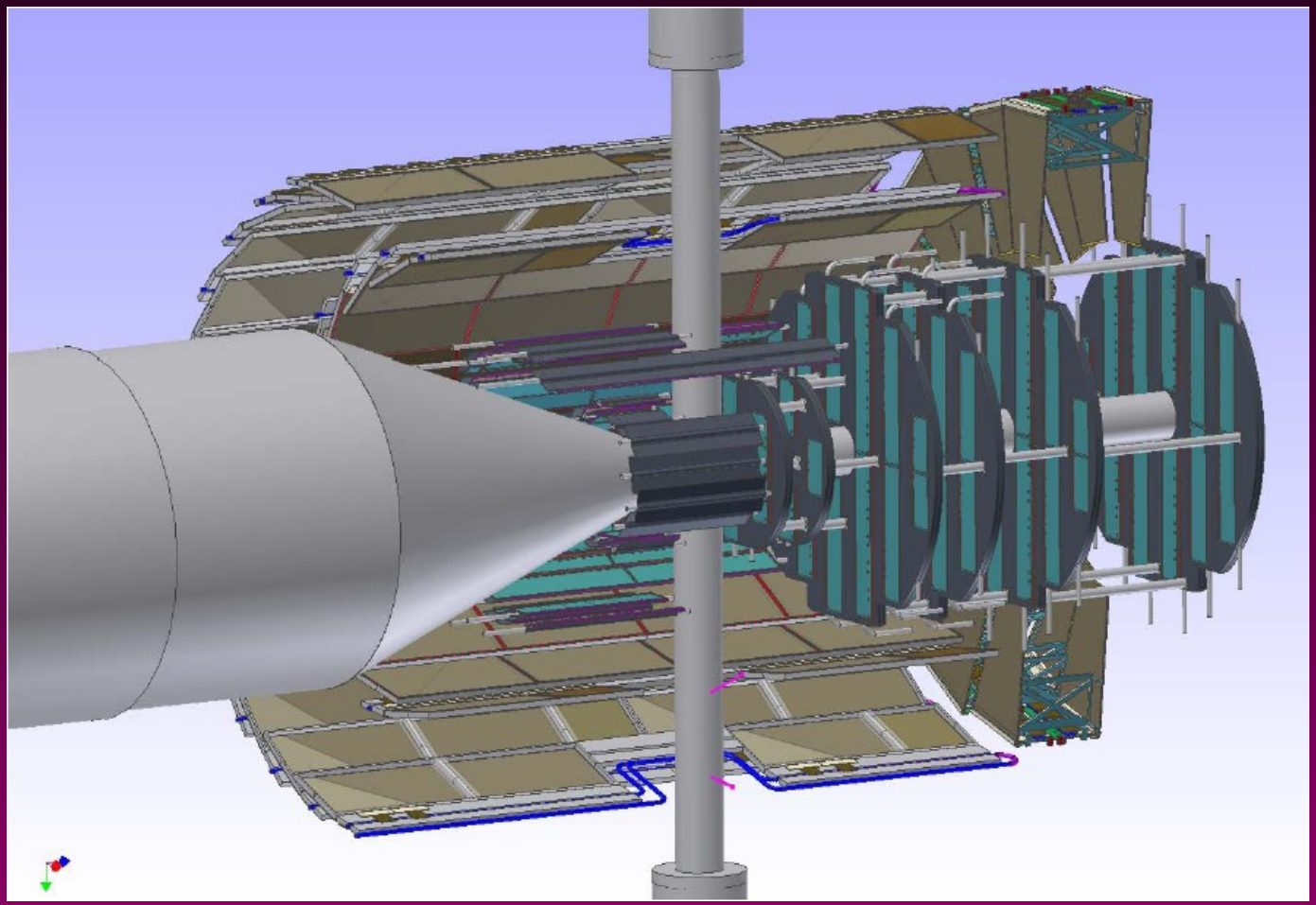

- Barrel :

  Layer 1 : radius 28 mm, SPDs

  Layer 2 : radius 53 mm, SPDs

  Layer 3 : radius 92 mm, SSDs

  Layer 4 : radius 120 mm, SSDs

- Forward :

  Disks 1-2 : radius 37.5 mm, SPDs

  Disks 3-4 : radius 75 mm, SPDs

  Disks 5-6 : radius 130 mm, SPDs + SSDs

Pixel specs

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Pixel size	*100 × 100 μm^2*
Chip active area	*11.4 × 11.6 mm^2 (116 rows, 110 cols)*
dE/dx measurement	*ToT, 12 bits dynamic range*
Max input charge	*50 fC*
Noise floor	*<32 aC (200 e^-)*
Clock frequency	*155 MHz*
Time resolution	*6.4 ns (1.85 ns r.m.s.)*
Power consumption	*< 500 mW/cm^2*
Max event rate	*$6.1 \cdot 10^6$ hits/($cm^2 \cdot s$)*
Total ionizing dose	*< 100 kGy*

Data rates

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antiproton-	*proton*	*Ar*	*Au*
Average flux [hits/cm^2·s] *Disk number*	*8.24·10^5* *Disk 6*	*3.30·10^5* *Disk 5*	*9.47·10^4* *Disk 4*
Average flux [hits/cm^2·s] *Barrel 1 - stave*		*2.55·10^5* *stave 3*	*1.03·10^5* *stave 13*
Average flux [hits/cm^2·s] *Barrel 2 - stave*		*2.55·10^5* *stave 19*	*2.54·10^4* *stave 25*
Max flux [hits/cm^2·s] *[hits/(readout chips·s)]*	*8.24·10^6* *~8.1·10^6*	*6.8·10^5* *~9·10^5*	*1.65·10^4* *~2.18·10^4*

p : $2 \cdot 10^{32}$
Ar : $2.4 \cdot 10^{31}$
Au : $2.2 \cdot 10^{30}$

annh. rate $2 \cdot 10^7$
@ 15 GeV/c

Routing direction

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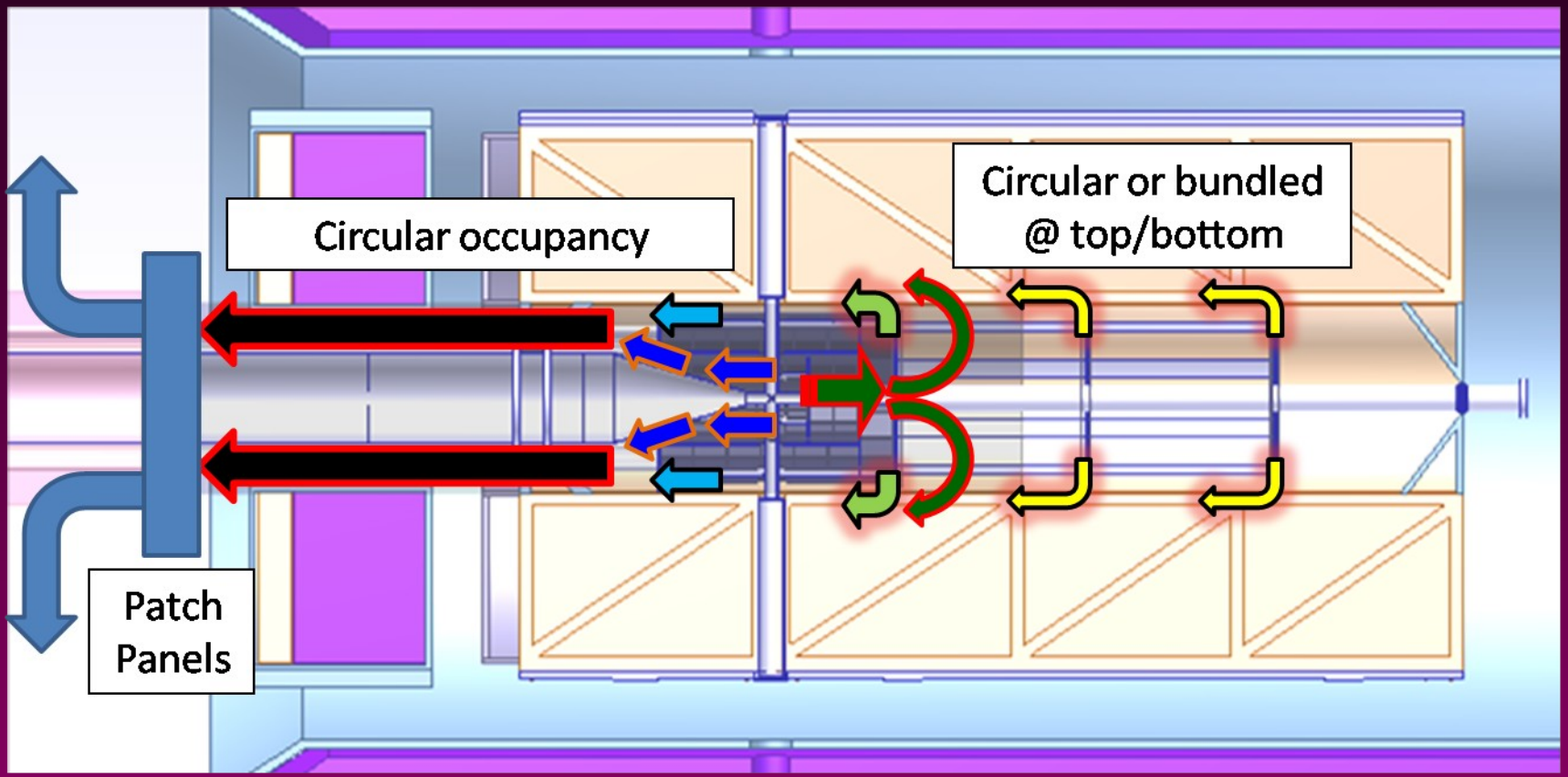

Module concept

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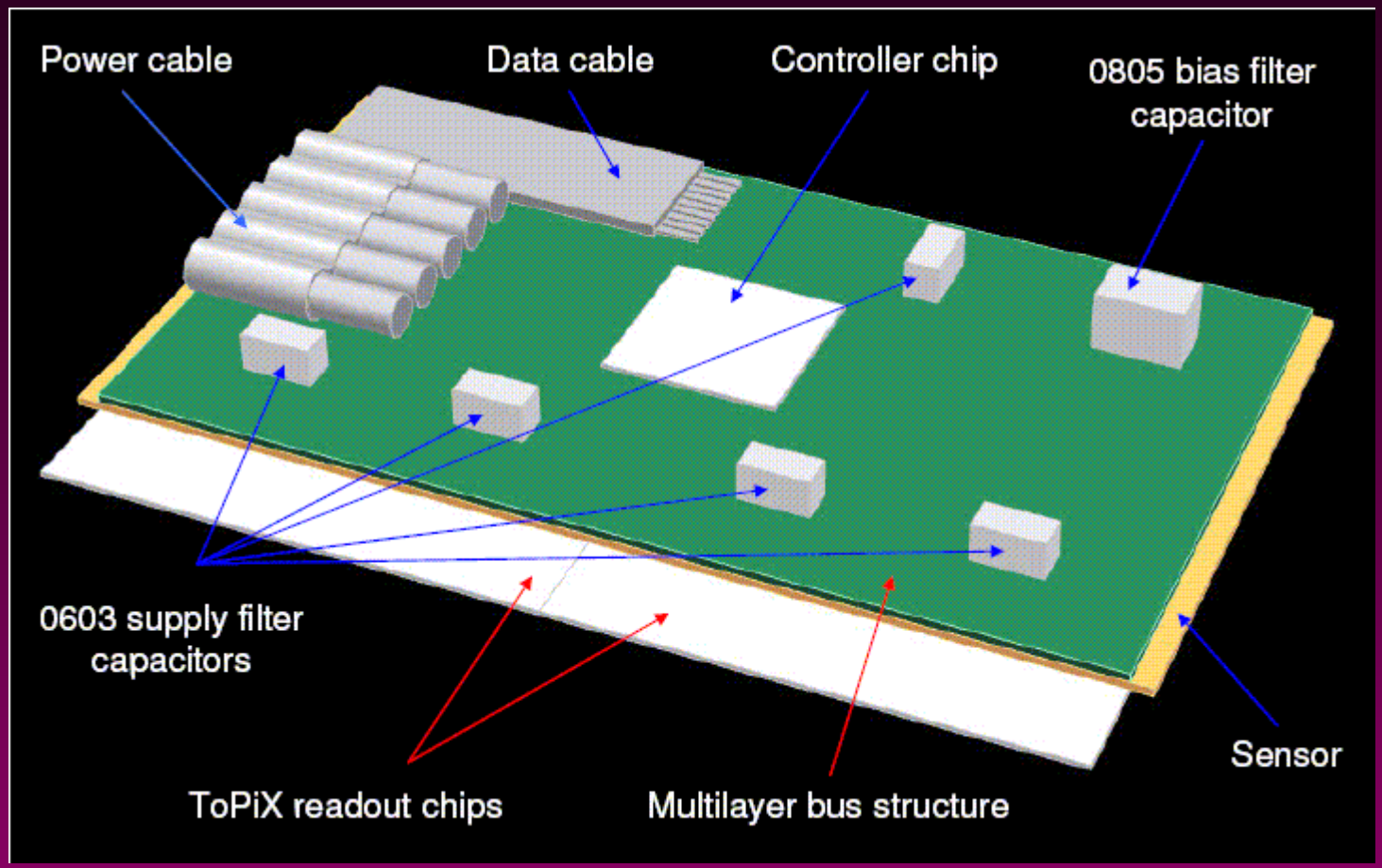

Module types

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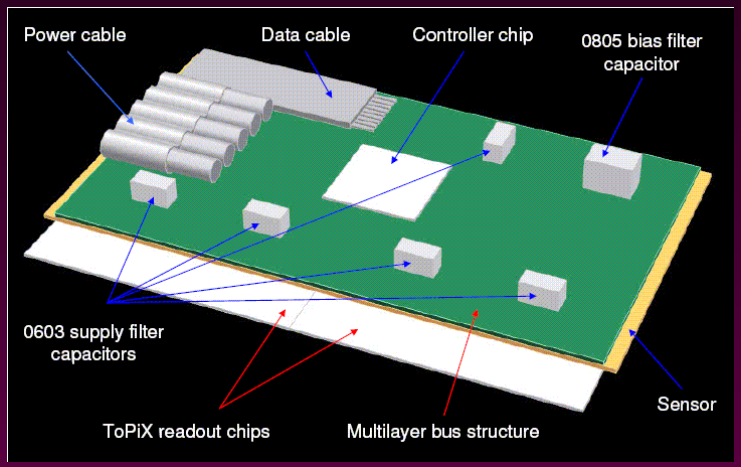

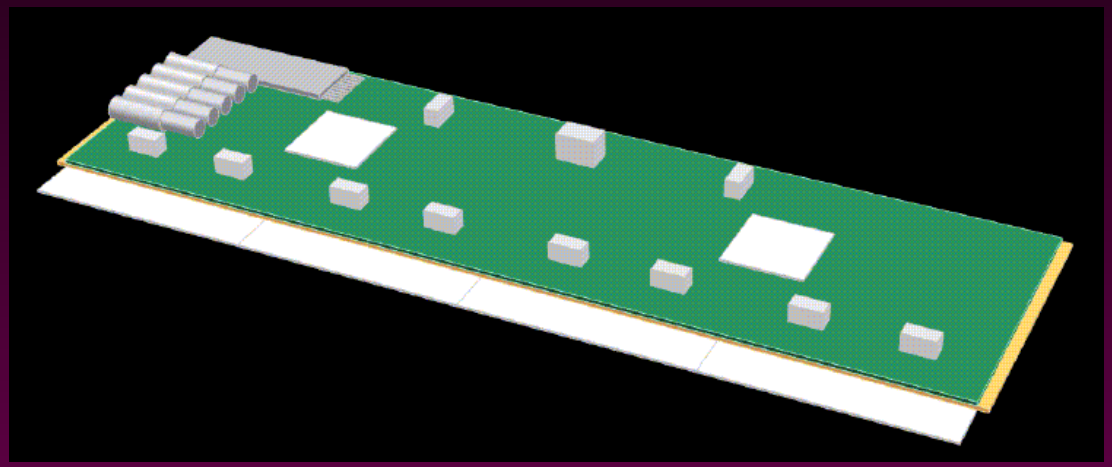

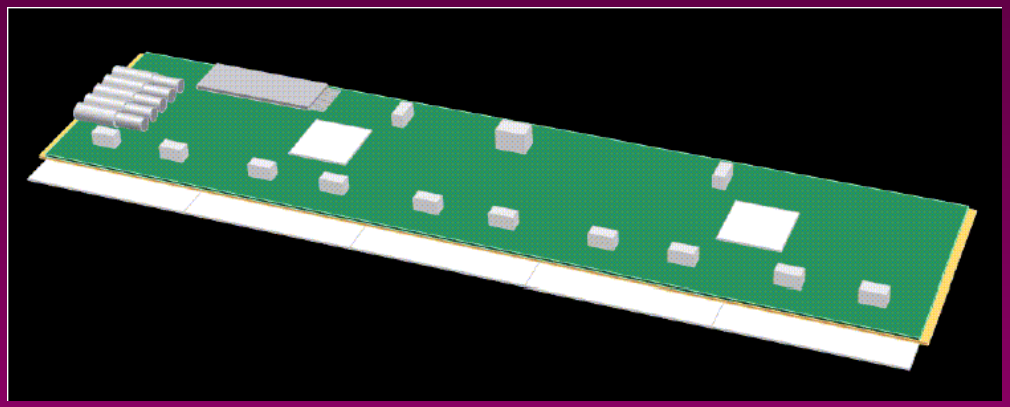

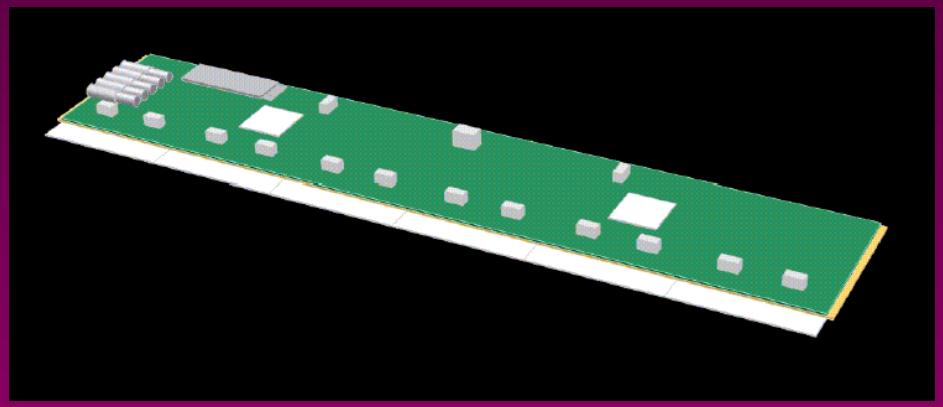

Readout scheme

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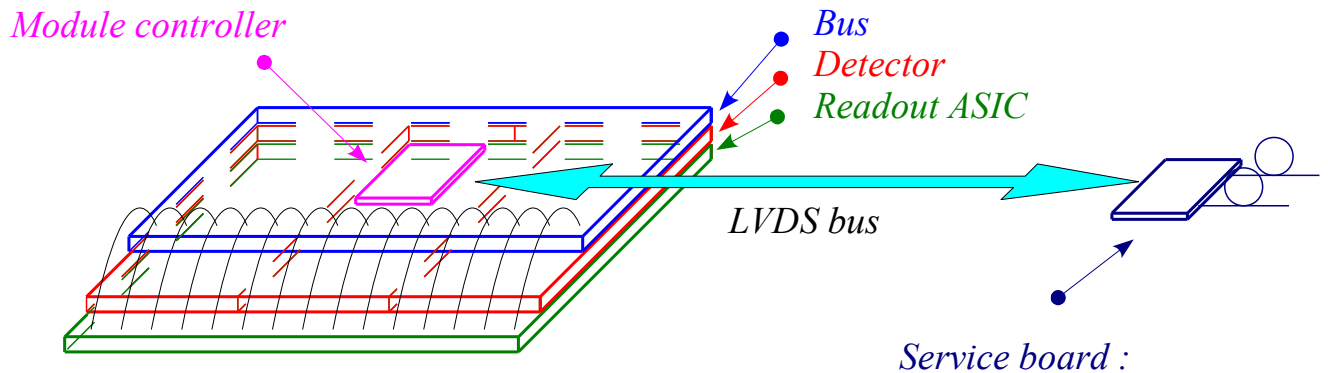
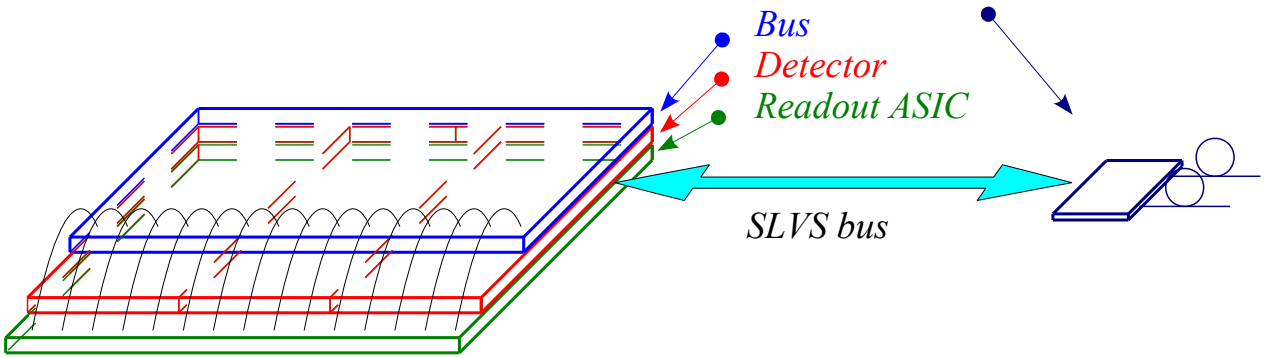


Option 1



Option 2

Readout options

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- Option 1
  - ☺ reduced number of cables
  - ☺ simpler ToPiX control logic
  - ☺ better management of data rate increase
  - ☹ requires an extra chip
- Option 2
  - ☺ no need of an extra chip
  - ☺ interface already under development at CERN
  - ☹ more cables

ToPiX ASIC

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- Custom development for the PANDA MVD
- Provides spatial and time coordinates plus energy resolution measurement (via ToT)
- Compatible either with p-type or n-type detectors
- Self triggered architecture
- Each event has a 12 bits time reference
- Data corresponding to a 12 bits counter cycle (26.21 μs) are packed in a frame, with an 8 bits frame counter (6.71 ms cycle)

Pixel cell

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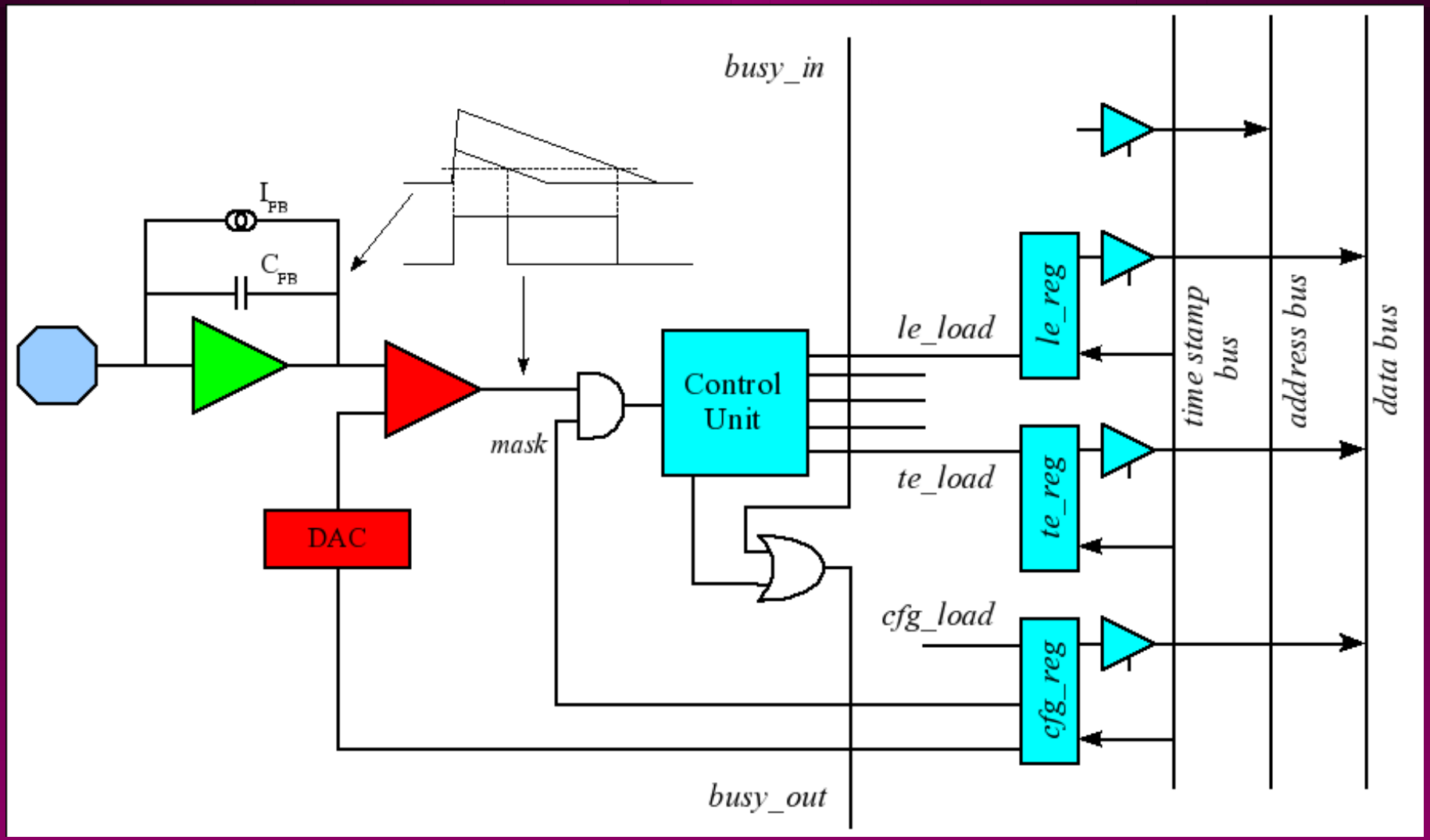

ToPiX block diagram

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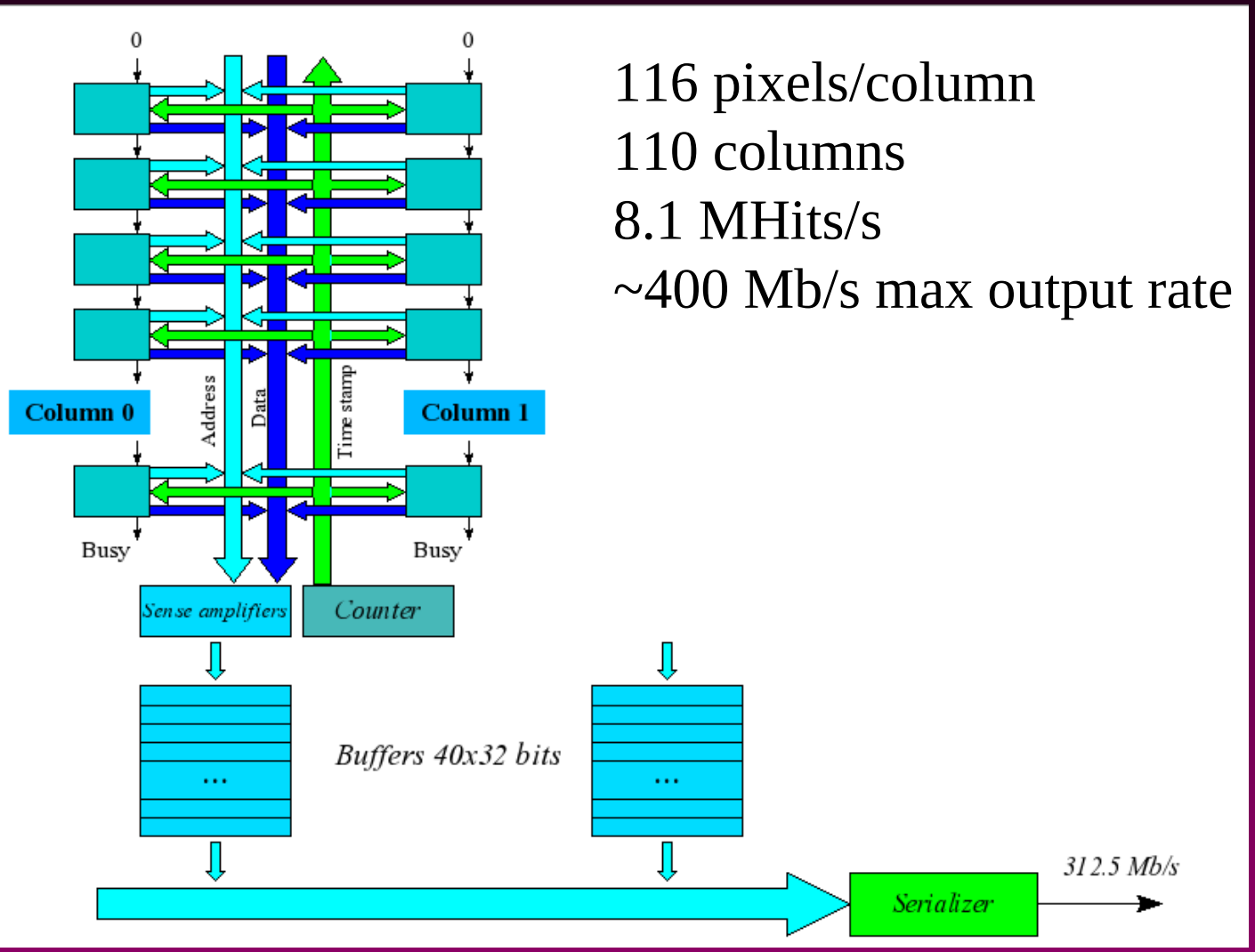

116 pixels/column
110 columns
8.1 MHits/s
~400 Mb/s max output rate

Data format

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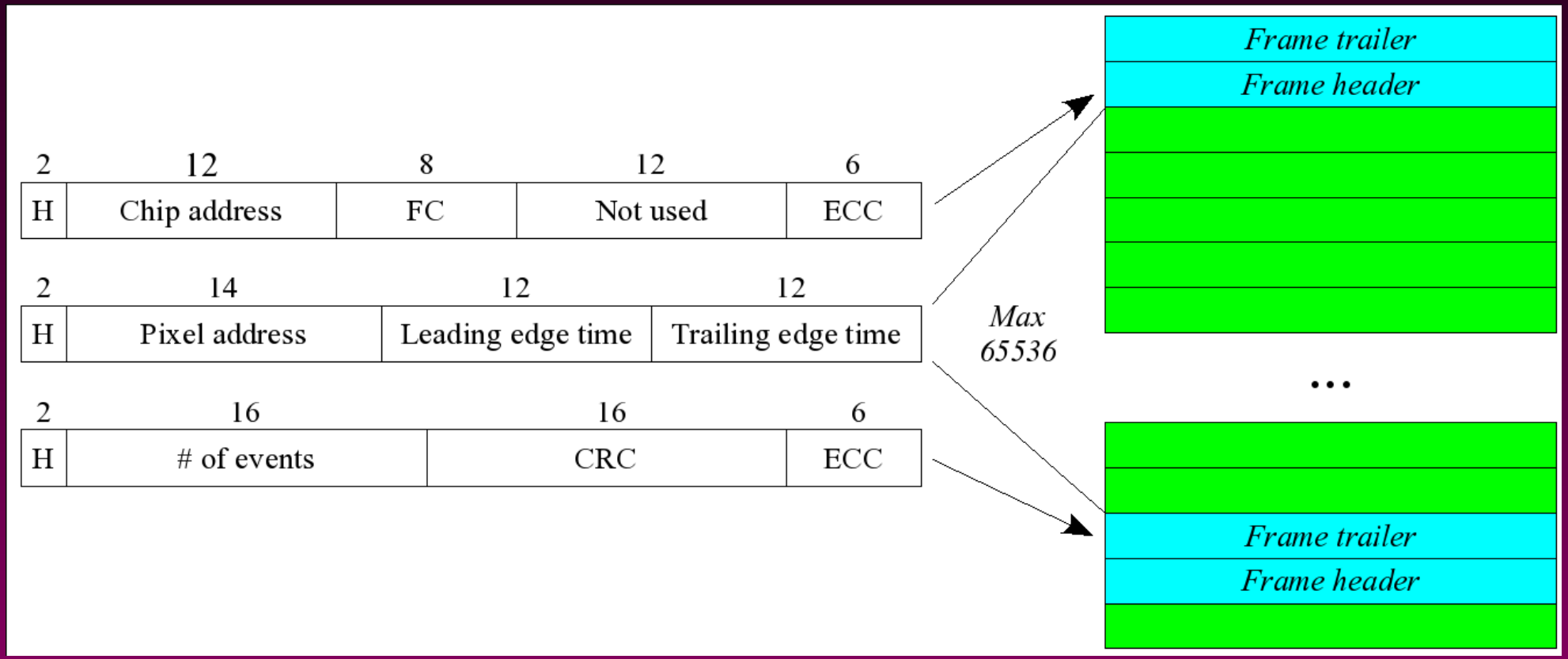

ToPiX v2 architecture

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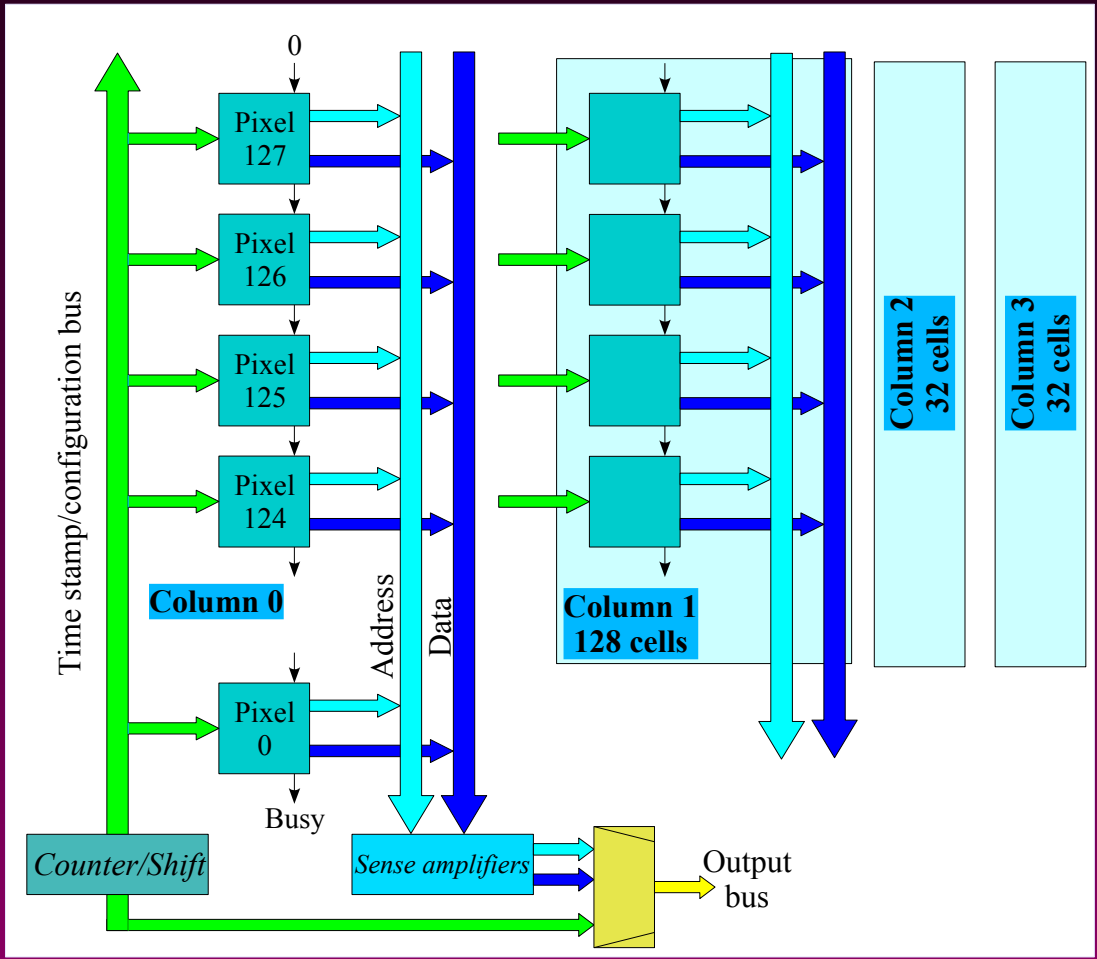

- Full pixel cell (analogue + digital)
- Two folded columns with 128 cells
- Two columns with 32 cells
- 5x2 mm^2 die area
- CMOS 0.13 µm technology
- SEU tolerant logic (based on the DICE cell)

ToPiX v2

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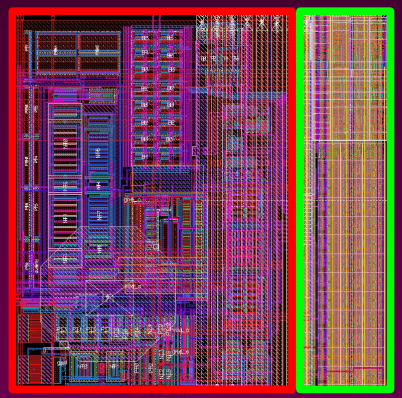
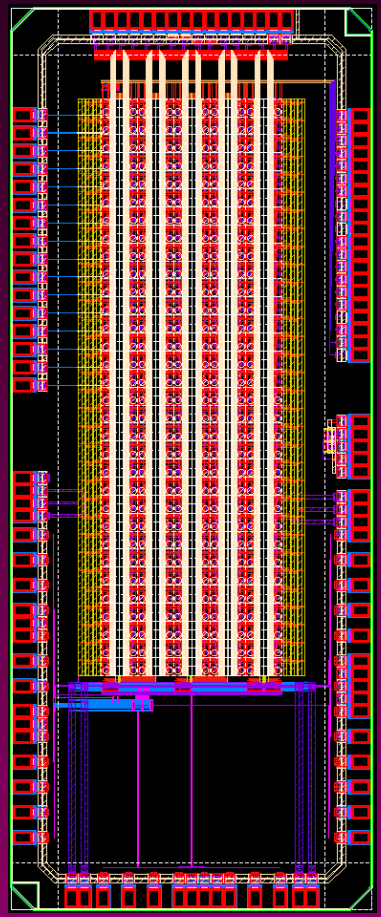
Pixel cell

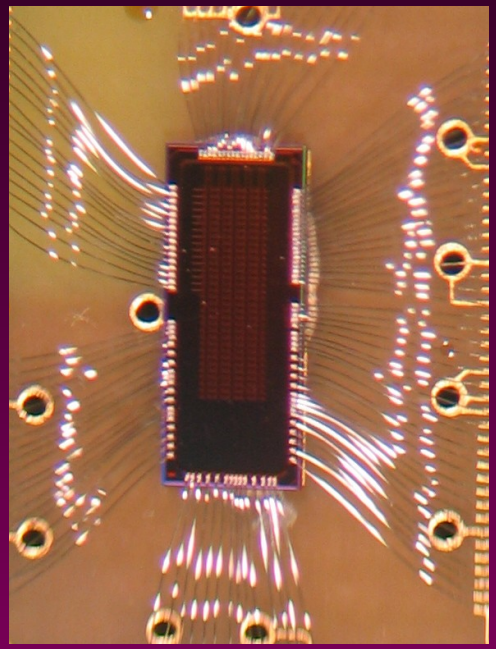
100 μm × 100 μm



Analog *Digital*

ToPiX prototype 5 mm × 2 mm





ToPiX v2

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Tests :

- electrical
- connected to a detector via wire bonding
- TID tests
- SEU tests

References :

D. Calvo et al, *A Silicon Pixel Readout ASIC in CMOS 0.13 µm for the PANDA MicroVertex Detector* , Nuclear Science Symposium Conference Record, 2008 IEEE, 19-25 Oct. 2008 Page(s): 2934 – 2939

D. Calvo et al., *The silicon pixel system for the Micro Vertex Detector of the PANDA experiment* – doi:10.1016/j.nima.2009.09.043

T. Kugathasan, et al., *Front end electronics for pixel detector of the PANDA MVD* - Proceedings of the Topical Workshop on Electronics for Particle Physics 21-25 Sep 2009 - Paris, France - CERN 2009-006, pag. 52-56

ToPiX v3

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- Under design
- 5x4 mm^2 die area
- CMOS 0.13 μm DM technology
  - LM → 6 thin, 2 thick metal layers
  - DM → 3 thin, 2 thick, 3 RF metal layers
- Triple redundancy-based SEU protection
- End of column logic
- 312.5 Mb/s serial output
- Pads for bump bonding

Analog cell

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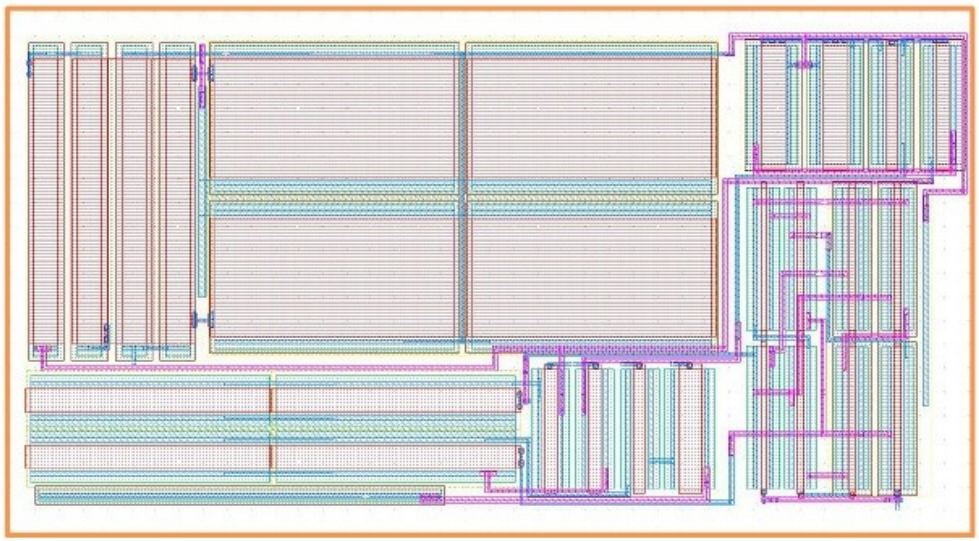
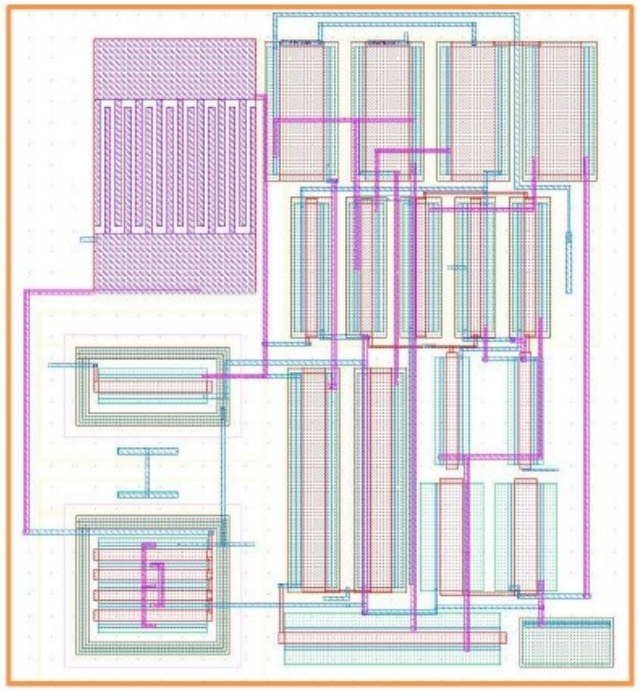
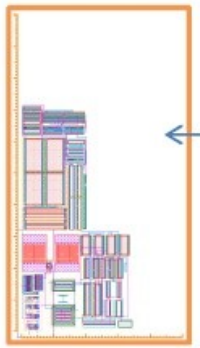
Filter stage: 40µm x 20µm (50% of area of the previous)



Preamplifier 35µm x 30µm



Analog Cell 100µm x 50µm



← To be designed

Digital cell

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Cell type	Cell size	Comments
Dice	$6 \times 7\ \mu m^2$	ToPiX v2
Triple redundancy	$7 \times 9.6\ \mu m^2$	ToPiX v3 data register
Triple redundancy with self correction	$9 \times 14.4\ \mu m^2$	ToPiX v3 control register

Digital readout

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- Common buses for two pixel columns
- Time stamp distribution @ 155 MHz
- Pixel readout @ $f_{CK}/4$
- Column bus circuitry already designed for the NA62 prototype, currently under test
- End of column control logic design started
- Submission foreseen for November 2010

GBT chipset

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Radiation tolerant chipset :

- GBTIA : Transimpedance optical receiver
- GBLD : Laser driver
- GBTx : Data and Timing Transceiver
- GBT-SCA : Slow control ASIC

Target Applications :

- Data readout
- TTC
- Slow control and monitoring links

Supports :

- Bidirectional data transmission
- Bandwidth :
  - → Line rate : 4.8 Gb/s
  - → Effective : 3.36 Gb/s

Radiation Tolerance :

- Total dose
- Single Event Upset

GBT

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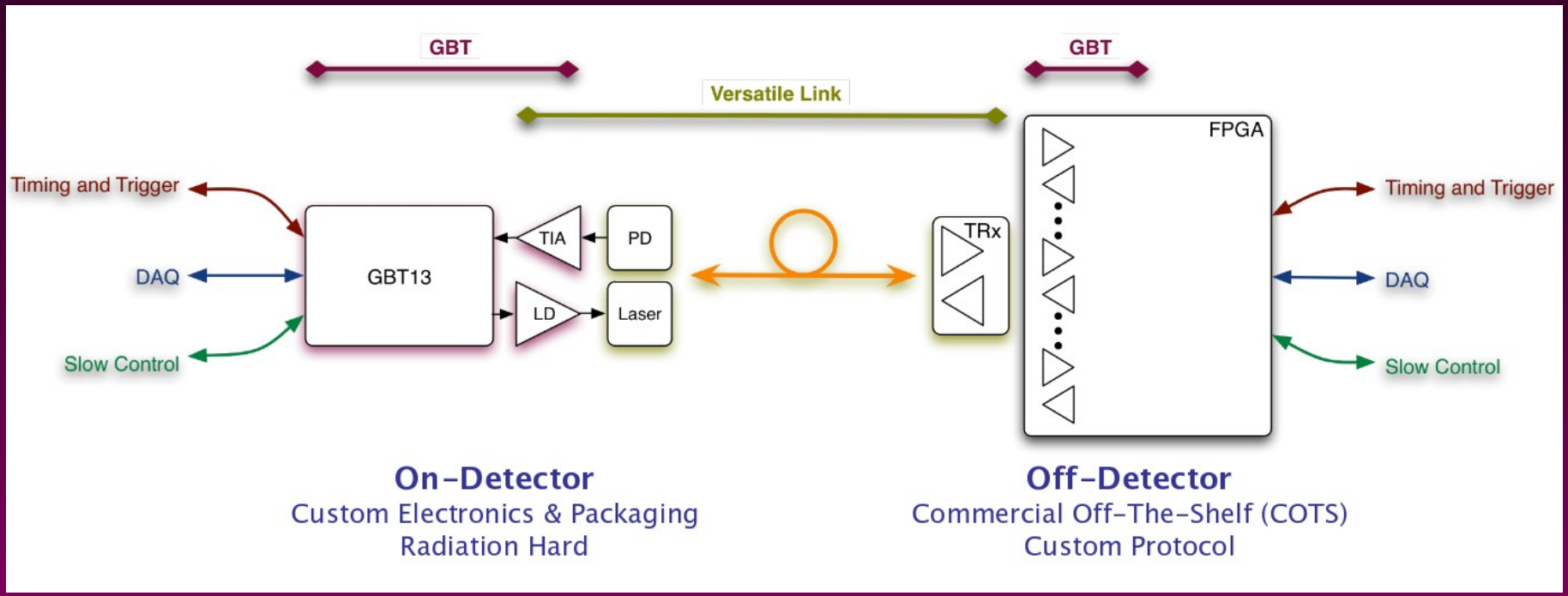

Conclusions

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- A pixel readout architecture has been defined – waits for more detailed rate simulations to be finalized.
- F/E ASIC with full pixel cells and columns has been designed and tested – new version, with full end of column logic is under design.
- A GBT-based interface to the DAQ system is under evaluation. Contacts with the CERN GBT group ongoing.