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**Report of Contributions**

Contribution ID: 0

Type: **not specified**

# **Application of Forth CPU for control and debugging of FPGA-implemented systems**

*Sunday, 26 May 2019 08:00 (1 minute)*

**Presenter:** ZABOLOTNY, Wojciech (Warsaw University of Technology(WUT))

Contribution ID: 1

Type: **not specified**

## **Automatic management of local bus address space in complex FPGA-implemented hierarchical systems**

*Sunday, 26 May 2019 08:01 (1 minute)*

**Presenter:** ZABOLOTNY, Wojciech (Warsaw University of Technology(WUT))