# Application of Forth CPU for control and debugging of FPGA-implemented systems

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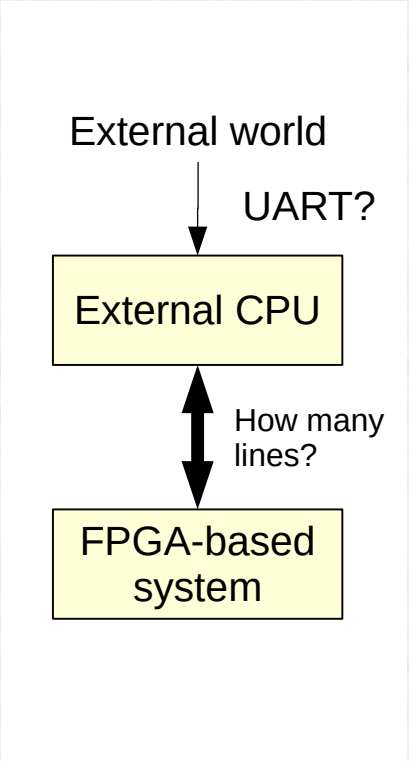
- Those tasks may be done from external computer via control interface, e.g., IPbus
- However, in case if we need an autonomous initialization of our system, the local CPU may be needed

# Local CPU

- The easiest method to solve that problem is to connect an external CPU (e.g., a simple and cheap ARM)



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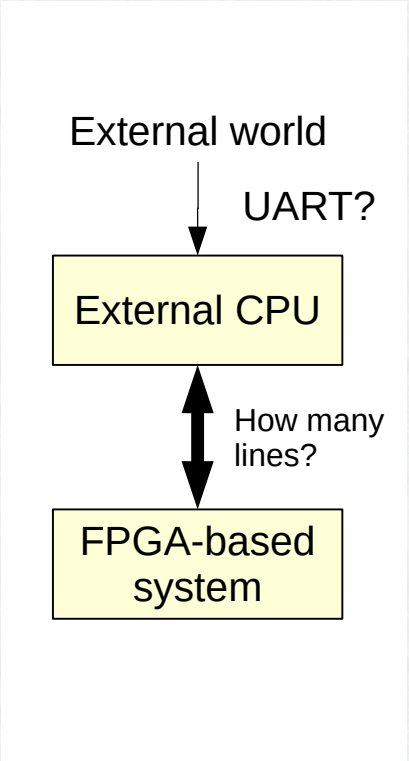

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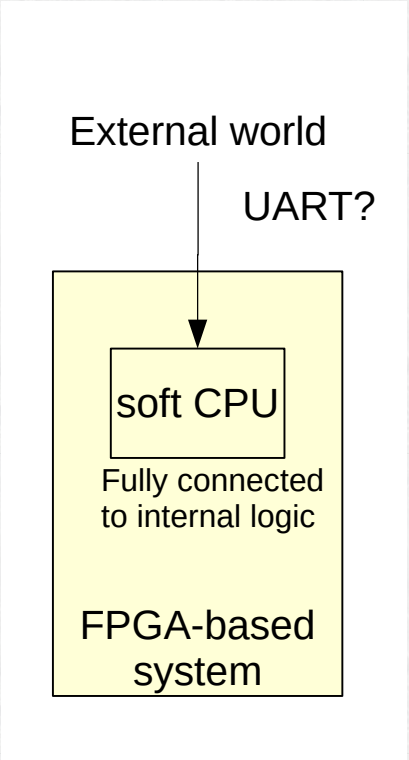

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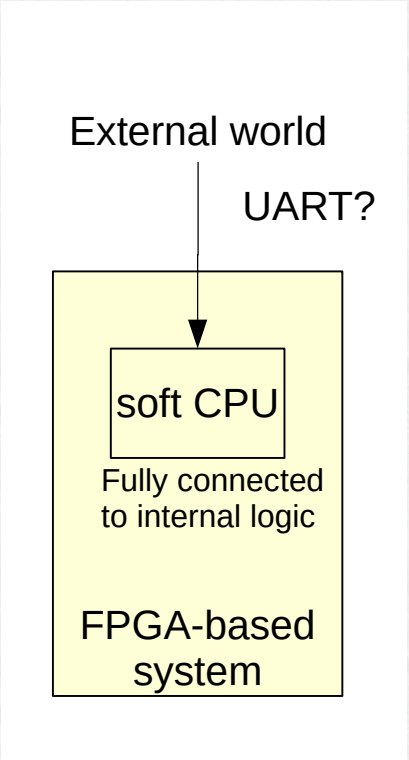

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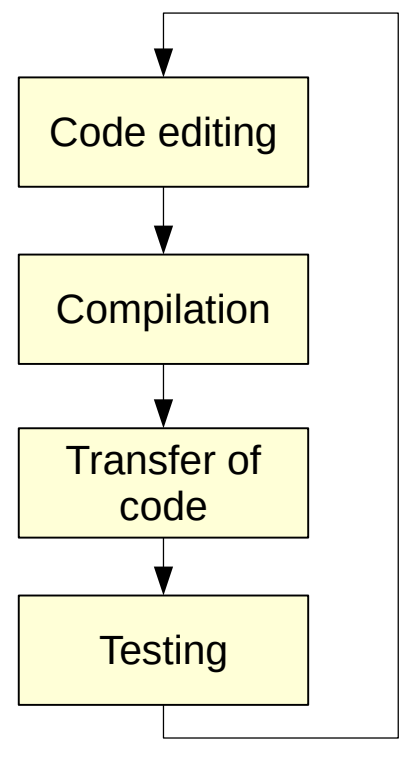

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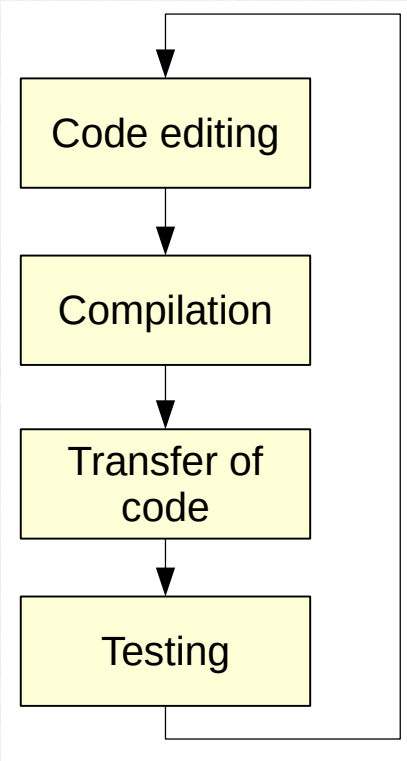
- Another possibility is to use Forth-capable CPU



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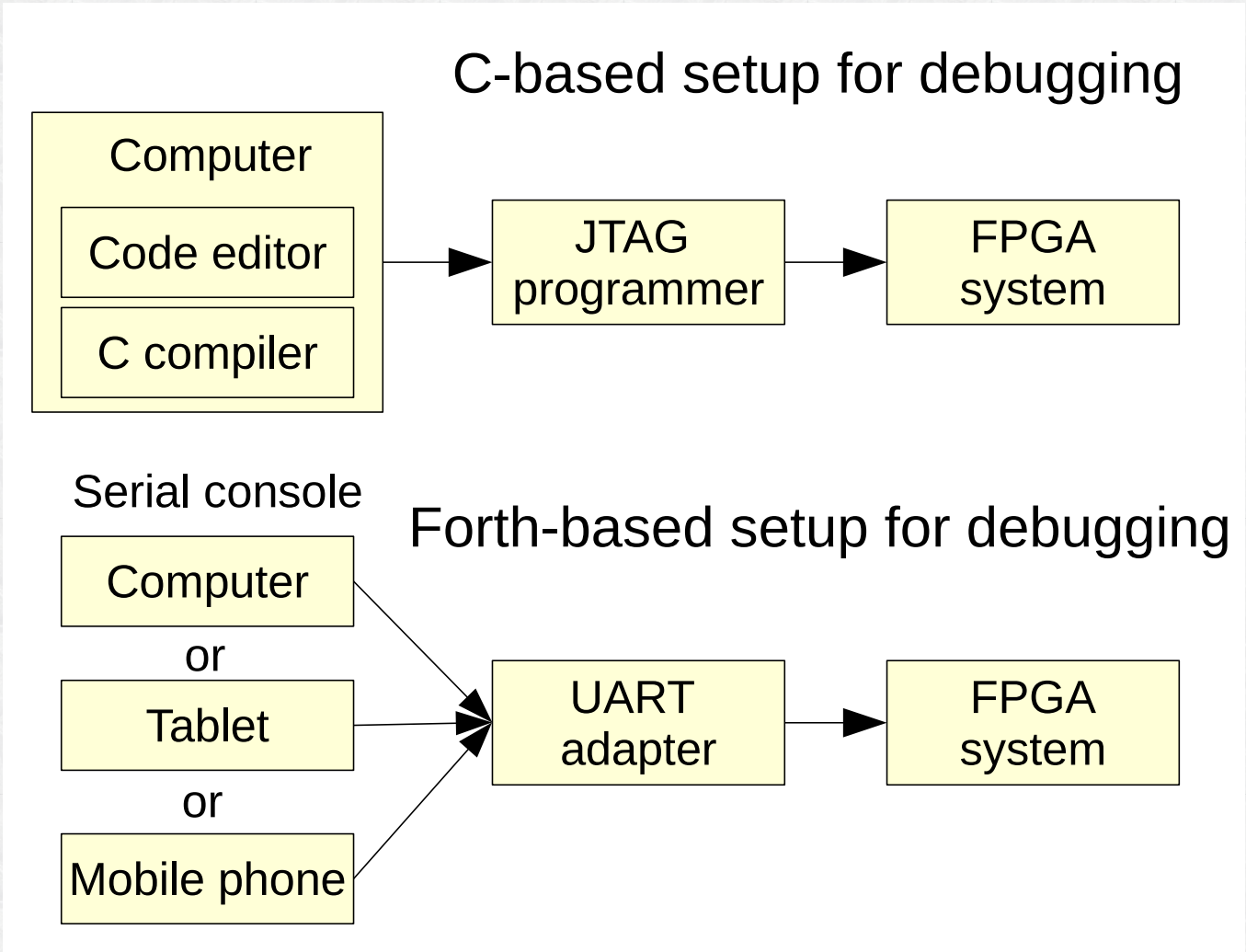
- Forth offers compact code with reasonable speed od execution
- It is possible to create complex, modular applications via incremental compilation
- The whole compiler and Forth CPU may be implemented in simple hardware, all what is needed for development is a serial console

# Comparison of required hardware



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```
>: fac ( n -- n! )
   1 swap 1+ 1
   ?do i *
   loop ;
   ok
>
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- How to avoid filling memory with incorrect definitions?
- It is possible to save the state of the system using the *marker* word, and restore it later

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- We can capture our commands in the terminal program.
- The captured definitions may be then moved to the source files.
- At the begining of the new session we may transfer those files to the Forth CPU

# Examples of Forth code


- Stack based language
- Reverse Polish notation used in calculations
- Limited support for local variables

```
\ i2c_wr1 writes a single byte
: i2c_wr1 ( dta addr -- )
    2* i2c_slv
    I2C_REGS 3 + io!
    64 16 or
    I2C_REGS 4 + io!
    begin
        I2C_REGS 4 + io@
        dup 2 and
    while
            drop
    repeat
  128 and if
      \ NACK in data
      134 err_halt
  then
;
```

# Forth for FPGA


- There are multiple implementations of Forth CPU in HDL (Verilog or VHDL)
  - http://www.forth.org/cores.html
  - http://www.ultratechnology.com/chips.htm
- We have tried to implement our own “tethered” version [2].
- The most successful implementation seems to be the J1 CPU designed by James Bowman [3].
- The original version is implemented in Verilog in 117 lines [4].

# J1B based Forth


- The Forth CPU is only one component of the successful Forth system
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  - saving the commands to the history file
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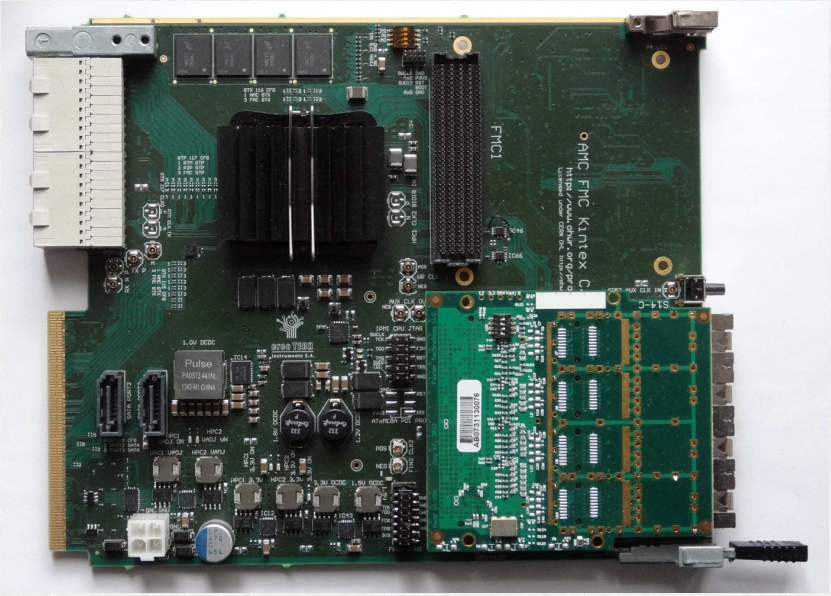
  - saving the commands to the history file
  - dumping the memory contents to the file
  - loading source files to the Forth CPU
- The "cold" word, if defined, is executed after the powerup or reset

# AFCK board controller

- Project developed for AFCK boards used as DPB prototype in CBM experiment
- Forth CPU uses I2C interface
  - to read the MAC address
  - to configure the Silabs Si57x clock generator
  - to configure clock switch matrix
- Support for Si57x required implementation of multiple precision arithmetics library
- The status of the initialization routine may be stored in register available for the firmware

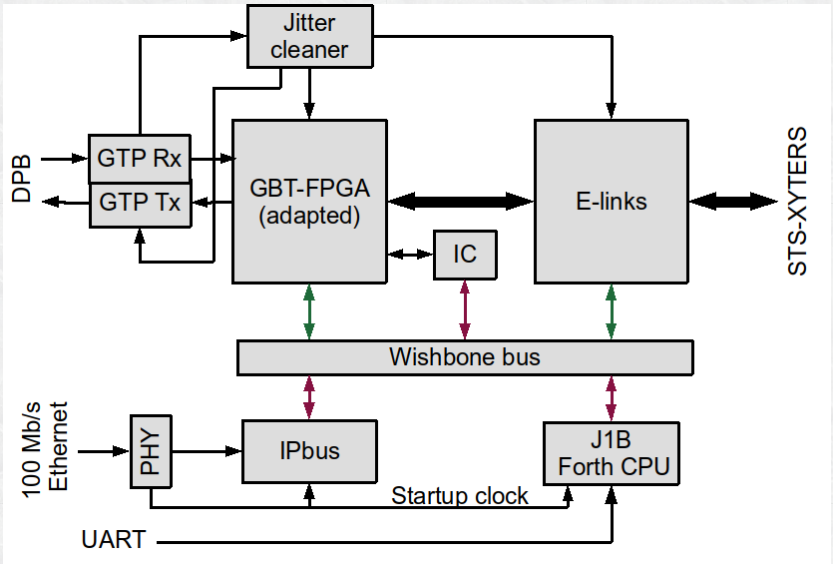


# Example word from arithmetics library


```
\ Definition of the unsigned double compare
: ud< ( a0 a1 b0 b1 -- flag )
    \ If MSW are equal, check the LSW
   rot ( a0 b0 b1 a1 )
   over over = if ( a0 b0 b1 a1 )
       \ MSWs are equal, so compare LSWs
      drop drop ( a0 b0 )
      u<
   else ( a0 b0 b1 a1 )
       \ MSWs are not equal, so their comparison produces the
      u> >r ( a0 b0 )
      drop drop r>
   then
;
```

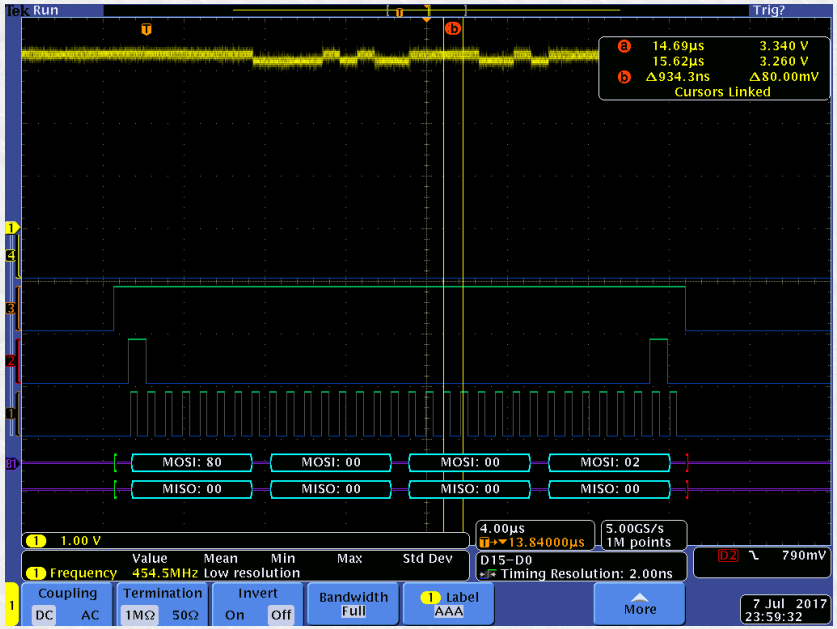
# GBTxEMU System controller

- Forth CPU is one of three masters of the internal Wishbone bus
- Its task is to initialize the system at powerup so that it can be further controlled via optical link
- Later on it can be used for interactive debugging and testing
- Access to internal registers is supported by address tables generated by the addr_gen_wb framework.



# Sayma board controller

- Library developed for Sinara project
- Implements support for many SPI connected peripherals



# How to start with Forth


- Experimenting with Forth does not require FPGA board
- J1B provides also the emulated environment based on Verilator
- Gforth is available for PC
- There are many implementations for microcontrollers. Just a few examples:
  - Mecrisp for ARMs
  - FlashForth for AVR and PIC microcontrollers
  - Amforth for AVR and RISC-V
  - Punyforth for ESP8266

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- Words created in interactive session may be used to create complex applications, e.g. used for initialization of the hardware.
- The ready application may be automatically started after power-up
- Forth may be a good solution for interactive in-field debugging or testing also of MCU-based systems

# Bibliography


[1] Leo Brodie.
Thinking Forth.
http://thinking-forth.sourceforge.net/ .

[2] Paweł Goździkowski and Wojciech M. Zabołotny.
Tethered Forth system for FPGA applications.
*Proc. SPIE*, 8903:89031M, October 2013.

[3] James Bowman.
The J1 forth CPU, 2010.
https://www.excamera.com/sphinx/fpga-j1.html .

[4] James Bowman.
The J1B source code, 2010.
https://github.com/jamesbowman/swapforth/blob/master/j1b/verilog/j1.v .