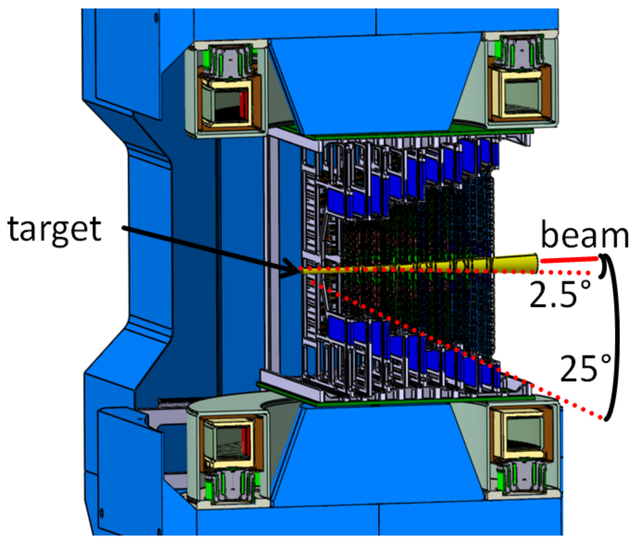
The Silicon Tracking System of CBM
getting ready for experiment

Adrian Rodríguez Rodríguez[1,2] for the CBM Collaboration

STS for the CBM experiment

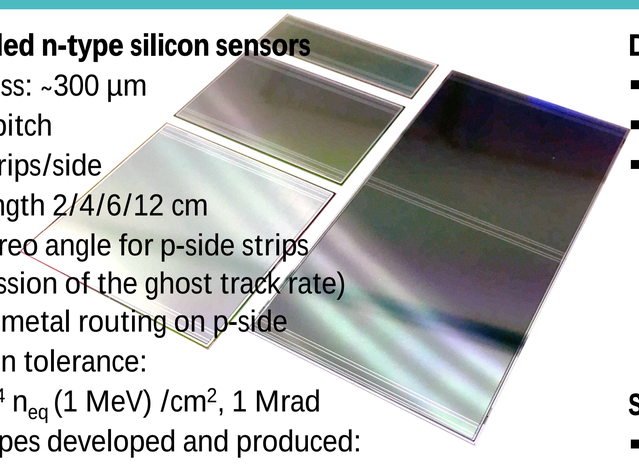


- track point measurement in high-rate collision environment: $10^5 – 10^7$/s (A+A), up to 10^9/s (p+A)
- physics aperture : $2.5° \leq \Theta \leq 25°$
- 8 tracking stations built with double-sided silicon microstrip sensors
- self-triggering front-end electronics
- material : ≈ 0.4% – 1.4% X_0 per station
- hit spatial resolution ≈ 25 µm
- Δp/p ≈ 1.8% (p > 1 GeV/c, 1 Tm field)
- track (> 1 GeV/c) and single hit reconstruction efficiency 96% and 98%

Silicon sensors and detector module

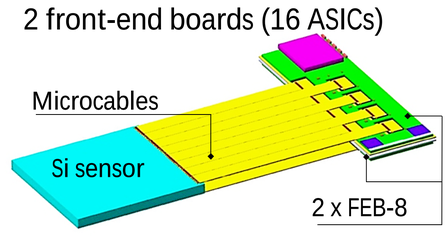
Double-sided n-type silicon sensors

- Thickness: ~300 µm
- 58 µm pitch
- 1024 strips/side
- strip length 2/4/6/12 cm
- 7.5° stereo angle for p-side strips (suppression of the ghost track rate)
- double-metal routing on p-side
- radiation tolerance: 1×10^{14} n_{eq} (1 MeV) /cm², 1 Mrad
- prototypes developed and produced: CiS/Germany and Hamamatsu/Japan



Detector module as functional unit:

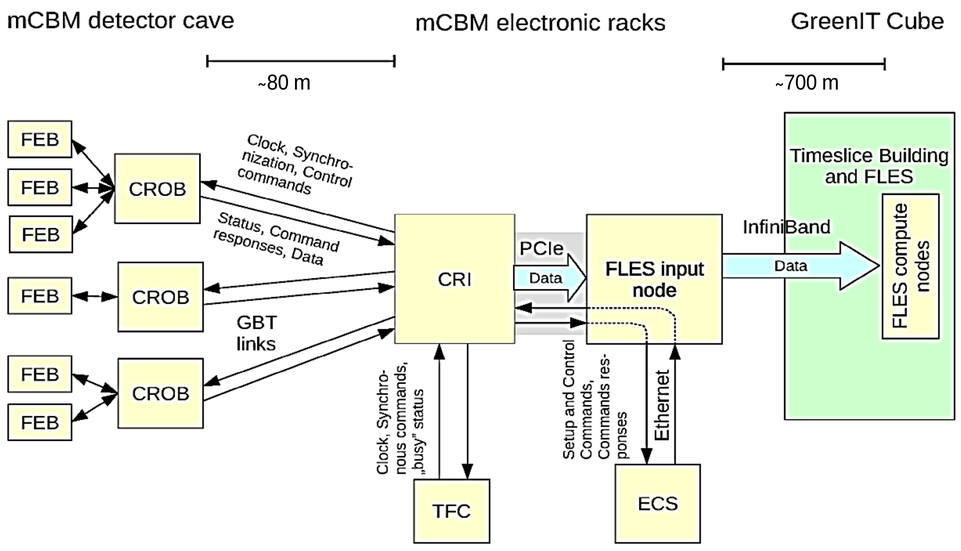
- silicon sensor
- stack of polyamide readout cables
- 2 front-end boards (16 ASICs)



STS detector in numbers:

- 896 detector modules
- 106 ladders
- 1.6 million channels

Readout chain



Block diagram of the STS readout chain

High performance, free-streaming readout chain

Main components:

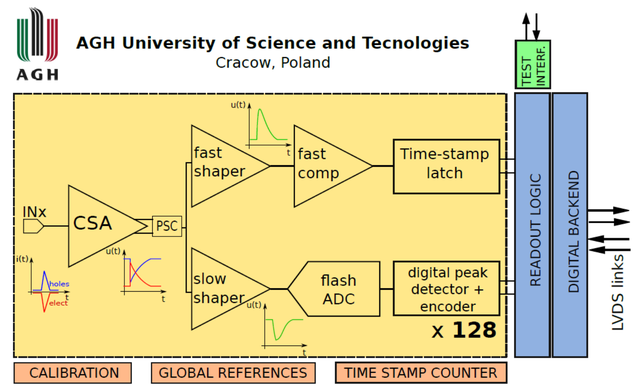
FEB: Front-end boards
ROB: Readout board
CRI: Common readout interface
TFC: Timing and fast control
ECS: Experiment control system
FLES: First level event selector

Front-end electronics

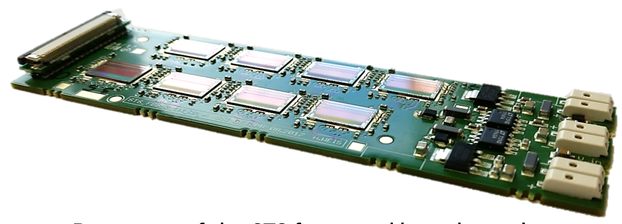
STS-XYTER ASIC

STS + **X**, **Y** coordinates + **T**ime and **E**nergy **R**esolution

- 128 readout channels + 2 test channels
- expected total capacitance: Up to 40 pF
- both signals polarity
- time resolution < 5 ns
- 5 bit flash ADC/channel (15 fC dynamic range)
- hit rate/channel: >250 kHz
- radiation hard layout
- digital backend compatible with the CERN-GBTx data concentrator



Block diagram of the STS-XYTER ASIC

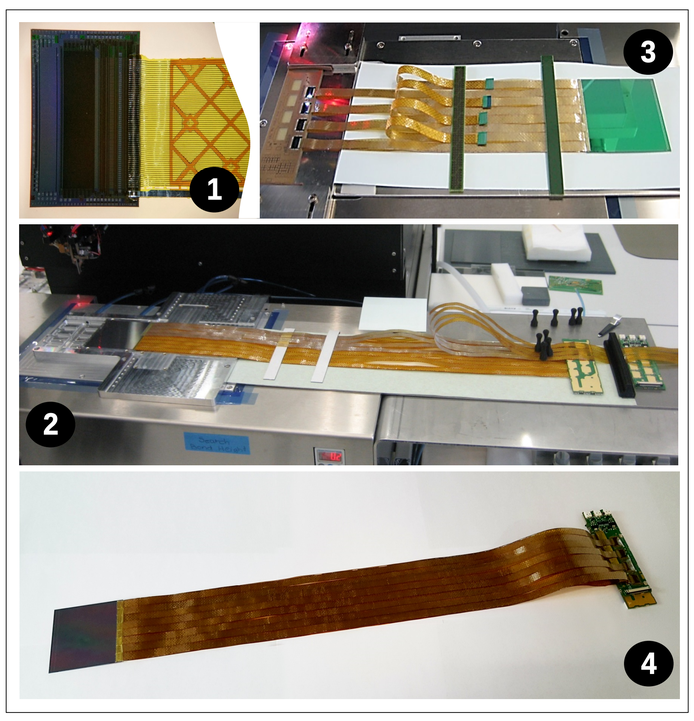


Prototype of the STS front-end board carrying 8 STS-XYTER ASICs

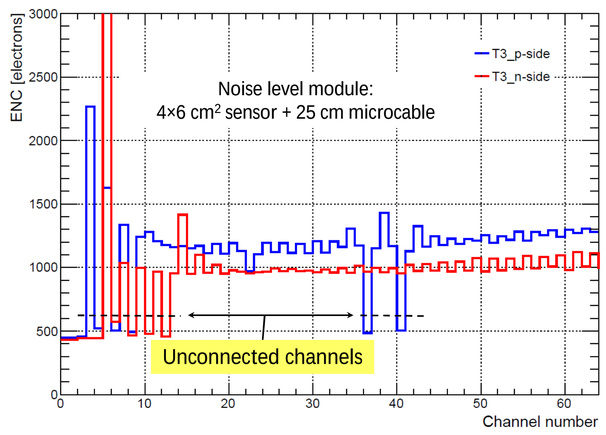
Front-end Board

- part of a functional module
- high-level integration board with 8 STS-XYTER ASICs and up to 5 data links per ASIC
- connected via microcables to the Si sensors

Module assembly

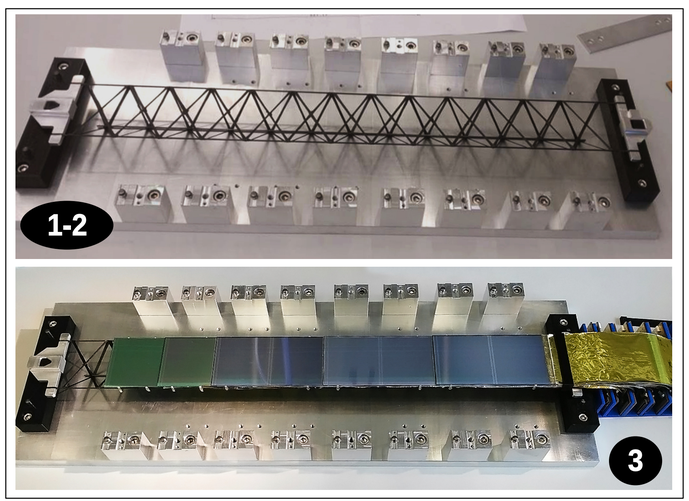


STEP_1: tab-bonding microcables to ASICs
STEP_2: tab-bonding microcables to Si-sensor
STEP_3: die and wirebonding ASICs to the FEB-8
STEP_4: glueing of shielding layers and spacers



Electrical connectivity tests

Ladder assembly



STEP_1: glueing support structures for sensor holding
STEP_2: mounting modules onto low-mass carbon-fiber support
STEP_3: semi-automated optical survey for monitoring sensor position (10 µm precision)
STEP_4: ladder transfer to mounting frame (See mSTS fig.)

mCBM at SIS18

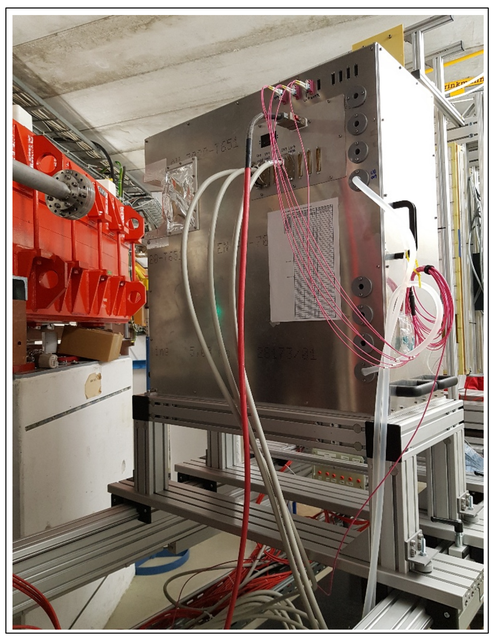
CBM full test setup for high rate, nucleus-nucleus collisions at GSI/FAIR SIS18

GOALS:

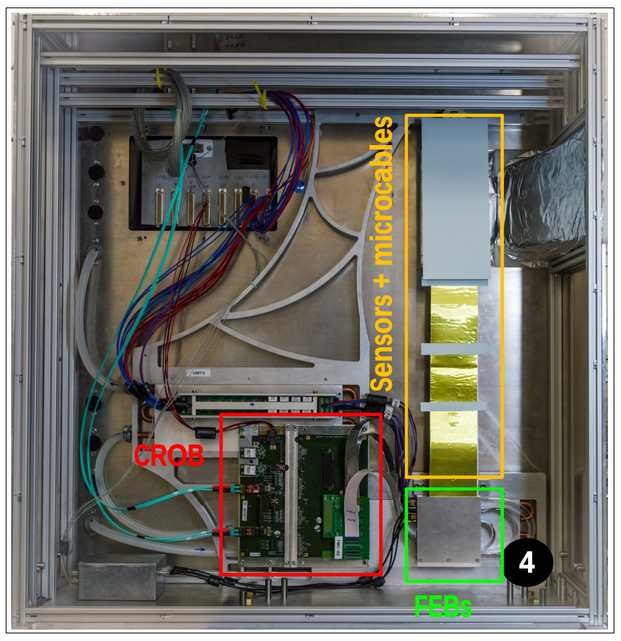
- demonstrator for full CBM data taking and analysis
- integrating prototype detector's modules into a common, free-streaming DAQ
- reconstructing physics observable (Λ reconstruction using Ni-Ni at 1.93 AGeV and Au+Au at 1.54 AGeV)

STS getting ready (mSTS)

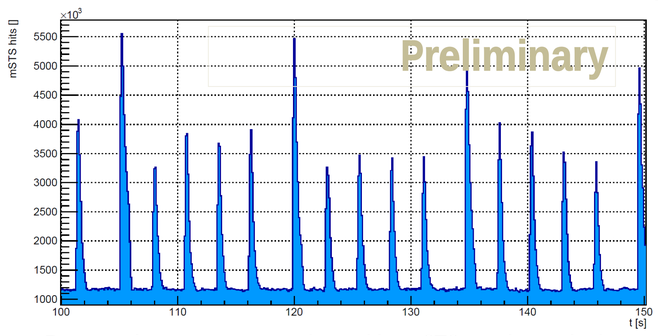
- operation of full STS modules in real data taking scenario
- 13 STS sensor modules grouped in 2 tracking stations (5 ladders)
- 208 STS-XYTER ASICs (~26600 readout channels)
- December 2018: first detector ladder with 2 modules installed



Installation of mSTS in the beam line at SIS18



Service box of mSTS containing ½ station built with 2 modules



Beam spill structure monitored in mSTS modules during commissioning runs

STS project:

Key participant institutes:
GSI (*Darmstadt, Germany*), JINR (*Dubna, Russia*), Univ. Tübingen (*Germany*), KIT (*Karlsruhe*, *Germany*), AGH (*Krakow*, *Poland*), JU (*Krakow*, *Poland*), WUT (*Warsaw*, *Poland*)

Timeline:

- Production Readiness: Jun. 2019
- Detector construction: 2019 – 2024

Assembly Centers: GSI-FAIR, JINR-VBLHEP

1. Goethe Universität Frankfurt am Main
2. GSI Helmholtzzentrum für Schwerionenforschung
a.rodriguezrodriguez@gsi.de

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