Pixel detector

Sezione di Torino

Status report on
the PANDA pixel detector readout

Module concept

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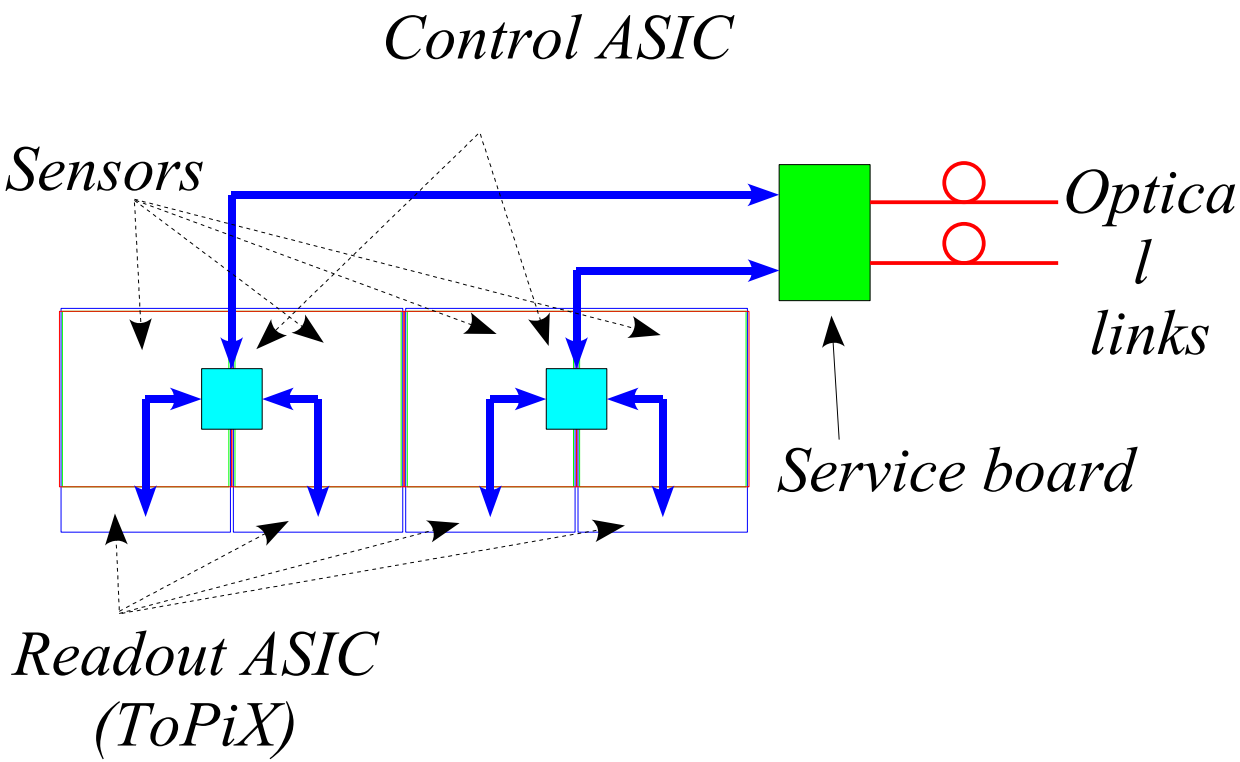

- Modules of 2,3,5 or 6 chips
- TPXctrl acts as a data concentrator. Chips can be chained
- Service board provides voltage regulation and electrical/optical transmission

Data transmission

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- All components have to be radiation hard.
- ToPiX → TPXctrl
  - 320 Mb/s electrical link (e-link)
- TPXctrl → Service board
  - 320 Mb/s (e-link)
  - 1 Gb/s (joint development with NA62 GTK)
- Service board → Counting room
  - GBT

Barrels

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Layer #	# of staves	# of ToPiX	# of TPXctrl
1	14	52	22
2	28	300	100
		352	122

Disks

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Disk #	# of ToPiX	# of TPXctrl
1	20	10
2	20	10
3	108	44
4	108	44
5	108	44
6	108	44
Total	472	196

Specifications

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- Pixel size : 100 μm × 100 μm
- Chip active area : 11.4 mm × 11.6 mm (116 rows, 110 cols)
- dE/dx : Time over Threshold, up to 100 fC
- Analog noise floor : < 32 aC (200 e^-)
- System clock frequency : 155.25 MHz
- Max event and data rates *(est.)* : $21 \cdot 10^6$ hits/s/chip - 1.4 Gb/s/chip
- Power consumption : < 500 mW/cm^2
- Total Ionizing Dose : < 100 kGy
- Equivalent neutron fluence : < $5 \cdot 10^{14}$ 1MeV n_{EQ}/cm^2

ToPiX v2

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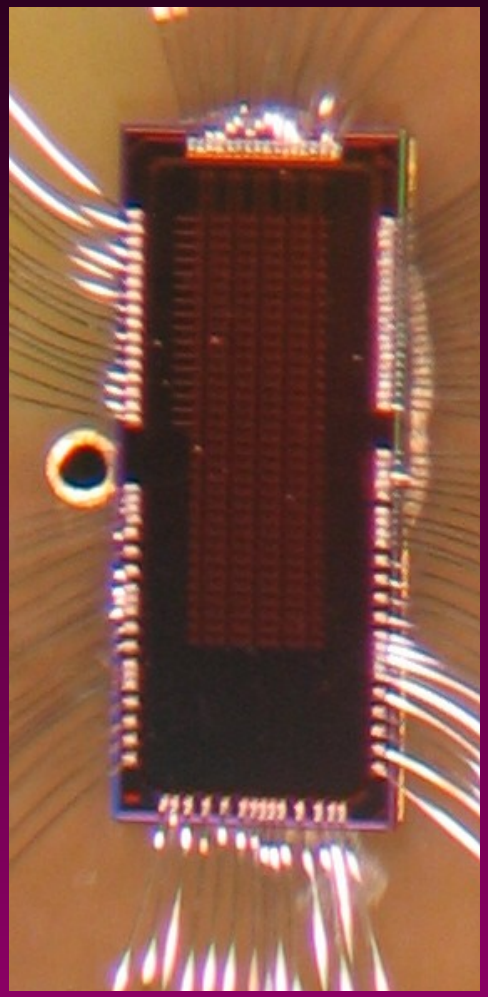

- Full pixel cell (analogue + digital)
- Two folded columns with 128 cells
- Two columns with 32 cells
- 5x2 mm^2 die area
- CMOS 0.13 μm LM technology
- Dice-based SEU resistant FFs
- Tests :
  - → test bench
  - → with a sensor and a radiation source
  - → TID and SEU

ToPiX v3

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- Under design
- 5x4 mm^2 die area
- CMOS 0.13 μm DM technology
- Triple redundancy-based SEU protection
- End of column logic
- 320 Mb/s serial output
- Pads for bump bonding

Triple redundancy

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Cell type	Cell size	Comments
Dice	$6\times7\ \mu m^2$	ToPiX v2
Triple redundancy	$7\times9.6\ \mu m^2$	ToPiX v3 data register
Triple redundancy with self correction	$9\times14.4\ \mu m^2$	ToPiX v3 control register

Pixel cell

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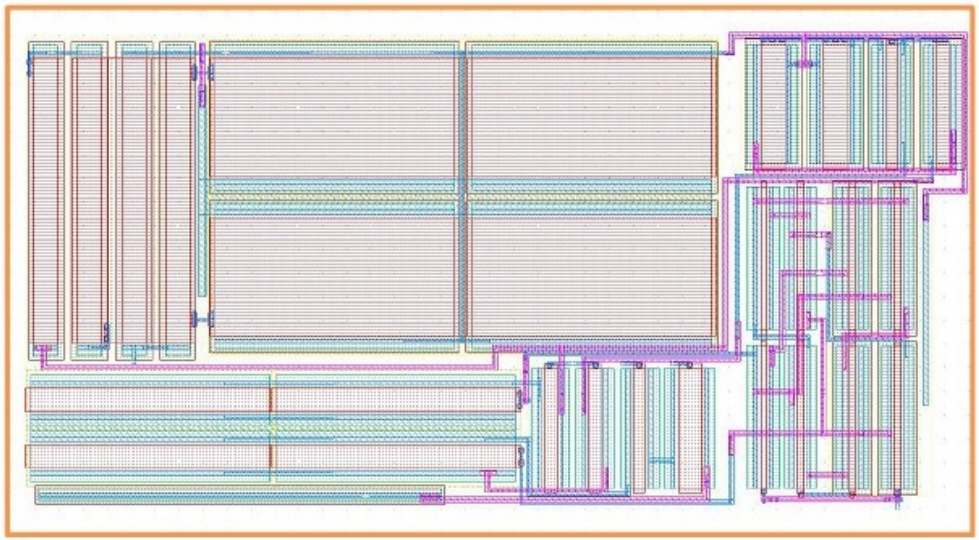
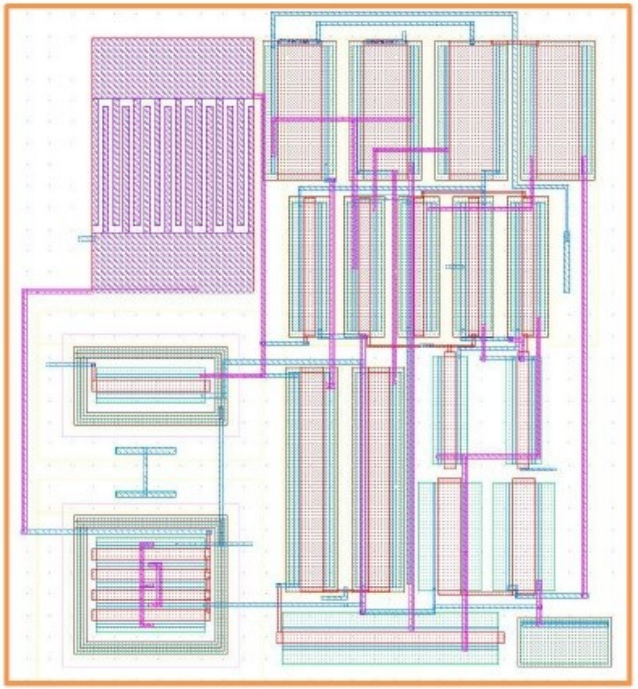
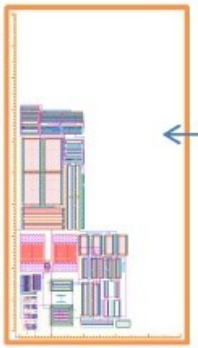
Filter stage: 40µm x 20µm (50% of area of the previous)



Preamplifier 35µm x 30µm



Analog Cell 100µm x 50µm



← To be designed

T. Kugathasan

Digital readout

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- Common buses for two pixel columns
- Time stamp distribution @ 155 MHz
- Pixel readout @ $f_{CK}/4$
- Circuitry already designed for the NA62 GTK prototype, currently under test
- End of column control logic design started (*L.Toscano*)

PANDA-GBT meeting

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- PANDA GBT-meeting on March 3rd 2010
- People : J. Christiansen, I. Konorov, G. Mazza, P. Moreira
- No showstoppers for the use of GBT for PANDA (neither technical nor political)
- GBT chip available in 2 years (~final version)
- Building block also available for customization
- FPGA code already available

GBT project

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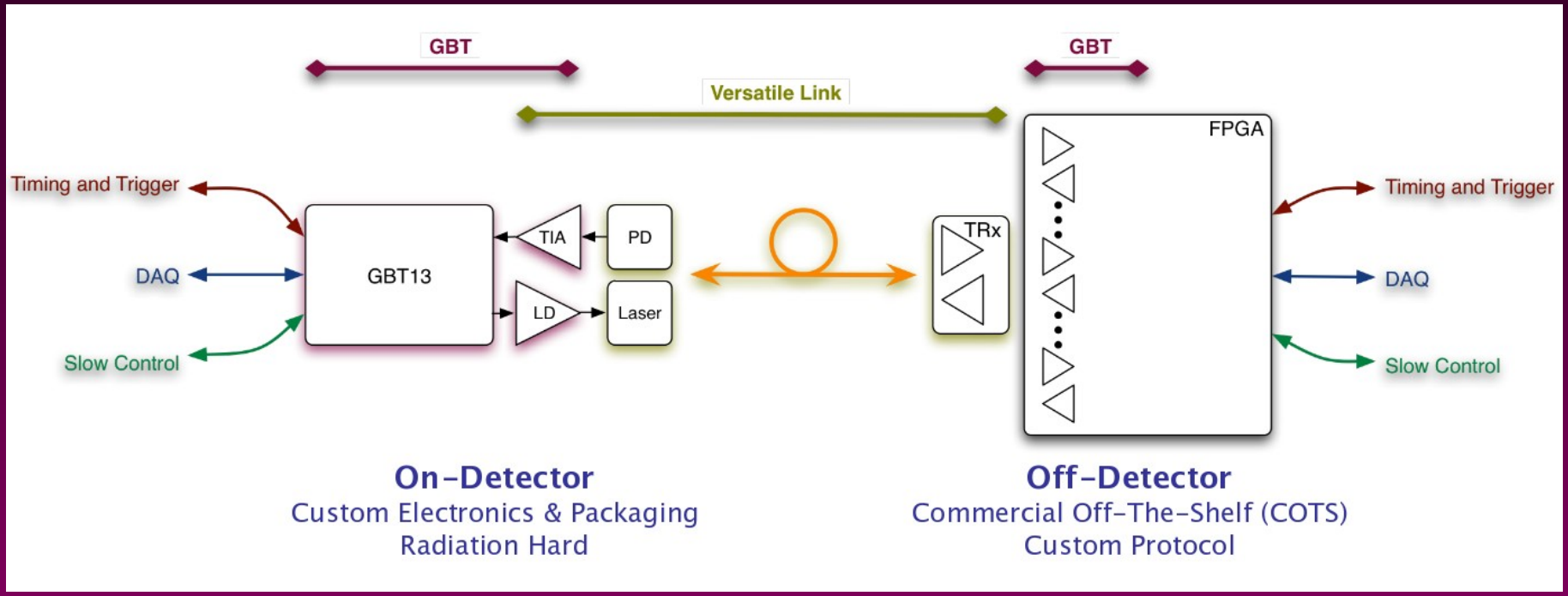

Conclusions

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- ToPiX v3 design is ongoing :
  - Analog cell design well advanced
  - Digital cell and end of column design started
  - Possible submission dates : May or November 2010
- Readout architecture design :
  - Cable testing → PdR presentation
  - First contacts with CERN for the GBT
  - Data rates still an open issue