Development of 10 bit pipeline ADC and triggerless data processing readout

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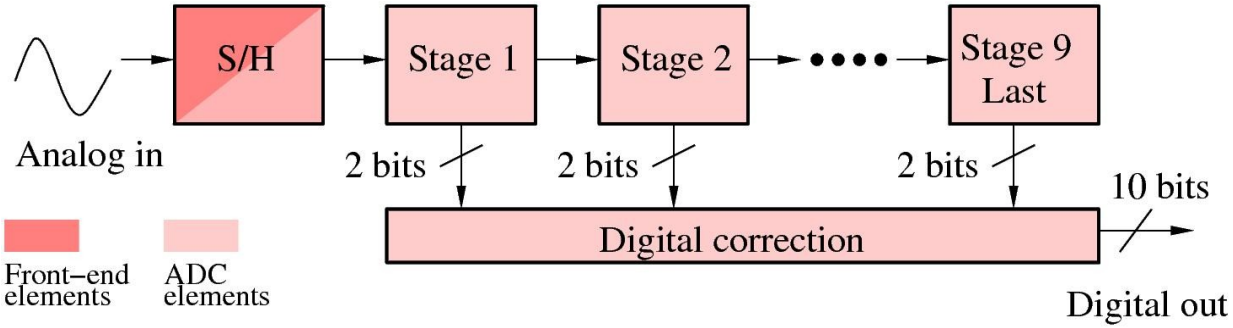
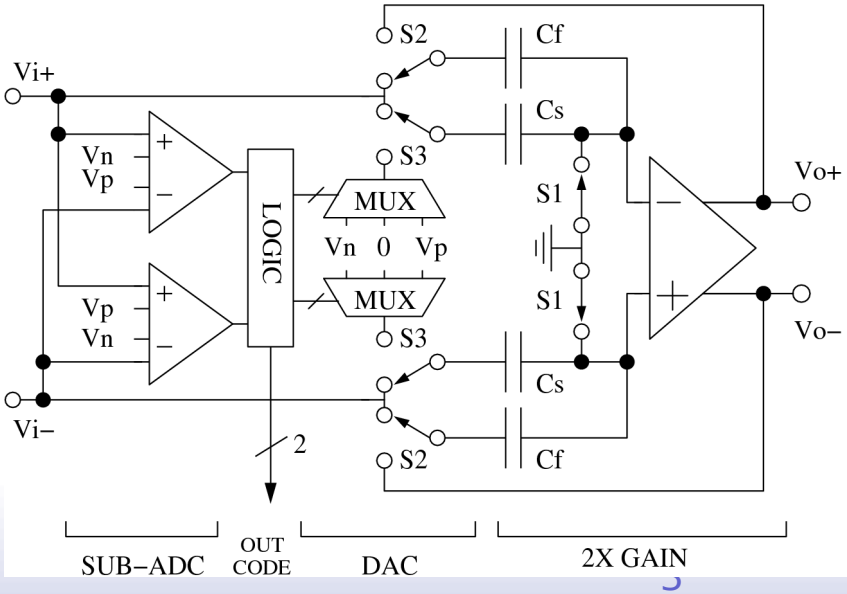
Outline

- Design and measurements of 10 bit pipeline ADC
- Triggerless readout with amplitude and time measurement
  - Simulations
  - Test setup
  - Measurements results

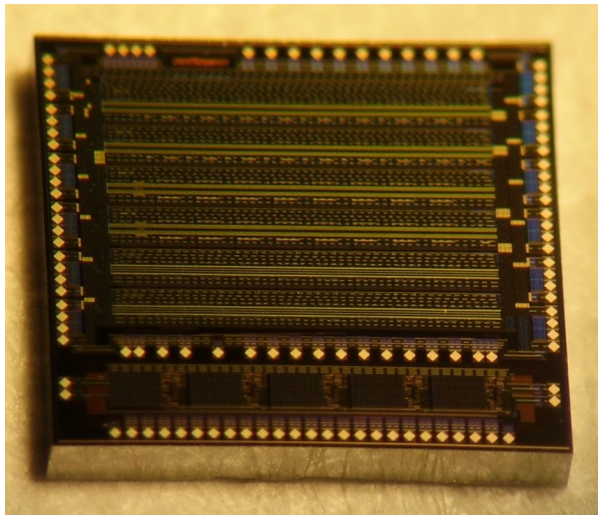
Design of 10 bit pipeline ADC

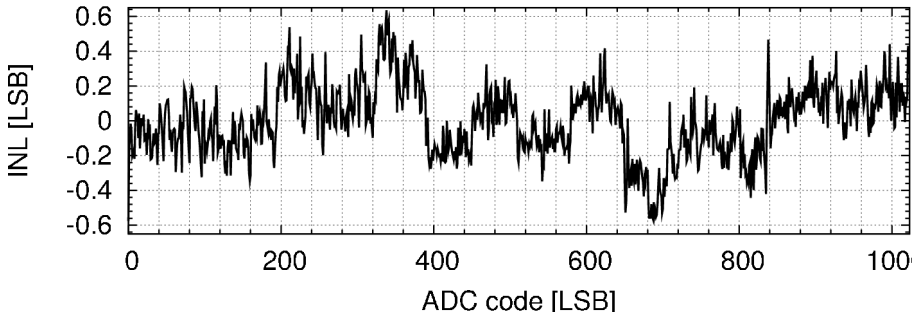


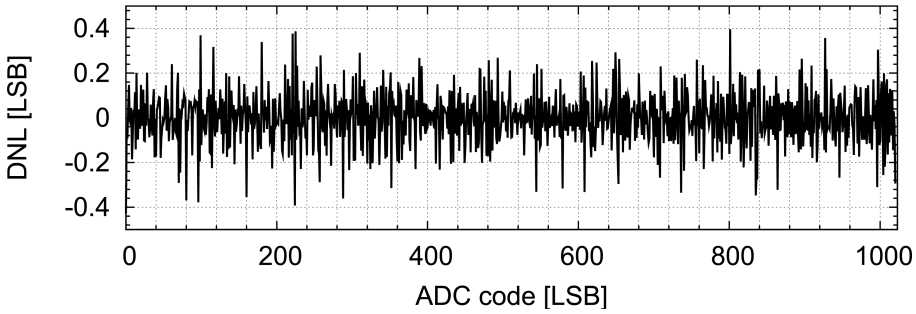
- 10 bit pipeline ADC 1.5 bit/stage
- Variable sampling frequency up to ~25 Ms/s
- Scalable power consumption
- Fully differential
- Power switching OFF/ON (ILC, CLIC beam timing)
- Present version in 0.35 μm AMS, smaller size technology soon...

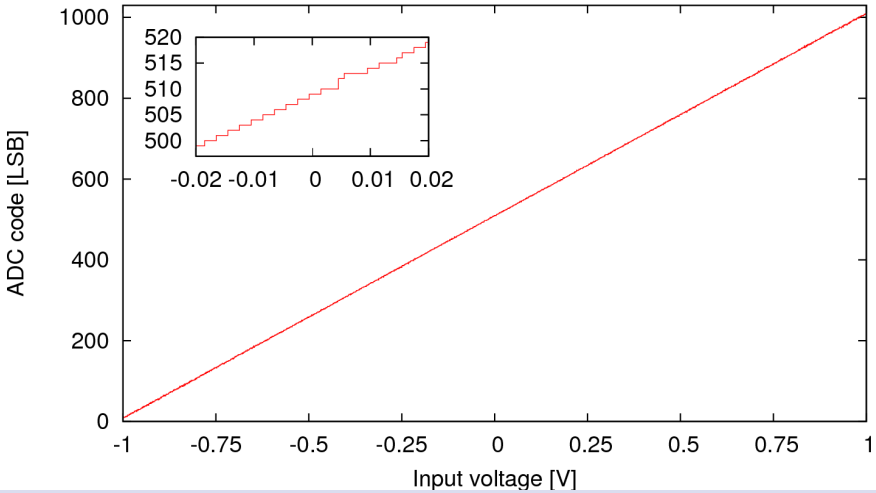


ADC static measurements





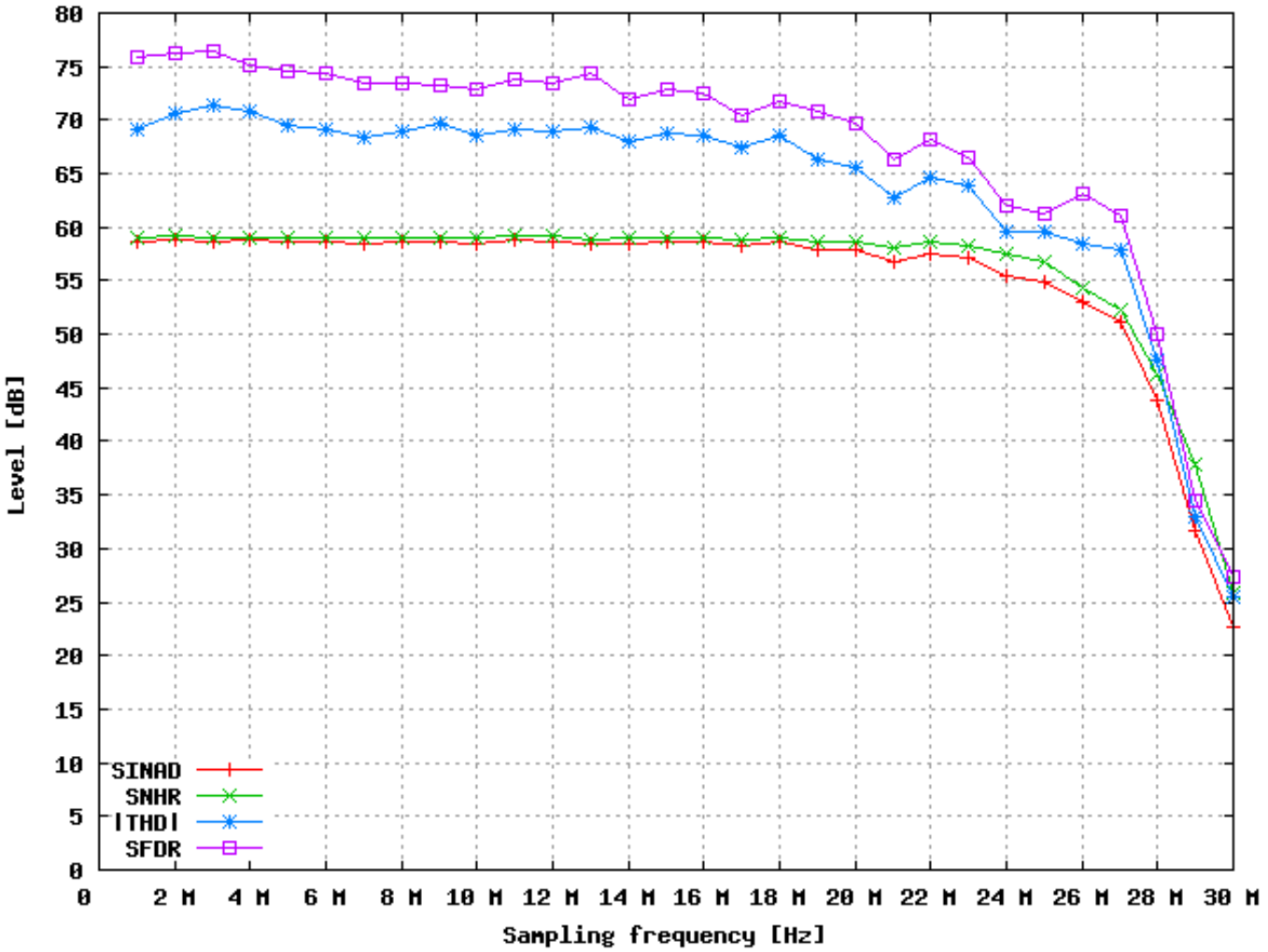




Very good linearity

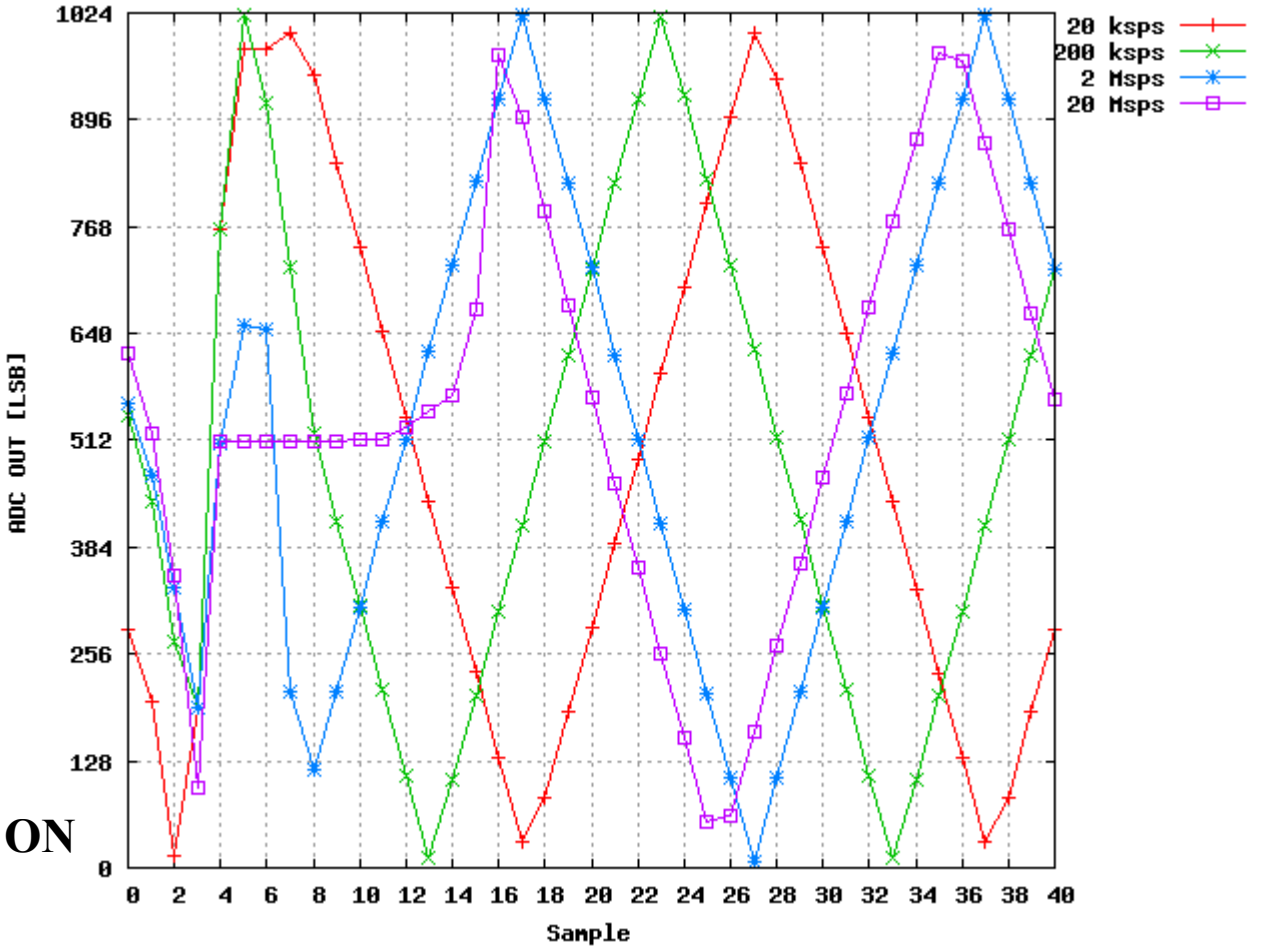
INL < 1LSB, DNL < 0.5 LSB

ADC dynamic measurements



Good dynamic performance ENOB ~ 9.5 bit

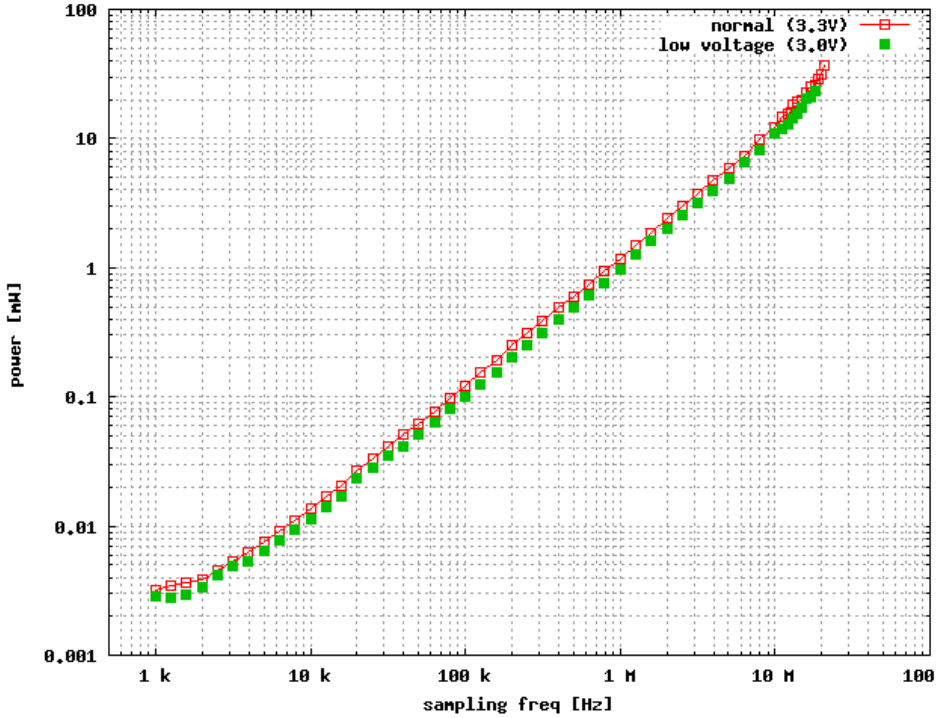
ADC – power OFF/ON

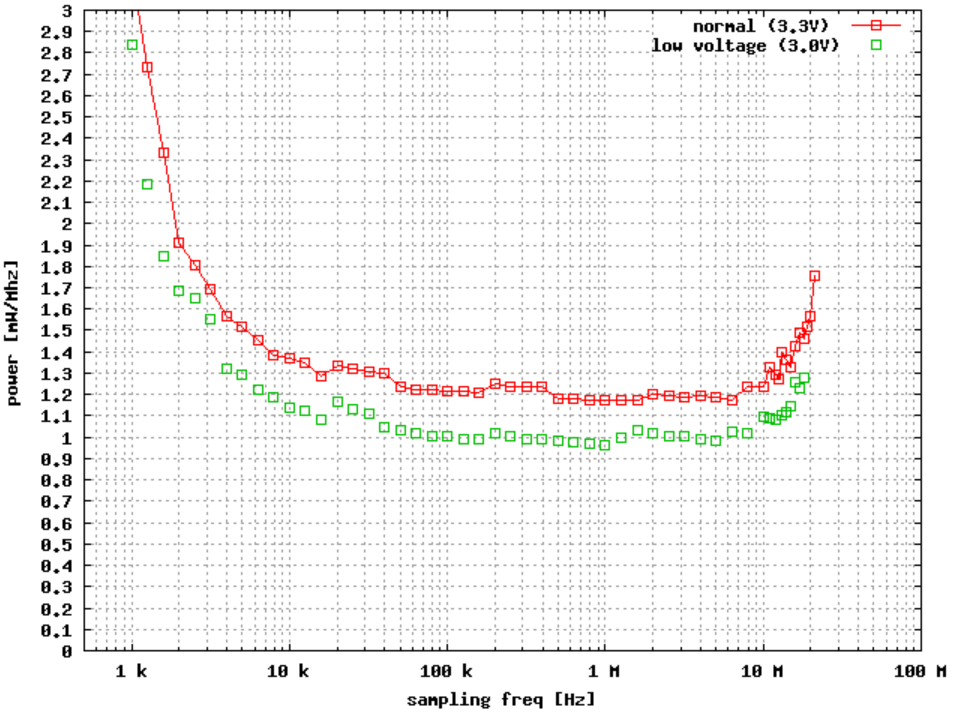


Power ON at t=0

Depending on sampling frequency 8-16 clocks needed for switching ON

ADC power consumption

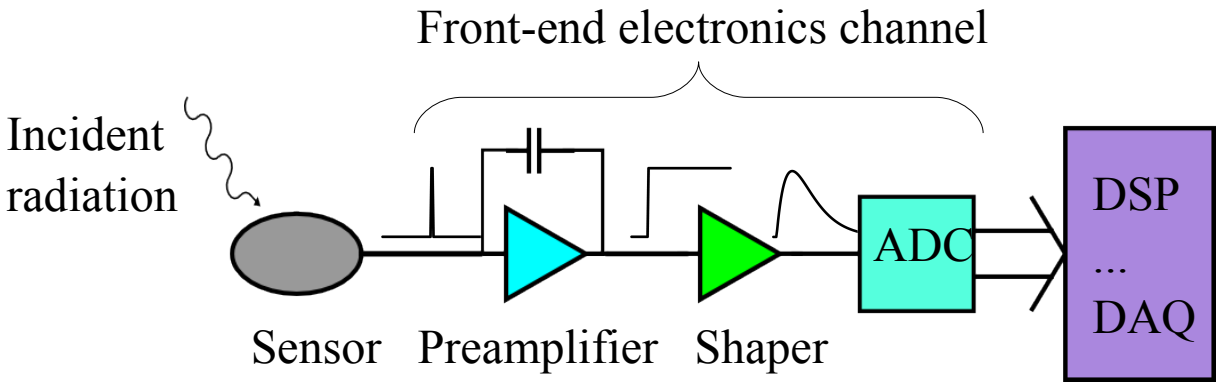




Presently power consumption about 1-1.5 mW/MHz at worst case (Nyquist input frequency, output buffers)

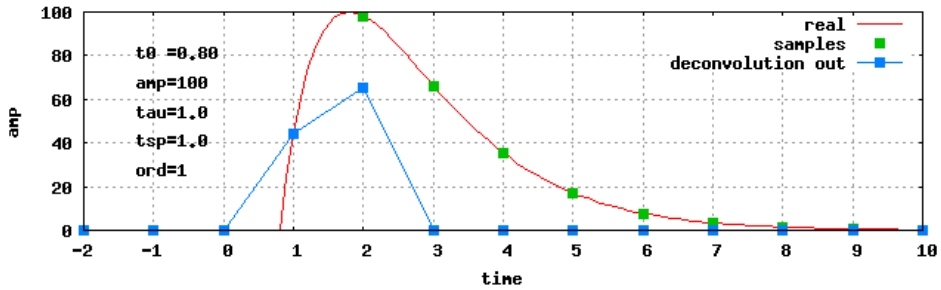
We have just submitted 8 channels ADC version layout with a pitch 200 µm per channel

Deconvolution - idea



- No trigger – ADC continuously running
- Fixed pulse shape at ADC input!!!
- Very good candidate is a semi-gausian 1st order CR-RC, only 3 samples are needed
- Timing and amplitude information are obtained manipulating deconvoluted samples
- For CR-RC shaping - 100% pileup free if $\Delta T_{pulse} > 3T_{samp}$, e.g. $T_{peak}=100ns$, $T_{samp}=100ns \rightarrow$ no pileup if $\Delta T_{pulse} > 300ns$

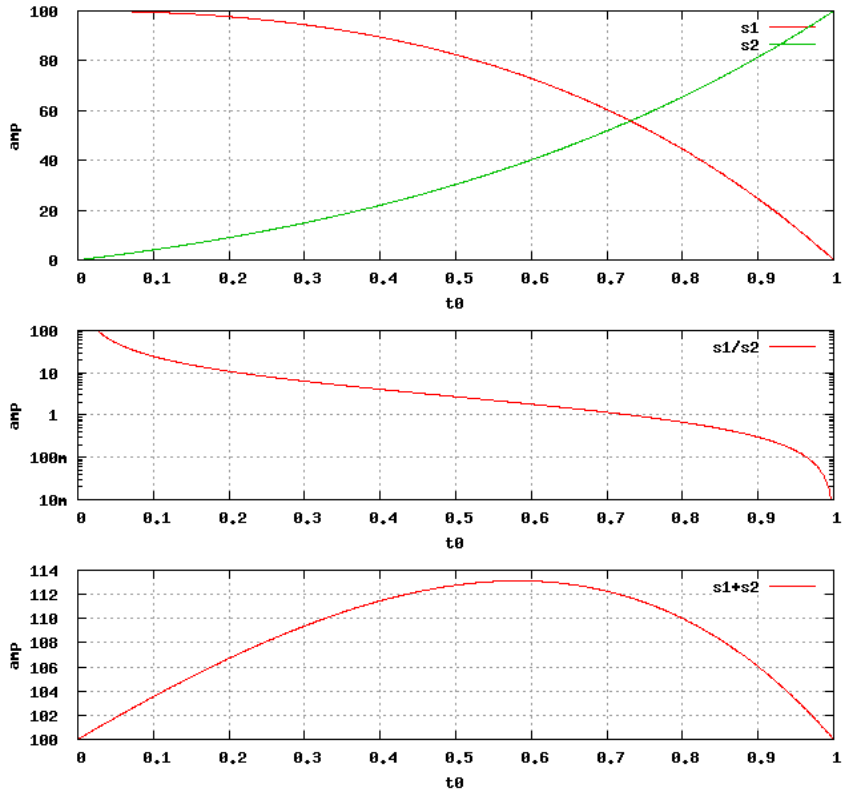
Simulated example of deconvolution for CR-RC shaping and $T_{peak}=T_{samp}$



Amplitude info is obtained from the sum of blue samples and timing info from their ratio (for both lookup tables needed)

Deconvolution after CR-RC

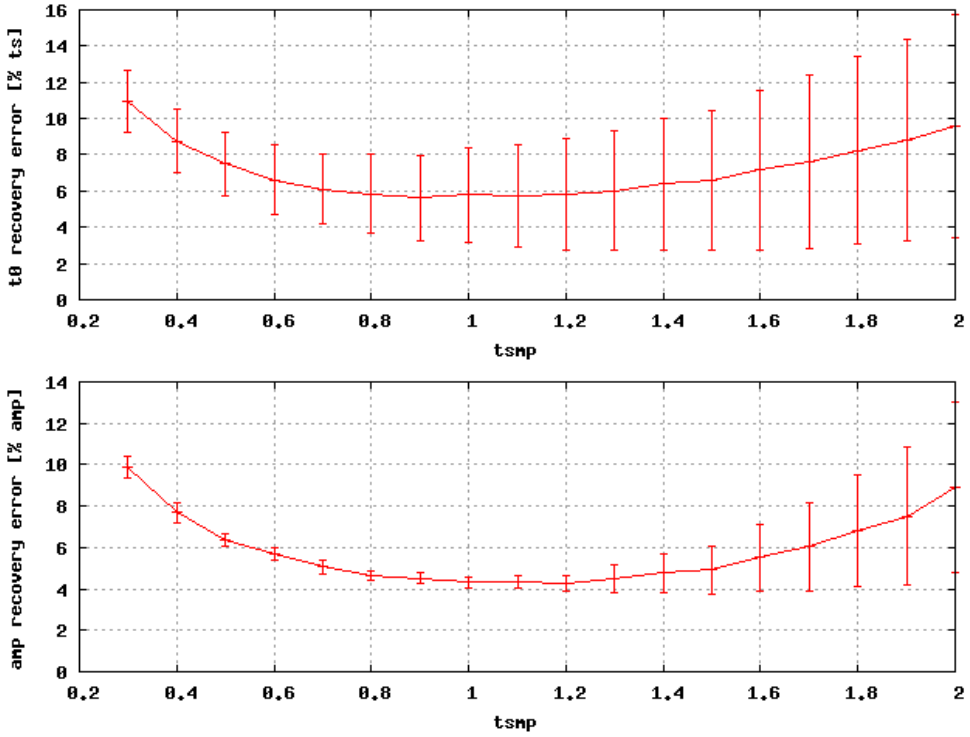
Deconvoluted samples, their ratio and sum



Simulated

Timing and Amplitude error vs Sampling time

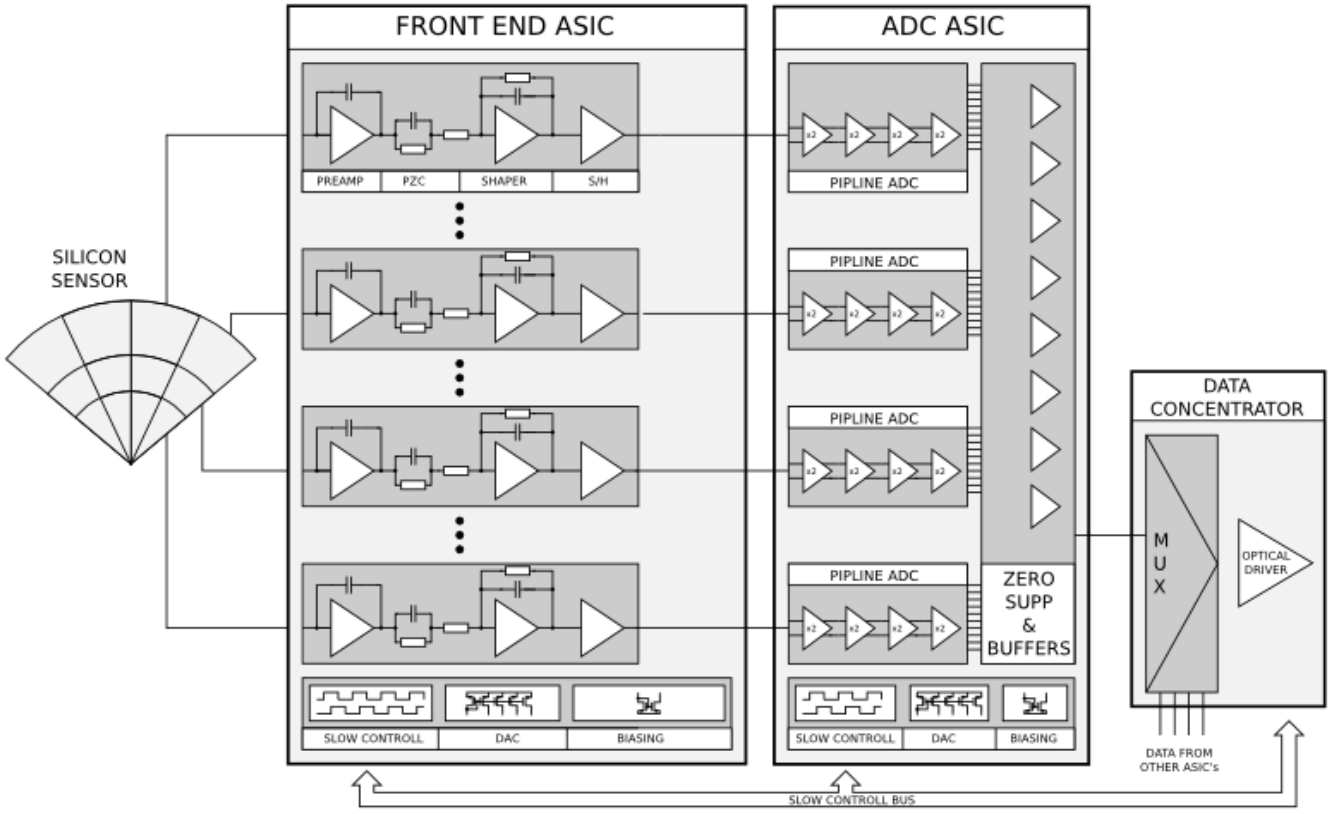
S/N =25 was used for this MC



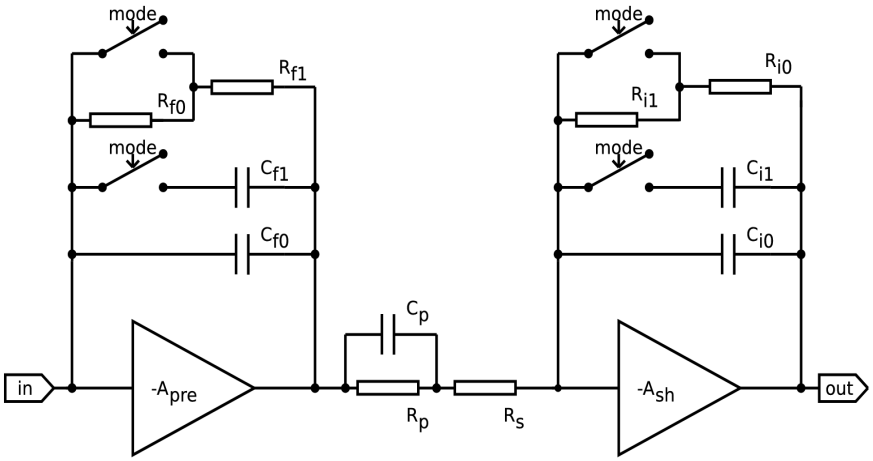
Other than CR-RC shapers are also considered but not shown here since no measurements are available

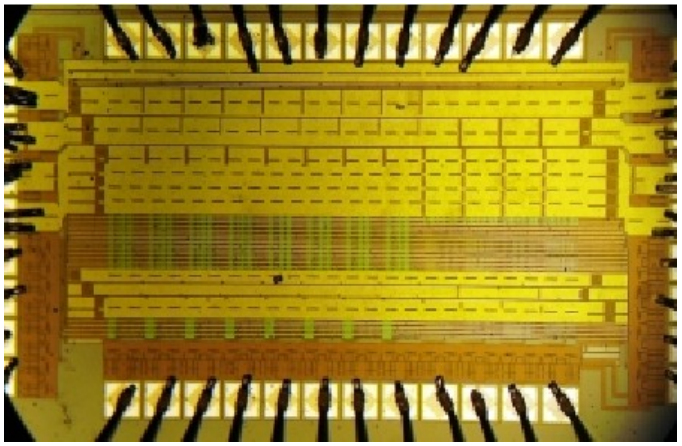
Readout architecture for luminosity detector at ILC/CLIC

- Prototypes in AMS 0.35 µm
  - 8 channels front-end
  - 1 channel ADC (no zero suppression)

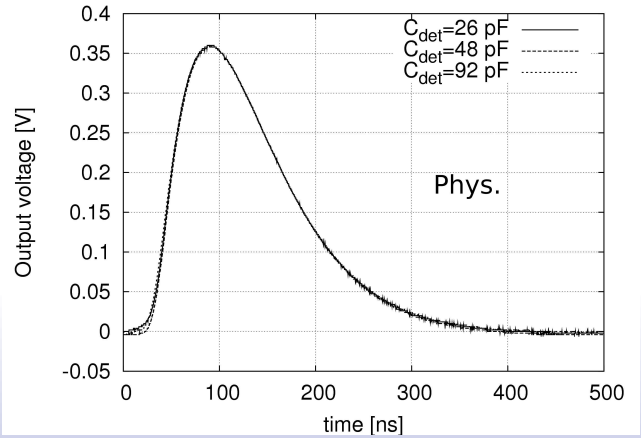


Preamplifier&PZC&Shaper



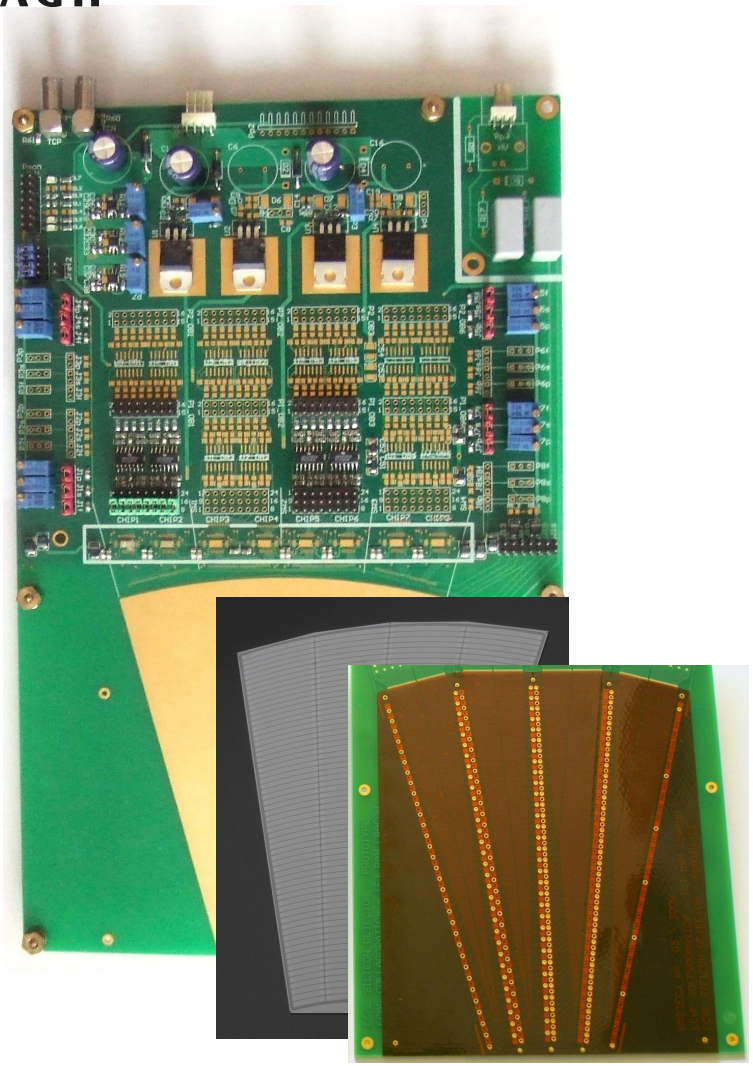


$$\frac{U_{out}(s)}{I_{in}(s)} = \frac{1}{C_f C_i R_s} \cdot \frac{s + 1/C_p R_p}{s + 1/C_f R_f} \cdot \frac{1}{(s + 1/C_i R_i)(s + 1/C_p (R_p \| R_s))}$$



- ASIC with 8 channels
- Variable gain (MIPs and high input charge up to ~ 10pC)
- C_{det} range ~ 0-500 pF
- 1st order shaper T_{peak} ~ 60 ns
- Power consumption < 9 mW/chan

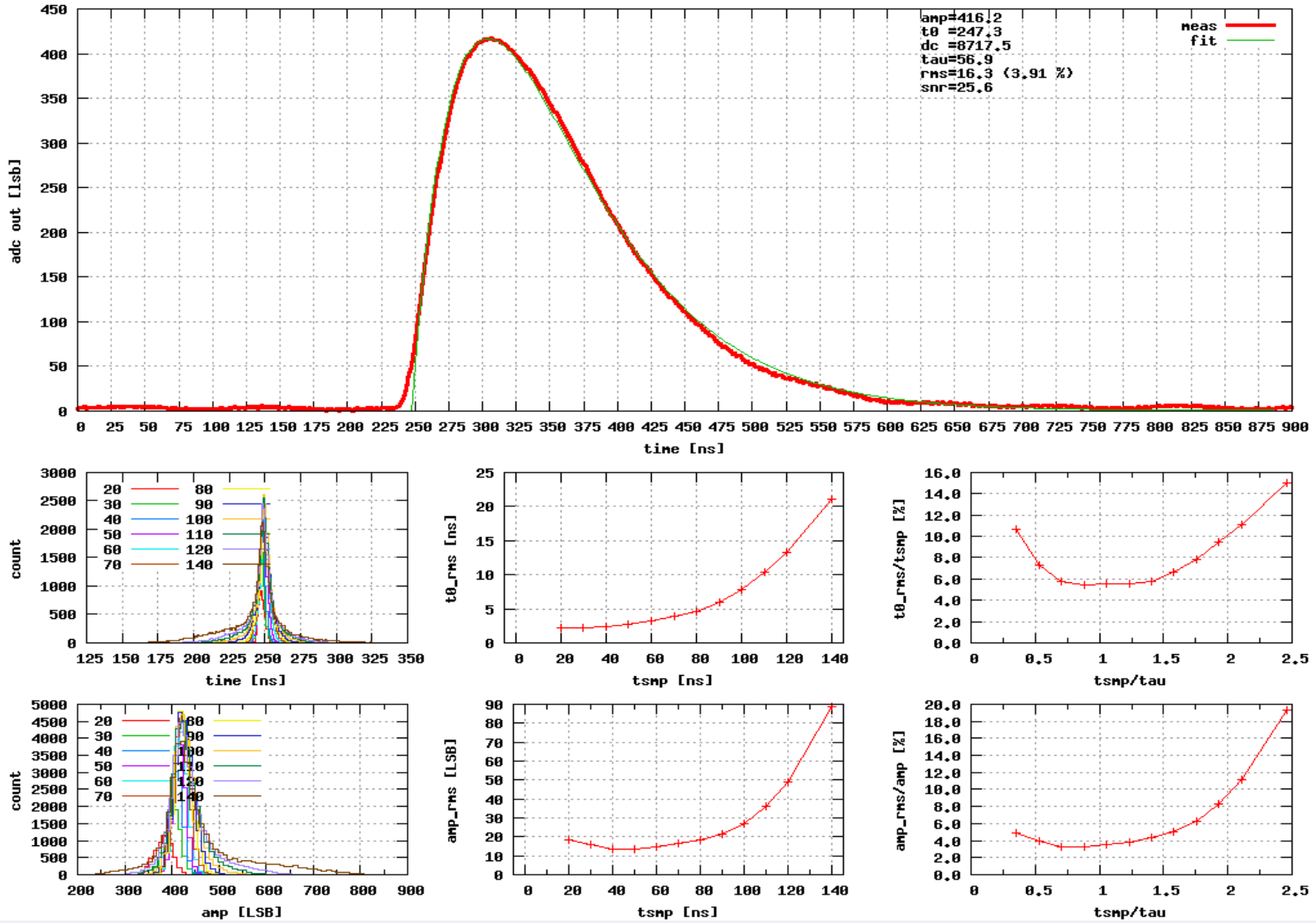
Test setup preparation



- Dedicated PCB board
- Silicon sensors for LumiCal
- Dedicated fanout
- 8 channel ASICs with preamplifier and shaper plus external buffers
- At present 8 channels external ADC (CAEN, our prototype has only 1 channel)

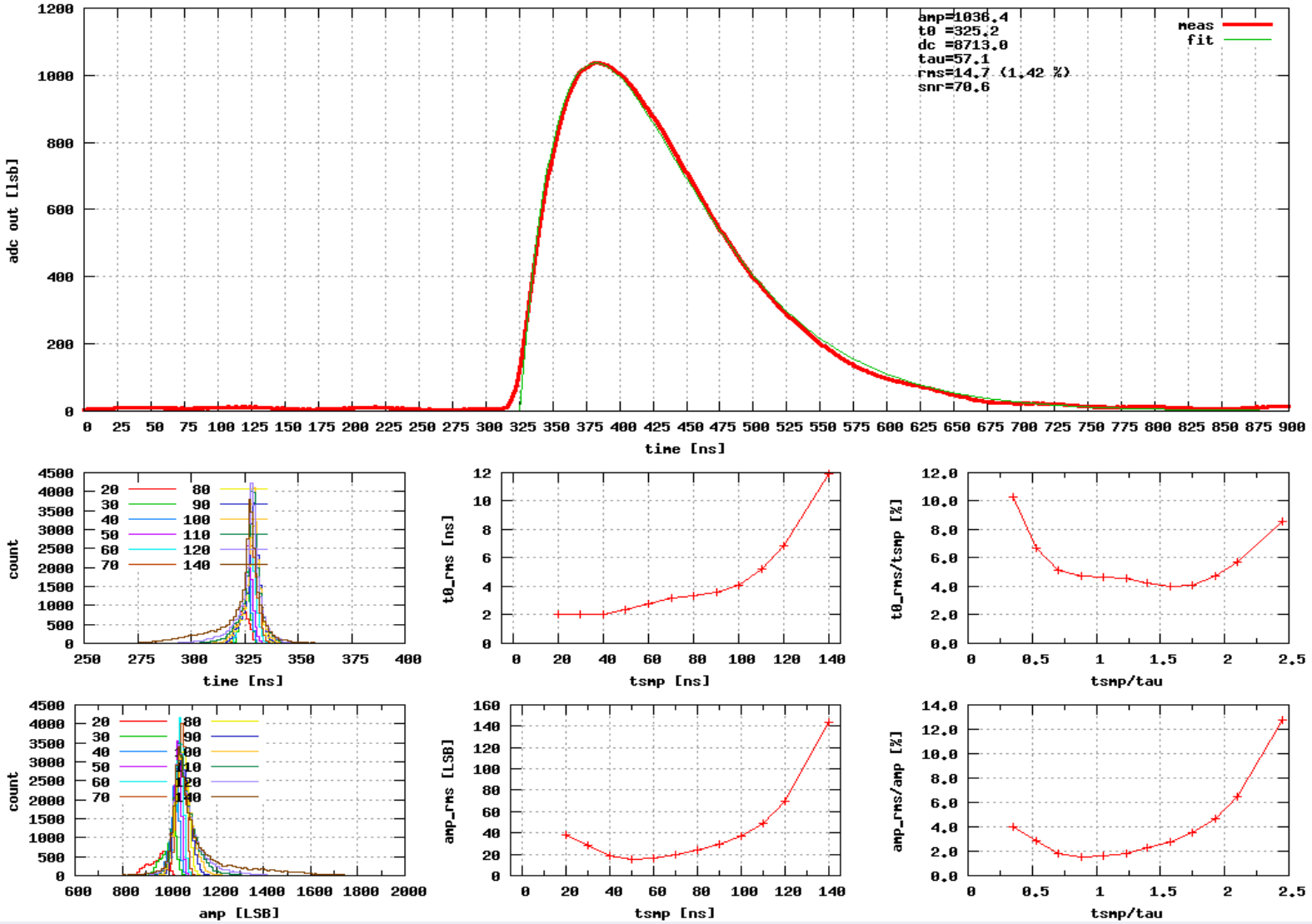
The results shown on next slides are obtained with electrical input test pulses – sensor not yet mounted

Measurements for S/N=25



$\Delta t/T_{sampling}$ resolution < 6%, Amplitude resolution ~ 3-4%

Measurements for S/N=70



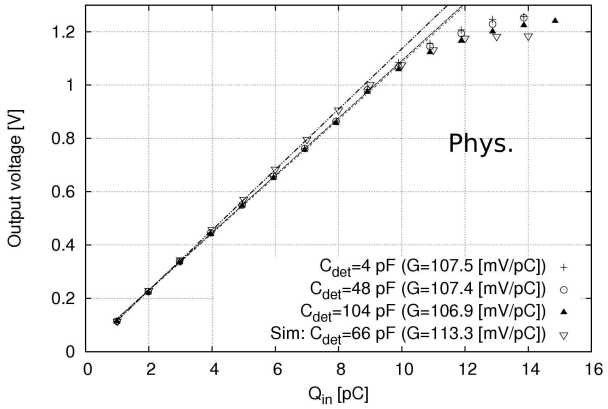
$\Delta t/T_{sampling}$ resolution ~4-5%, Amplitude resolution ~ 1.8%

Summary

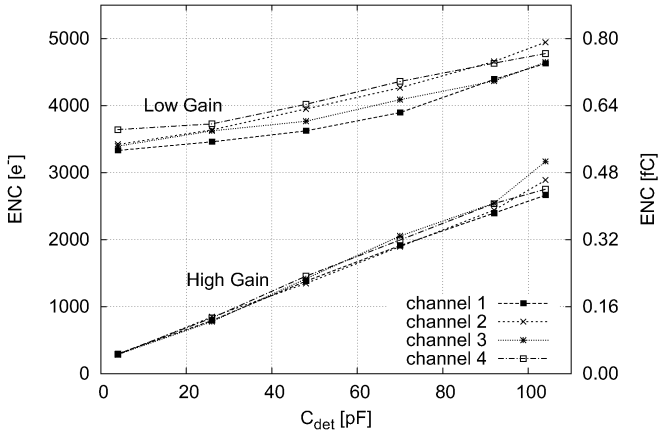
- Works on readout architecture with triggerless data sampling and signal deconvolution started:
  - Simulations studies with different shapers
  - Measurements with CR-RC shaper
- First measurements show promising results regarding timing and amplitude resolution
- Good agreement between simulations and measurements
- To be done:
  - Measurements with prototype multichannel ADC ASIC
  - Further ADC development (for less power)
  - Other shapers...
  - ...
- Thank you

Front-end measurements

Gain



Noise



Mode	Gain [mV/fC]	Noise@50pF [fC]	Linearity [pC]	Rate [MHz]	Crosstalk [%]
Physics	0.107	0.62	10	3	≈1
Calibration	≈20	0.28	0.035	2.5	≈0.1