

A detailed wireframe model of a roller coaster track. The track is shown in a perspective view, curving around the page. It features several loops, drops, and turns. The track is composed of multiple parallel lines, suggesting a multi-lane or multi-track system. The background is white, and the track is rendered in a light gray wireframe style.

# Quick Status Controls

Machine Meeting, 14.05.2019  
Ralph Bär

- Situation
  - Request was not known to ACO or IND (communication needs to be improved)
  - Estimated work: 1 (experienced) IND person x 1 week
  - IND team is fully occupied by UNILAC Vacuum Controls Upgrade, no availability
  - UNILAC = priority task, not to be interrupted
  
- Suggestion (already discussed and coordinated with VAC and IND)
  - Commissioning of bake-out extension right after UNILAC Project (week #45: 4.-8.11.2019)
  - Bake-out period immediately after (week #46: 11.-15.11.2019)
  - IND will try to do it earlier but on best-effort base
  
- Recurrent Comment
  - IND team must fully focus on FAIR activities from 2019 ff. in order to keep schedule plans
  - IND team has no capacity for technical support for already commissioned systems (e.g. CRYRING vacuum, UNILAC vacuum after completion, TVS, ...)
  - IND team cannot continue UNILAC vacuum controls upgrade for TK & EH
  - Needs to be further discussed with ACC division lead

# Status of some Controls Activities (intermediate)



- **General System**
  - Service break successfully done week #19
  - System upgraded (Linux OS, DB, Migration to Java11, OpenJDK, new FESA release, git repository, ...)
  - Extensive software tests scheduled for next week (Dry-run)
- **Storage Ring Mode**
  - Requirements and design complete
  - Project team formed and fully engaged and focused
  - First 2 software development sprints completed, implementation ongoing, project on track
- **Real-Time Issue in SCU (parallel LSA download during RT-Ramp execution)**
  - New SaftLib w/o D-Bus: significant performance gain achieved
  - Tests in DEV system: No RT hick-ups any more (testing to be continued)
  - Work around “all-pattern-stop” during LSA download not needed any more
- **Clock Synchronisation of MIL-FG (“16 sec issue”)**
  - Technical concept worked out (clock recovery from MIL transmissions)
  - Implementation starts now
  - In case of problems: fallback-solution available (cabling required)
- **DAQ-Functionality for SCU (reference value readback during ramps)**
  - Implementation on HDL and FESA level ongoing (SCU-bus and SCU-MIL-bus), on schedule
  - Internal review meeting imminent
- **New SIS18 Spill Abort System (fast-Quad, KO, CaveA/M features)**
  - Implementation ongoing: on schedule