The Silicon Tracking System (STS) readout chain

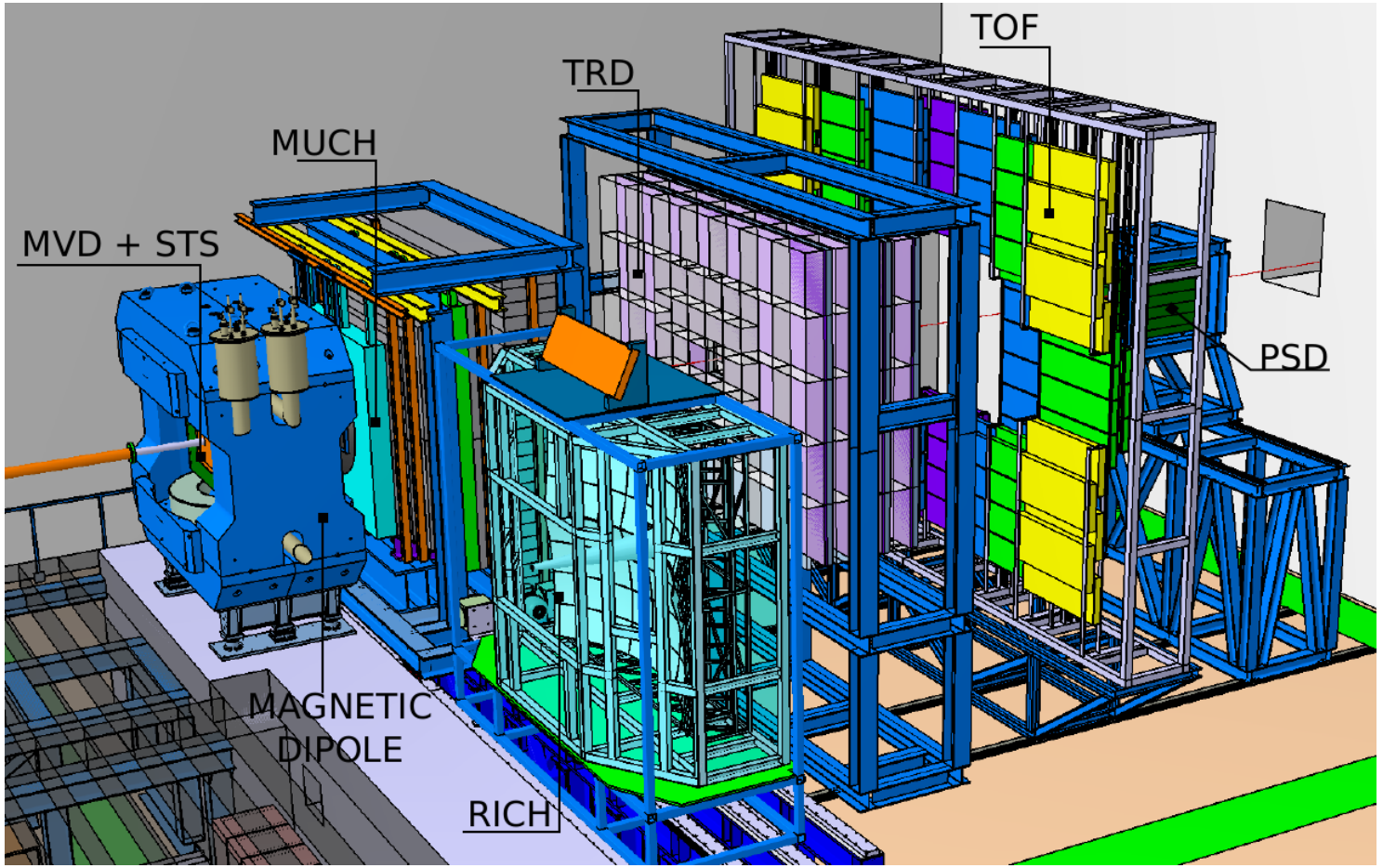
Adrian Rodriguez Rodriguez for the CBM Collaboration

DPG Spring meeting

München, March 19th, 2019

The Compressed Baryonic Matter experiment (CBM) at FAIR

Exploring the QCD phase diagram at high net baryon densities



→ 10^5-10^7 A+A collisions/s
→ Fast and radiation hard detectors
→ Self-triggering electronics
→ 4D event reconstruction.

Outline

→ Introduction to the CBM Silicon Tracking System

→ The STS readout chain design and implementation

→ Readout chain components:
:: Front-end electronics (FEE)
:: Readout board (ROB)
:: Data processing board (DPB)/Common readout interface (CRI)

→ Applications of the STS readout chain in the module assembly and test

→ The STS in the context of the mCBM beam campaign

→ Summary & outlook

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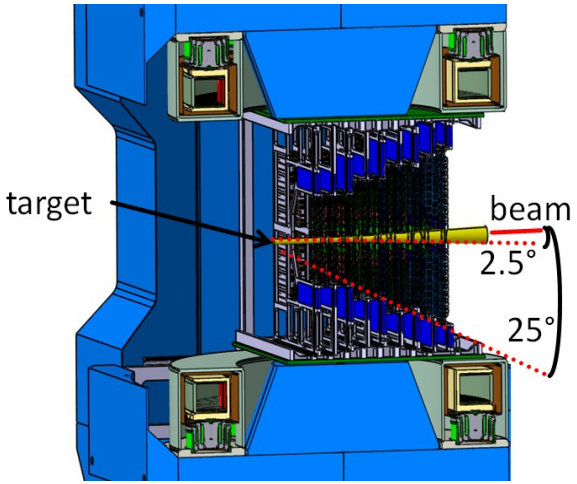
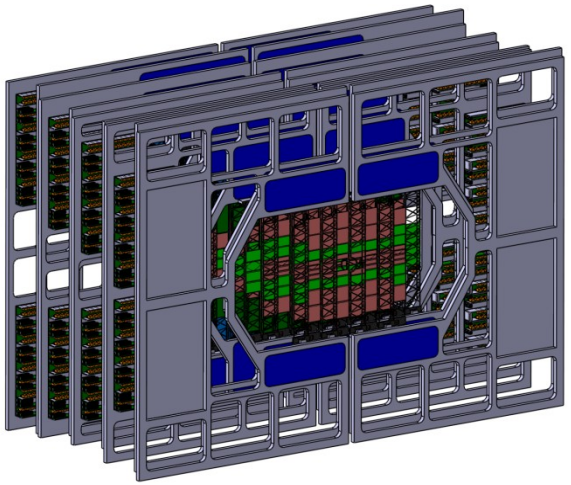
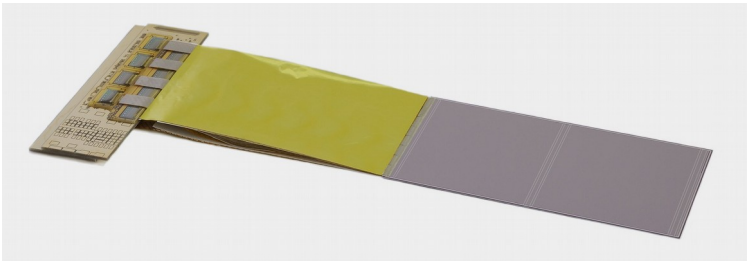
The Silicon Tracking System (STS) of the CBM experiment







Requirements & challenges:

→ High detection efficiency.
→ Momentum resolution: <2%
→ Tracking up to 1000 charged particles/collision.
→ Low material budget 0.3%-1.5% X_0 per station.
→ Ionizing dose at the electronics place ~200 krad/yr.
→ Power dissipation ~40 kW.

Wednesday, March 20, 2019, 17:45–18:00, HS 12
Performance simulations of the Silicon Tracking System of the CBM Experiment at FAIR
•
Evgeny Lavrik for the CBM collaboration

Design:

→ 8 tracking stations inside 1T magnetic field.
→ Based on ~ 900 double-sided Si sensors with 4 different sizes:
- 2x6 cm^2, 4x6 cm^2, 6x6 cm^2,12x6 cm^2.
- 7.5° stereo-angle for the p-side strips

→ Built as a functional module:
- 1 Si sensor + microcables + 2 FEB.
- 1 FEB carries 8 ASICs (1024 channels).

Wednesday, March 20, 2019, 16:30–17:00, HS 11
The Silicon Tracking System of the CBM Experiment
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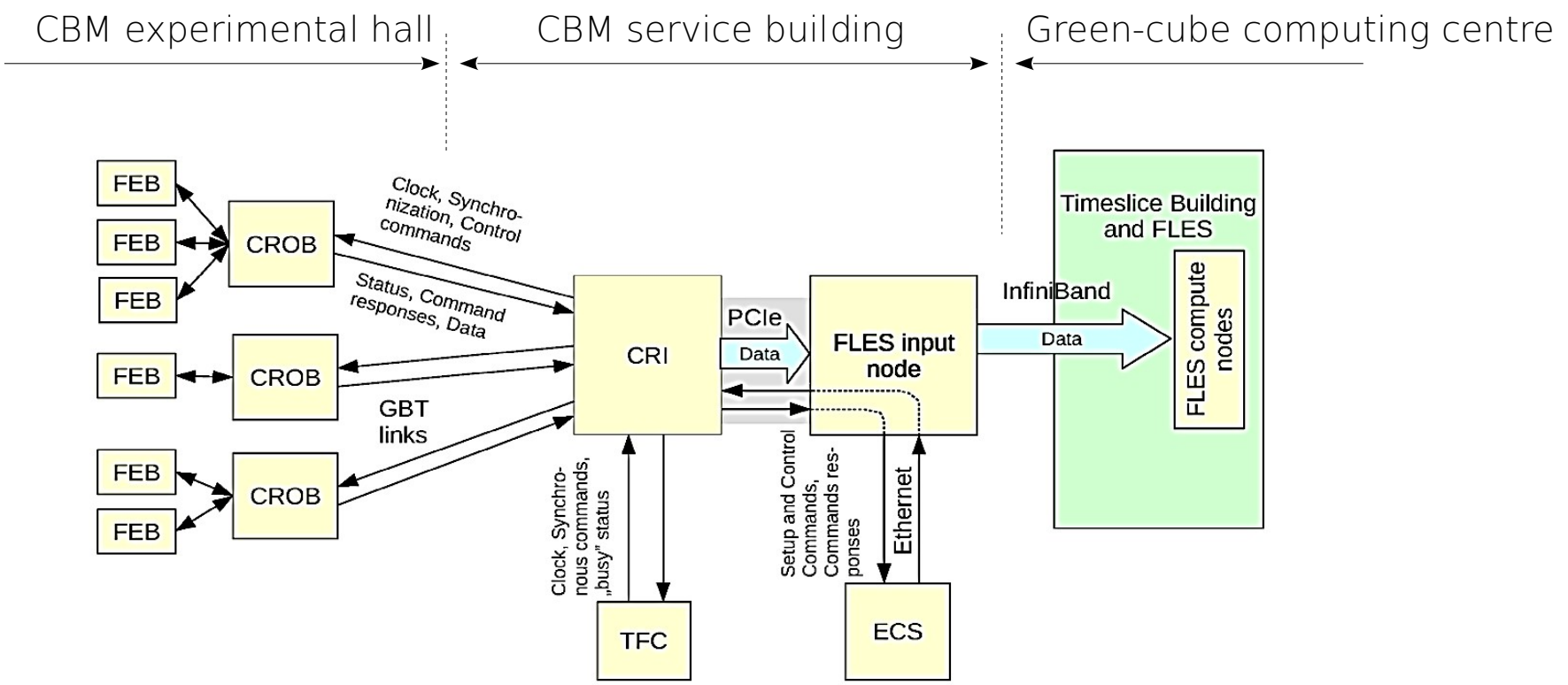
Ievgeniia Momot for the CBM collaboration

The STS readout chain



→ Front End Boards: Part of a functional module; it carries 8 STS-XYTER ASIC/FEB

→ Read Out Board: Based on CERN-GBTx and Versatile links components.

→ Common Readout Interface:FPGA based, interface for Timing and Control and data preprocessing

→ First Level Event Selector: Time slice building, full event reconstruction and online event selection

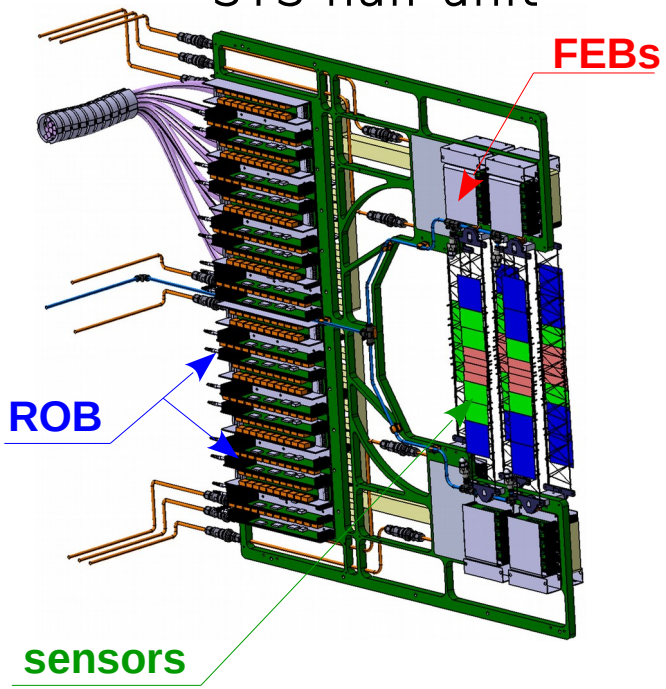
STS chain implementation in numbers

1752 FEBs
24000 electrical links
~30-80 cm

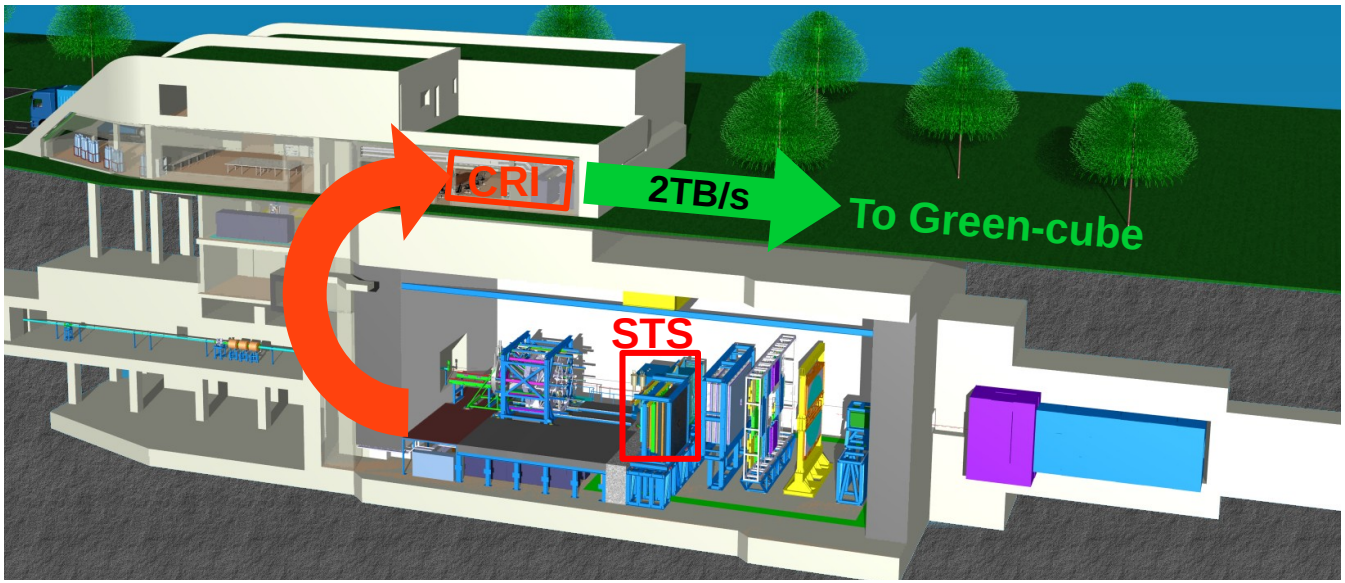
600 ROBs
2400 MM fibers
~50-80 m

78 DPBs
up to 624 SM fibers
~700 m

STS half unit



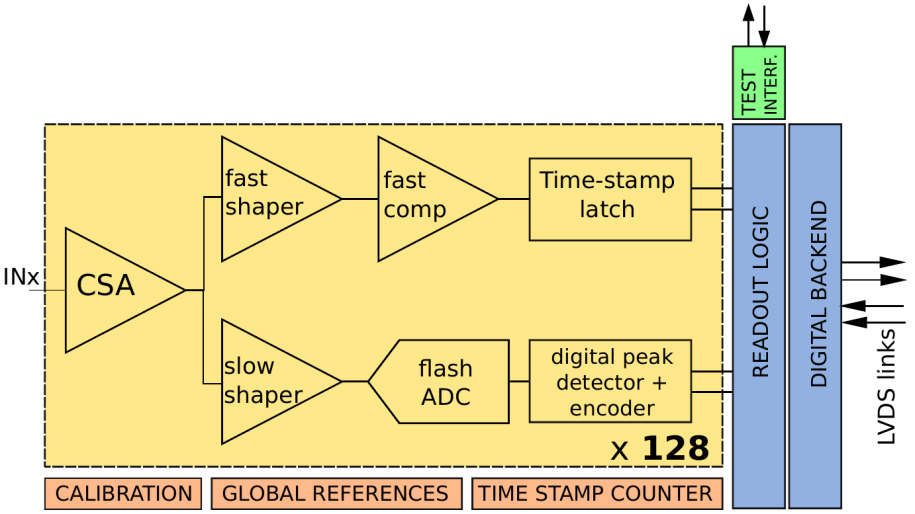
CBM building and cave



Front-end electronics

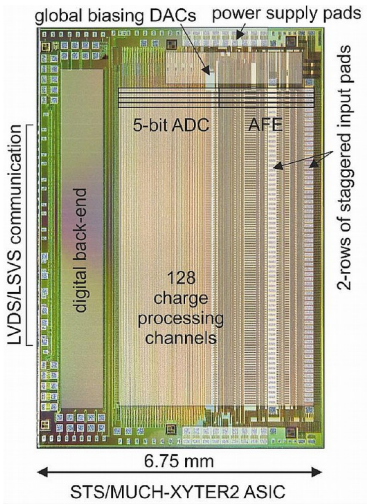
STS-XYTER front-end ASIC
STS+X,Y coordinate, Time and Energy Resolution

- Low power, self triggering ASIC
- 128 channels readout
- time resolution: ~5 ns
- 14 bit Time stamp
- 5 bit in-channel flash ADC
- ADC linearity range up to 15 fC
- radiation hard layout
- power consumption: <10 mW/ch
- digital backend compatible with the CERN-GBTx

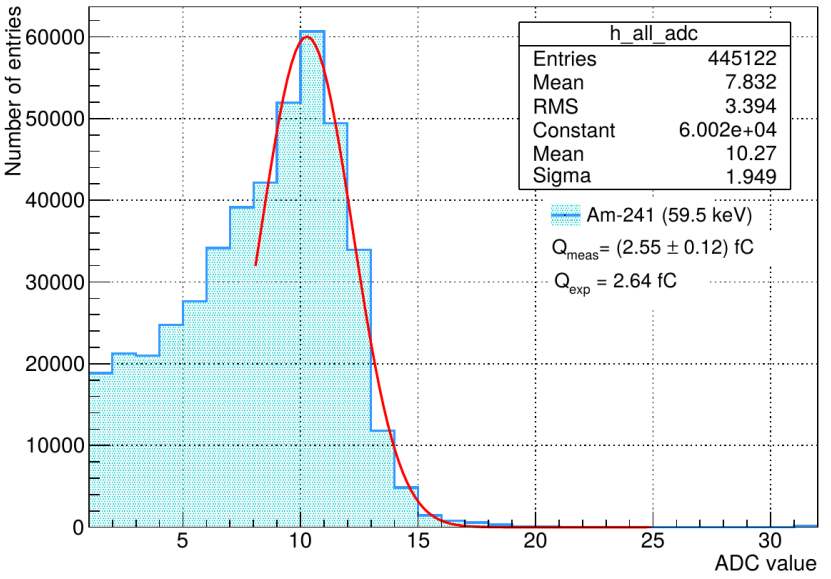


Block diagram of the STS-XYTER

AGH University of Science and Technology



Sensor readout using the STS-XYTERv2 (^{241}Am)



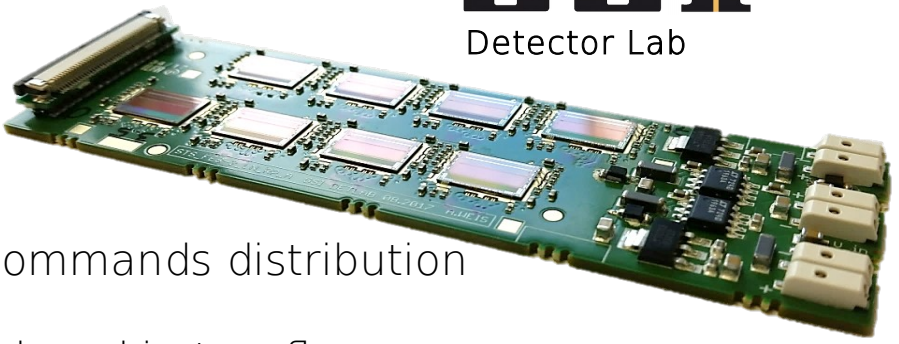
STATUS: STS-XYTERv2.1 with optimized features available since January 2019

Front-end electronics

Front-end board (FEB-8):

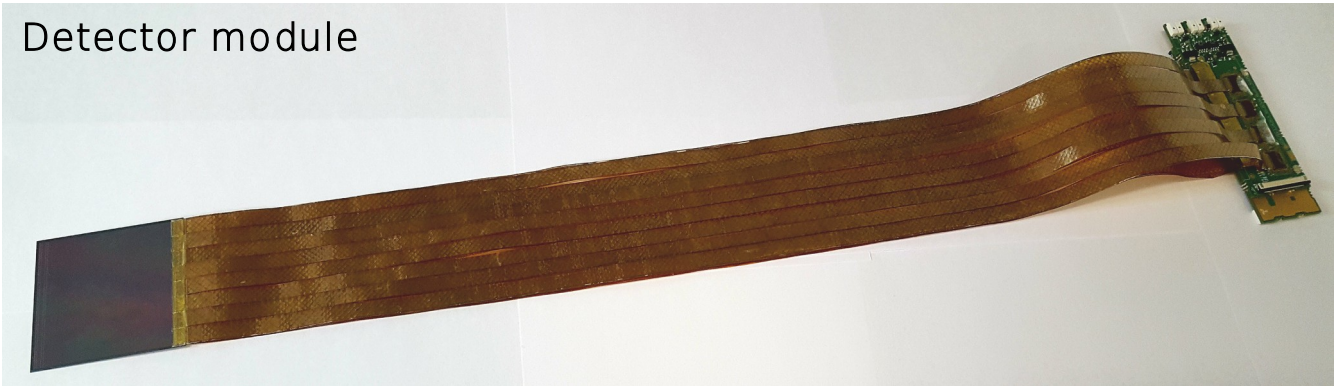
- carries 8 STS-XYTER ASICs (up to 5 LVDS links/ASIC)
- connected via micro-cables to the Si sensor
- **highly integrated (space, cooling)**

GSI Detector Lab



Allow to test the ASIC integration, clock and control commands distribution

STATUS: The prototype FEB-8 have been already produced in two flavours (FEB-A, FEB-B) to address module integration aspects



Full detector module assembled with 6x6 cm^2 sensor, 45 cm micro-cables and 2 FEB-8

Monday, March 18, 2019, 14:45–15:00, HS 12
High-density interconnection technologies for the CBM STS
•
Patrick Pfistner for the CBM collaboration

Monday, March 18, 2019, 15:45–16:00, HS 12
Ladder assembly procedure for the STS of the CBM Experiment
•
Shaifali Mehta for the CBM collaboration

Readout board

Common CBM prototype Readout Board (C-ROB)

for prototyping of all GBT based readout chains in CBM

- Full GBTx, SCA and Versatile Link functionality required for readout and control.
- STS: final ROB with different form factor, connectors, cooling features.

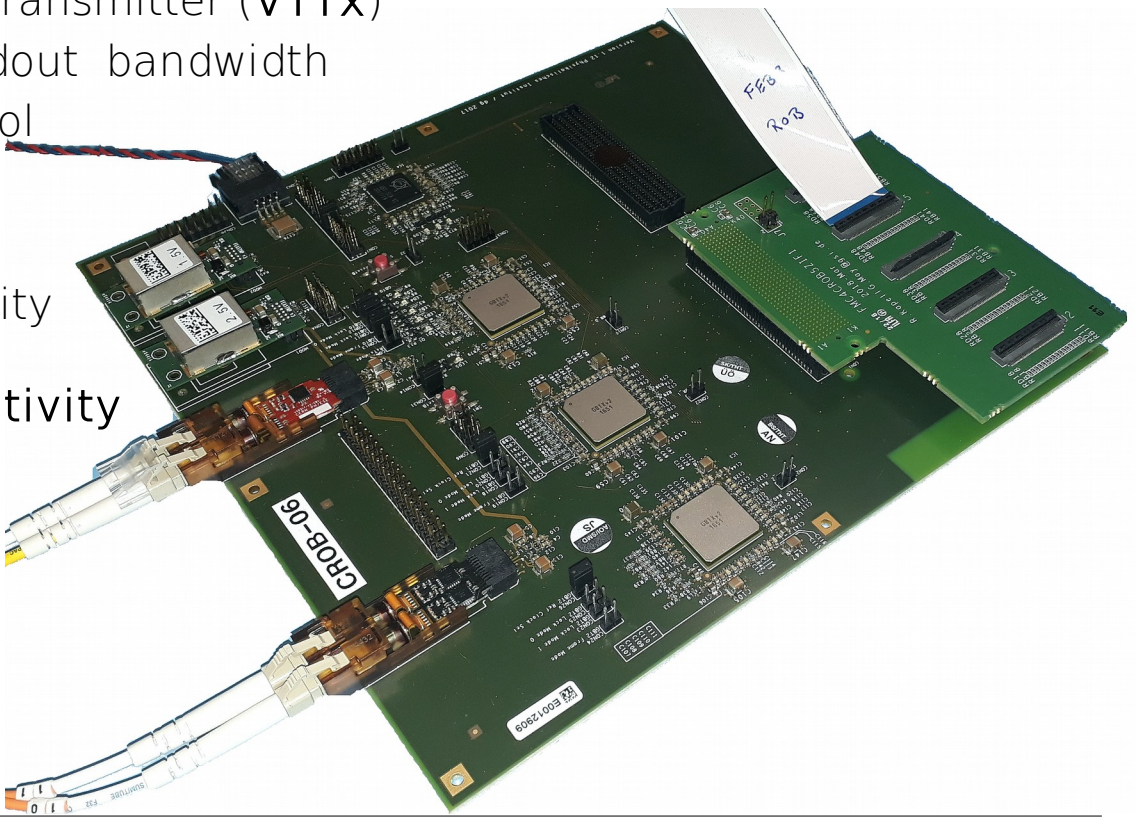
C-ROB features:

- 3 GBTx ASICs
  :: connect up to 40 STS-XYTER devices at 320 Mbps: hit readout, control responses
- 1 Optical Transceiver (VTRx) and 1 Twin Transmitter (VTTx)
  :: 3 optical uplinks : 13.44 Gbps total readout bandwidth
  :: 1 optical downlink at 3.2 Gbps for control
- 1 GBT SCA
  :: I2C interface for control of slave GBTx
  :: additional multi purpose SCA functionality

FMC connector with all frontend connectivity

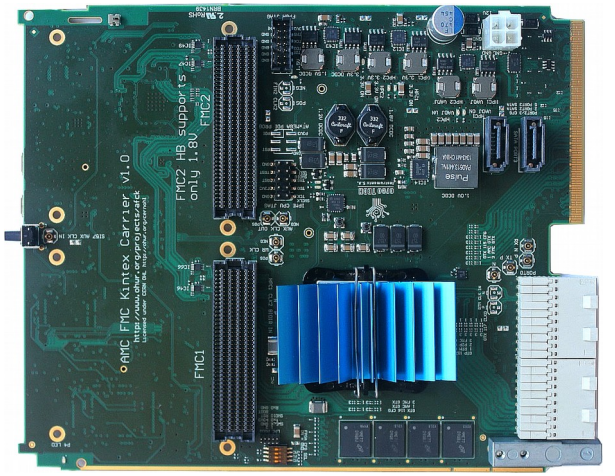
- GBTx E-Links
- required and useful SCA functionality
- flexibly connect any FEE prototype

STATUS: Available since Q4 2017



Data Processing Board

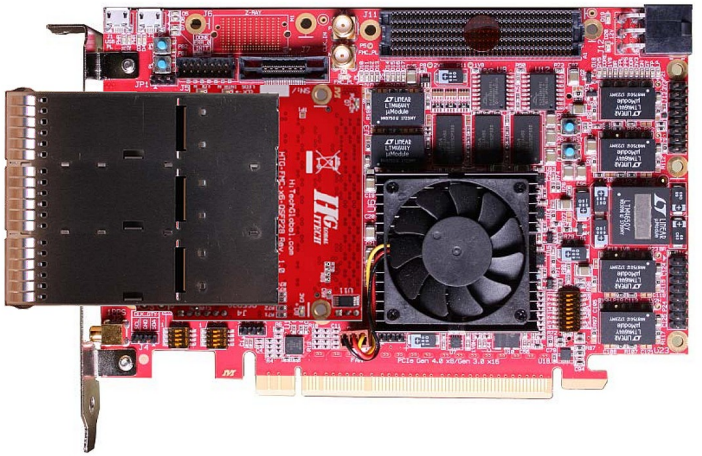
AMC FMC Carrier Kintex (AFCK) as DPB prototype available
- µTCA board
- also standalone operation
- Xilinx Kintex-7 325T FPGA
- 2 FMC (HPC) and RTM connectors
- multiple interface cards available



Flexible test and development platform:
- use with various FMC interfaces for prototype readout chains.
- firmware and software development DAQ systems for detector testing

STATUS: Currently it is used as the main DPB in all the DAQ systems available.
From Lab detector's testing until full mSTS demonstrator

Prototype (CRI) based on the HTG-Z920 board
- it will cover the functionality of both the DPB and FLIB in a single FPGA board
- simplify the hardware/firmware design



STATUS: First boards available.
Testing firmware in the development phase

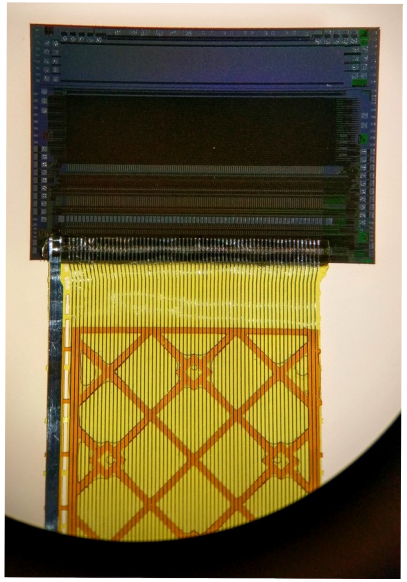
Readout chains for STS

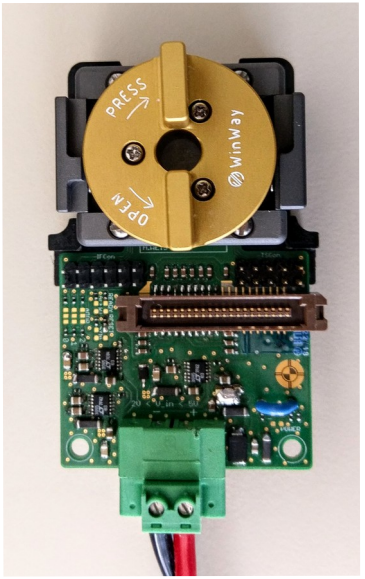
Development of **multiple DPB flavors** with different firmware and hardware components for various readout chains:

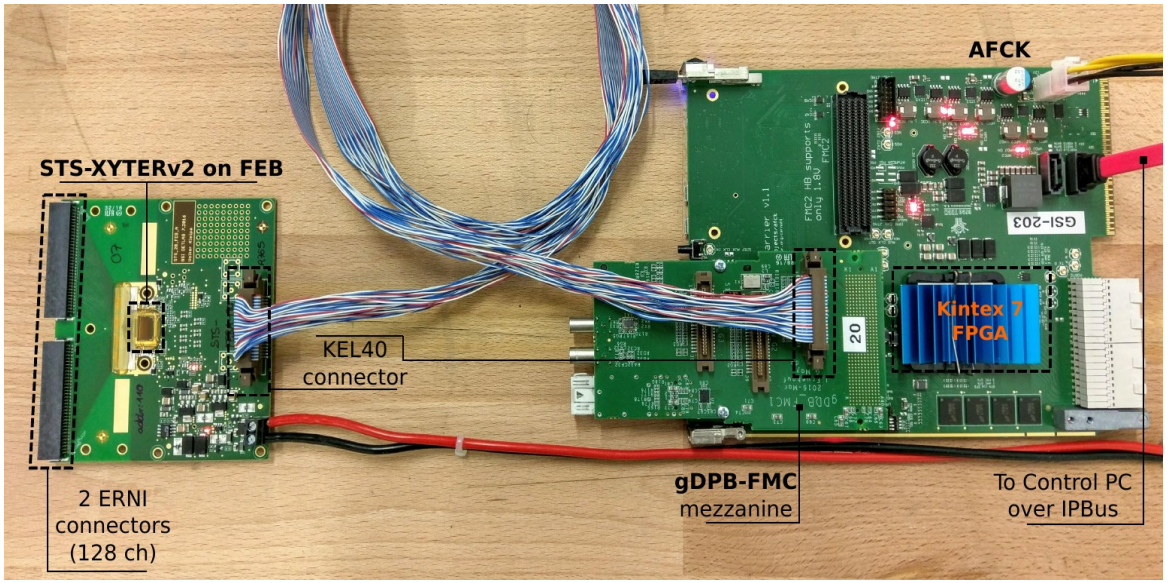
Purpose	Readout	Chain description
ASIC testing & QA	Pogo-pin station Prototype FEB (1 ASIC)	Standalone system DPB e-link flavour AFCK based
Full module testing	Test-box system - FEB-8 - Full module readout	DPB GBTx flavour AFCK based
mSTS	Several module readout	Full readout chain prototype - AFCK based (2018-2019) - CRI based (2019+)

ASIC testing & QA

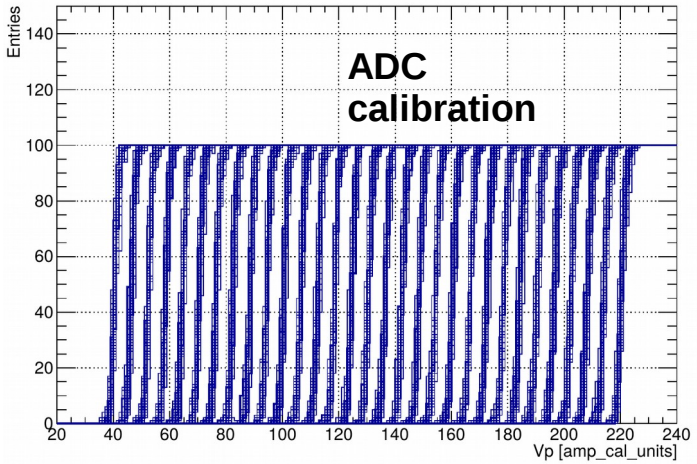
AFCK based readout chain for ASIC tests and QA

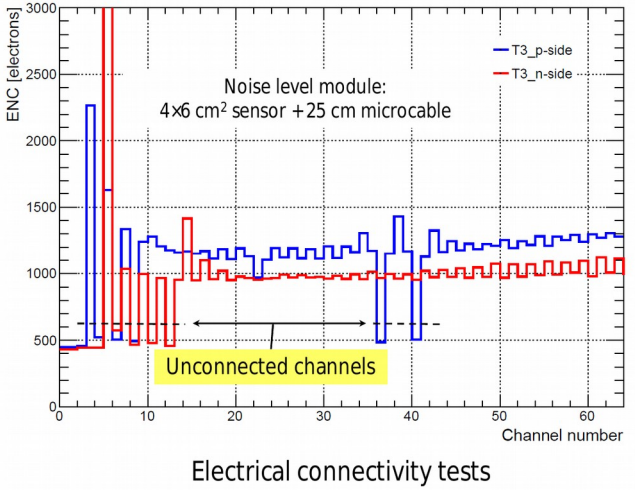


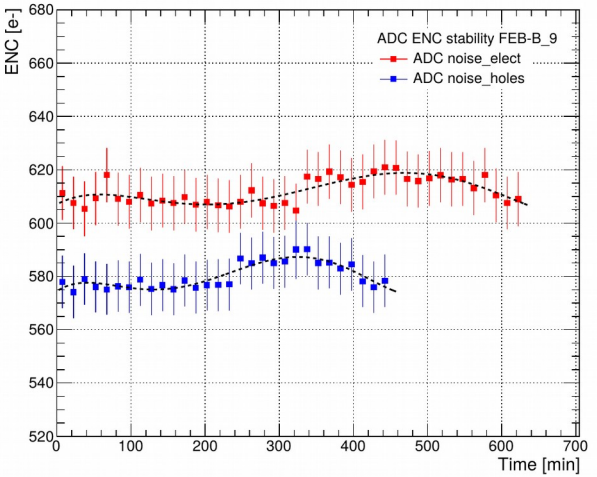




Examples of ASIC test: ADC calibration, noise readout, connectivity check, long term stability







mSTS

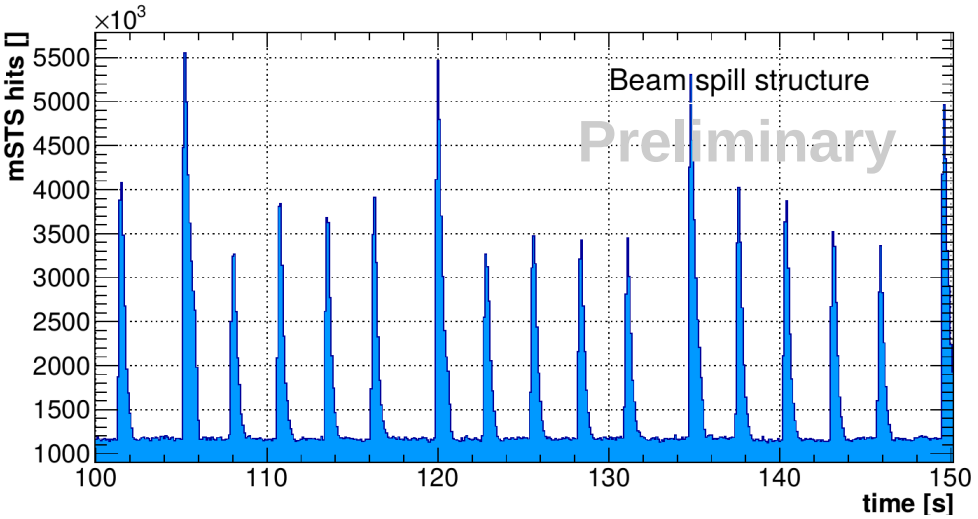
mCBM: CBM full test setup for high rate, nucleus-nucleus collisions at GSI/FAIR

GOALS:

- demonstrator for full CBM data taking and analysis
- integrating prototype detector's modules into a common, free-streaming DAQ

mSTS:

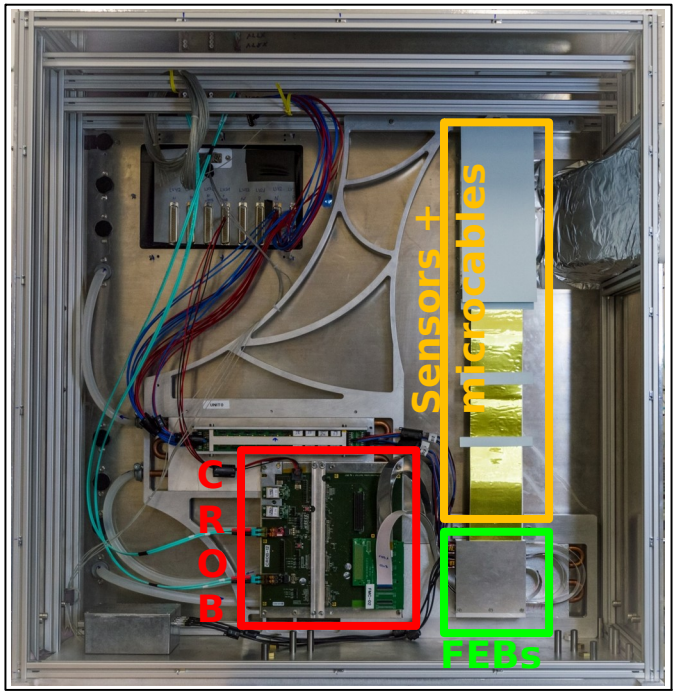
- 2 tracking stations
- 13 detector modules
- more than 26000 readout channels
- 8 ROB (13 GBps)



Beam spill structure monitored in mSTS during commissioning run. December 2018

mSTS

Installation in the beam line



Service box of mSTS containing ½ station

STATUS: First station installation is completed.
Data taking is ongoing

Monday, March 18, 2019, 16:30–17:00, HS 12
Status of the mCBM@SIS18 experiment at GSI/FAIR
•
Christian Sturm for the CBM collaboration

Summary and Outlook

Front-end Board, Readout Board and Common Readout Interface are the major components of CBM Silicon Tracking System readout chain:

- Prototype **FEB** with 8 STS-XYTER ASICS have been produced and tested.

- The STS-XYTERv2.1 is available since January 2019.
  :: Two detector modules have been assembled and they are fully operational in mSTS.

- Common **ROB** has been successfully operated in multiple subsystems readout chains.

- Common **DPB** hardware based on the FPGA board functions used for various development and prototype readout chains.
  :: modular approach: two DPB flavours used in the module assembly and testing

- Final STS readout chain based on the **CRI** board. Possible CRI FPGA candidate has been identified and it is currently in the testing and firmware developing phase

- mSTS project (testing setup for detector and full readout chain) is ongoing.

mCBM is a demonstrator for the CBM data taking and analysis chain
(operational since December 2018)

Thanks for your attention!