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CBM DENEYİNDEKİ ÇİFT TARAFLI SİLİKON MİKRO-ŞERİT DEDEKTÖR SİSTEMİNİN KARAKTERİZASYONU

Merve DOĞAN

Fizik Anabilim Dalı

Nükleer Fizik Programı

DANIŞMAN
Prof. Dr. Ela GANİOĞLU NUTKU

II. DANIŞMAN
Dr. Christian J. SCHMIDT

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İSTANBUL

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First of all, my dear CBM group, It was a pleasure to meet you and work with you. Thank you all for your efforts and sharings.

I would like to dedicate this thesis to Dr. Christian SCHMIDT, who has believed in me from the beginning and has always encouraged me. It was a great chance for me to benefit from his knowledge and experience.

Eylül 2019 Merve DOĞAN

SUMMARY

Ph.D. THESIS

Merve DOGAN

CHARACTERIZATION of DOUBLE SIDED SILICON MICRO-STRIP DETECTOR SYSTEM in CBM EXPERIMENT

İstanbul University

Institute of Graduate Studies in Sciences

Department of Physics

Supervisor : Prof. Dr. Ela GANIOGLU NUTKU
Co-Supervisor : Dr. Christian J. SCHMIDT

The compressed baryonic matter (CBM) experiment will examine the behaviour of nuclear matter in early universe and will be one of the major experiment in Facility for Antiproton and Ion Research Center (FAIR). In order to determine the type of the particles, momentum, energy and charges sub-detector systems will be used. The silicon Tracking System (STS) is the core detector system of the CBM experiment that provides momentum and tracking information of the charged particles. Among the electronic parts, the STS-XYTER ASIC constitutes one of the important component of the CBM environment since it is the dedicated electronic for the read-out from double sided silicon micro strip detectors. Therefore, basic ASIC functionalities enable to be checked with a prototype pogo-pin station. In this thesis, the assembly of the detector modules to be used in the STS system, the quality assurance test protocol and the results of the STS-XYTER ASIC willl be given. Studies in this thesis will also constitute one of the fundemental values as a reference for the upcoming mini CBM and CBM experiment.

Keywords: FAIR, CBM, Silicon Tracking System, STS-XYTER ASIC, Silicon Micro-Strip Sensor

CONTENTS

1. INTRODUCTION

1.1. FAIR

The Facility for Antiproton and Ion Research (FAIR) is one of the biggest research center in Darmstadt, Germany which will provide high energy beams of antiproton and ions with remarkable quality and intensities. FAIR is going to operate SIS100 synchrotron accelerator to accelerate particles from protons to the heaviest element uranium with the help of electric and magnetic field. Such ions will be used to create radioactive ions. Before the beam transfer to SIS100, UNILAC will pre-accelerate the particles. In order to use highest beam intensity in experiments from synchrotrons and other accelerators, the operation of FAIR is planned to be particularly versatile with carrying out five different particle beams at the same time in that up to five research programmes. In addition, four scientific programs will be the main research activities at FAIR: the NUclear Structure and Reactions program (NUSTAR) for detailed studies of nuclei that are far from stability, the Atomic, Plasma Physics and Applications program (APPA) in order to determine the atomic structure and extraordinary plasma, the Compressed Baryonic Matter program (CBM) targeted at the study of the QCD phase diagram and microscopic properties of strongly interacting matter at high baryon densities and finally the hadron structure and dynamics program (PANDA) for the structure of hadrons and exotic states of matter [1]. Though, the compressed baryonic matter (CBM) experiment will be one of the major experiment in FAIR which will examine the high energy collisions between heavy nuclei to determine the behaviour of nuclear matter in a range of densities supernova explosions and neutron stars. In such high density states, protons and neutrons are foreseen to melt into a quark-gluon plasma. Such phase process can only be observed at very high energies which provided by the FAIR accelerators [2].

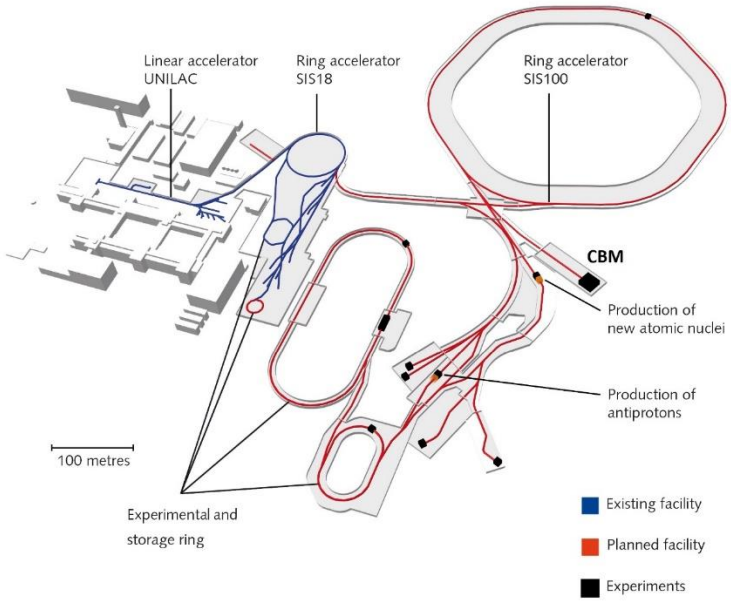

Figure 1.1: Fair Facility [2]

1.2. THE COMPRESSED BARYONIC MATTER PHYSICS

The Compressed Baryonic Matter (CBM) experiment is one of the prominent experiment of the future Facility for Antiproton and Ion Research (FAIR) in Darmstadt. It is possible to determine 10^7 interactions per second, a rate will allow to examine rare events [3]. In order to perform such high rate experiments, accelerators that are enable to accelerate nuclei to the high energies are needed and the most efficient one is synchrotron. It can be operate at more than a million turns per second and is a circular accelerator that work a bit like hammer throwers. The ionised particles gain more energy through alternating electric field in each turn and magnets hold them on their circular orbits inside the ring.When the intended beam energy is reached, ions are directed onto a suitable target [4].

With this design, the SIS100 synchrotron accelerator operating for hadron physics at FAIR provides primary beams of protons and uranium up to 89 GeV and 35 AGeV respectively as well as nuclei with $Z/A = 0.5$ of up to 45 *AGeV* with extraordinary quality in order to study the structure of neutron stars and cores of collapsed supernovae. It is possible to achive the correspnding nuclear matter density at energy densities of up to 2.5 *GeV*/fm^3 and baryon densities of about 35GeV and 11 AGeV with SIS100 respectively [5]**.** The preliminary aim of the Compressed Baryonic Matter Experiment is to investigate the QCD phase diagram of strongly interacting particles at high baryon densities which can be generated at SIS100. To this end, a high energetic heavy ion beam is shot onto a target foil. A collision of nuclei results in a shower of secondary particles that can be identified and characterized in the laboratory for determination of the kinetic parameters to study the dynamics of the collision. The secondary particles which need to be identified are leptons and hadrons. In the events, including charm or lepton pairs with 1000 charged particles at reaction rate up to 10 MHz. In neutron stars, nuclear matter of higher densities exists and as well as it is foreseened that strongly interacting matter in the form of a hot *quark-gluon plasma* (QGP) came up during the first microseconds of the early universe [4].

At baryon high densities, phase transitions is a structure in the phase diagram. The nucleons behave like a gas at low densities. When density and temperature are increased nucleons are excited into baryon resonances which decay into pions and nucleons afterwards. Hadronic matter called as the mixture of nucleons, baryonic resonances and mesons. This hadronic phase can be seen as the white area in figure 1.2. At very high temperature, hadrons melt and their components, the quarks and gluons, generate a phase called quark-gluon plasma. This deconfinement phase transition from hadronic matter to quark-gluon matter occurs at a baryon density zero (170 MeV) that is 130 thousand times hotter than the interior of the sun. After the big bang, these circumstances prevailed in the early universe for a few microseconds and it is possible to be studied in heavy ion collisions [6]**.**

Herewith, the main idea mentioned above for the CBM experiment can be summarized in two steps like to identify electrons, positrons and charged hadrons including all mother particles that have decay branches into these particles and secondly to measure dimuon pairs that observed from vector meson decay including charmonium [7].

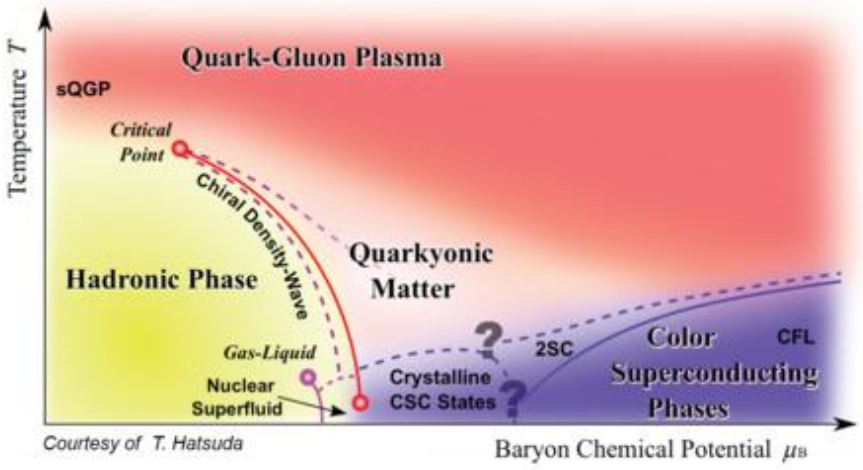

Figure 1.2: Schematic of the prospected phase diagram of strongly interacting matte [6].

Furthermore, experimental research of the CBM will clarify some kind of astrophysical issues such as [4]:

- What does matter look like under the very large gravitational pressure in the interior of neutron stars?
- Do nucleons still exist there or does matter melt into matter of quarks?
- What limits the total mass of a neutron star?
- How does a *super nova* collapse and the subsequent explosion of the burnt out star evolve?
- Do such processes create the composition of elements that we find in our planetary system?

1.3. EXPERIMENTAL OBSERVABLES

The greatest challenge in the CBM Experiment is to find the prospected phase transition and diagnostic probes in chrial symmetry. Observation of hadrons might be a proof for beginning of the chiral symmetry restoration. Since the decay of short-lived vector mesons into dilepton pairs is observable, they can be measured directly. On the other hand, it has been estimated that abnormal overpressure of charmonium due to screening effects in the Quark Gluon Plasma (QGP) is an experimental signal of the QGP. Particles that contain heavy quarks, such as charm, are produced in the first stage of the collision. The study of the production of open and hidden charm is planned at FAIR and the production mechanisms of D and J/ψ mesons are thought to be sensitive to the conditions inside the early fire ball [8]. The phase that is called freeze-out is the phase in the final, expected state after the collision in which there are no new particle production. Studies of this phase enable with the measurement of bulk observables. On the other side, by measuring the rare probes that is to say secondary particles with heavy quarks such as Λ, Σ, Ξ, Ω, J/Ψ, D.., it is possible to obtain some information about the earlier phases. By the way of some measurements such as mass distributions of dileptons, measurement of multi-differential observables such as the flows of identified particles as a function of the transverse momentum and mass distribution of particles involving heavy quarks as a function of

momentum; information on the early and dense phase of the fireball evolution can be obtained. Conditionally, such measurements require fast detection systems [9]**.**

Potential observables are listed below [10]:

1- ρ,ω and ϕ as a low-mass vector mesons which decay into e^- e^+ pairs to obtain restoration of chiral symmetry in dense baryonic matter.
2- Charmonium, D mesons for the processes of in medium production and for the properties of highly compressed strongly interacting matter.
3- Λ, Ξ, Ω particles (multi strange baryons). They are thought to be sensitive to the dense and early stage of the collision.
4- Observables like collective flow and critical event by event fluctuations that promise information on the existence of a critical point.
5- Thermal photons from the dense and hot fireball and direct photons of first collisions.
6- Pentaquarks, bound kaonic systems etc.

Particles such as electrons, protons and positrons are usually accelerated to energies in the GeV for high energy experiments and instead of primary particles especially secondary particles are examined since they are comperatively more stable. Type of the particles, momentum, energy and as well as charges are detectable quantities of those interactions. In order to detect such kind of variables sub-detector systems which can be used for each quantities, are preferable than one detector. Those sub systems can briefly explain like below:

- In order to measure the direction of a particle vertex detector is used in the system and it should be near the interraction point to be able to decrise extrapolation errors.
- to measure the curvature of the charged particles in magnetic field, a tracking station is used to determine the momentum of the particles.

to measure the energy of electrons and photons electromagnetic calorimeters with a high atomic number material, are needed. Hadrons (protons, neutrons, pions, kaons) penetrate the electromagnetic calorimeter but interact in the hadron calorimeter [11].

2. GENERAL PARTS

2.1. CBM DETECTORS

The experimental set up has to fulfil some requirements listed below [10]:

- enable to identfy the electrons with a pion suppression factor as high as 10^4
- hadron identification with large acceptance
- high granularity for detectors
- fast read out system
- low dead time for detector
- radiation hardness for electronics and detectors
- high speed data acquisition

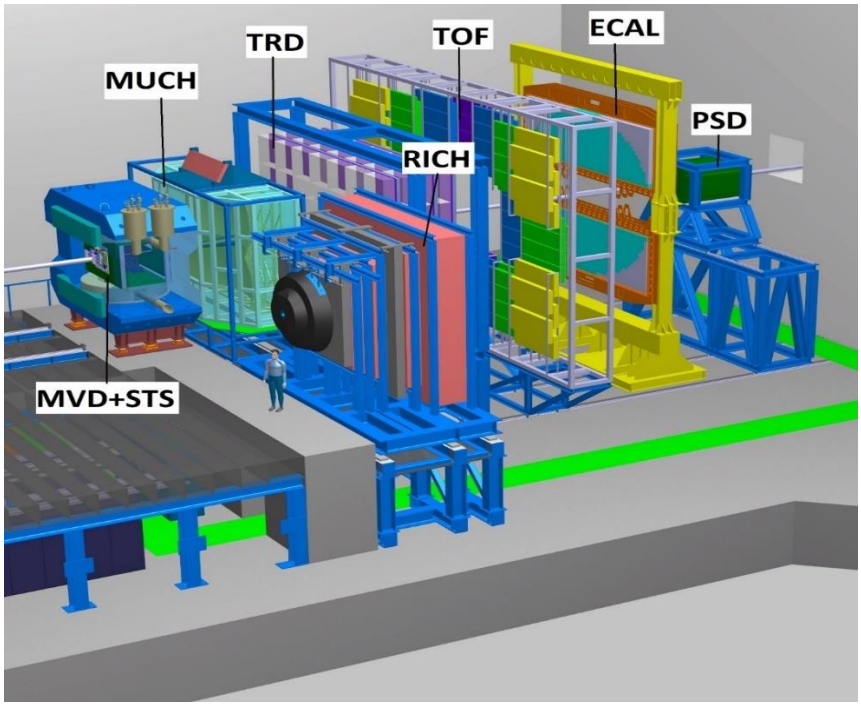

Figure 2.1: CBM Experimental set-up.

Dipol Magnet: The dipol magnet is used to provide a vertical magnetic field in while the secondary particles travel. It serves to identify the momentum of the particles through the track curvature which is used to place STS system has a gap between the pole tips of 1.44m vertically and 3.m horizontally. The length along the beam is 1.5 m with a stored energy of approximately 5MJ. The magnet type is H-type with warm iron yoke as well as cylindirical superconducting coils. Opening angles are respectively ±25° vertically and ±30° horizontally as seen from the target. Inside the dipol magnet, the operating current is 686A with maximum magnetic field about 3.9 T in the coils that is made of rustproof steel [12].

The Micro-Vertex Detector (MVD): The MVD system will be used for dielectron analysis and for track reconstruction with together the STS. It is thought to assembly as close to the target in order to provide secondary vertex resolution. Acceptance of the first system will have a smaller polar angle based on radiation dose, however, the assembly condition for the last two MVD stations had better to be as close to STS to enhance the assignment of hits to tracks reconstructed in the STS [13]**.**

The Ring Imaging Cherenkov Detector (RICH): In the CBM experiment it is obligatory for the physics analysis to seperate the pions and electrons. For this purpose, the RICH detector is used in CBM. It will serve to identify the electrons in a range up to 8 to 10 GeV/c. The RICH detector is planned to be placed behind the Silicon Tracking System to measure the low mass vector mesons at SIS100 [14]. It consists of a radiator that is CO_2 gas at 0 ° C temperature, two photon detector and two planes of concave mirrors [15].

The Muon Chamber System (MUCH): The MUCH can be allocated in plane of the RICH for the CBM muon configuration. It serves to track muons through a stack of hadron stopping absorber. This system is planned to be allocated downstream of the silicon tracking system and it consists of triplet detector planes between several hadron absorber layers which are made from iron plates of thickness 20 cm, 20 cm, 20 cm, 30 cm, 35 cm, 100 cm respectively. In addition, It consists 15-18 gaseous tracking chambers in triplet detector system behind every iron planes [16].

The Transition Radiation Detector (TRD): The Transition Radiation Detector will be used for both muon and electron configurations. In the moun configuration, the TRD merely serves as additional tracking planes to enhance tracking by using their energy loss features in the detector volume and was designed as three detector stations in approximately 600 m^2 area. Stability at high interaction rates, identification of charged particles and tracking and pion rejection capabilities are the important parameters for the TRD System [17].

Electromagnetic Calorimeter (ECAL): The Electromagnetic calorimeter system is planned to be used for neutral mesons that decay into photons as well as for direct photons. The ECAL System will comprise 140 modules of sandwich layers of 1 mm lead and 1mm scintillator. ECAL module has the size of 3 x 3 cm2, 6 x 6 cm2 and 12 x 12 cm2. These layers are considered to allow a flexible position according to the target [18].

Projectile Spectator Detector (PSD): In order to adjust the collision centrality and to measure the energy distribution, a Projectile Spectator Detector (PSD) was designed for the CBM environment. It is made of a lead-scintillator calorimeter which provides adequate energy resolution. It is a significant issue to determine the number of nucleons that participate is a collision in order to predict the collision centrality. These particles are those knocking the beam nuclei that overlap with target nuclei. The PSD system is planned to be composed of 44 systems

around the beam position with a relatively large area where projectile particles loose their most of their energy [19].

TOF: The Time-of-flight system is planned to be used with the purpose of measuring the speed of flight of secondary partcles in order to identify hadrons. It consists of a resistive-plate chamber with multi gaps. It will placed between 6m and 10m downstream from the interaction target covering the full aperture of the angles of 2.5^0 to 25^0 in an area that is $120m^2$. About 80 ps resolution is necessary for the system [20].

Beam Pipe

The beam pipe in the CBM system is made of a resistant material and has less interaction with the particles. Beryllium is used mostly in many experiments because of its thickness against the pressure reist for chamber Wall [21]. The beam pipe has 0.5 mm thickness and will cross the detector, ın addition it is linked to the target chamber on the beam upstream side. It further has a connection downstream STS Wall with RICH or MUCH detectors [22].

As it is seen in figure 2.2, for the CBM beam pipe two design have been developed with FLUKA calculations. This two design has the same sequence through the STS, RICH and MuCh, followed by a bellow that provides a skew of the subsequent beam pipe with angles between 0.7 and 1.8 degrees for Au beams. In one version, the beam pipe has a 16.16 cm Radius up to the entrance of the PSD then the radius becomes narrow as 9.5 cm. In order to center the beam in the pipe, narrower pipe is horizontally displaced by 5 cm in comparizon with the wider one. Furthermore, In the other design, the beam pipe has a 9.5 cm radius that starts after the bellow with a horizontal displacement of 6.5 cm. As a next step the beam pipe models will be used in physics simulations with the intend to study the impact of the additional background radiation on the performance of particle identification [23].

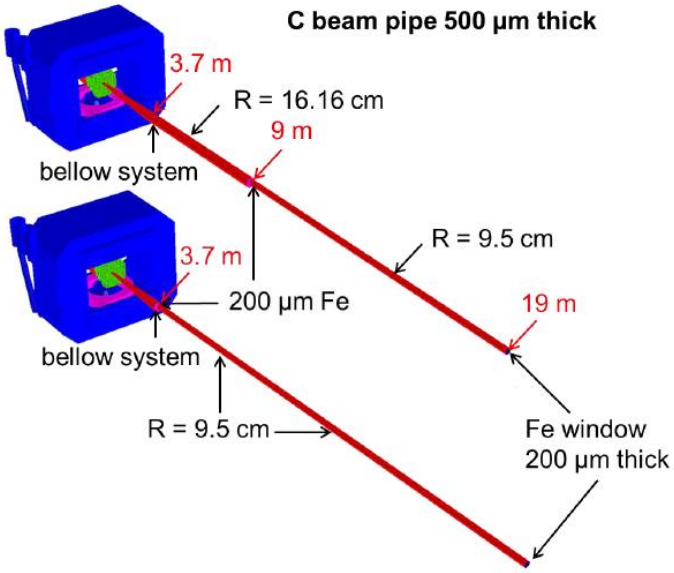

Figure 2.2: Two beam pipe example for the CBM.

2.2. SILICON TRACKING SYSTEM (STS)

The silicon Tracking System (STS) is one of the key detector systems of the CBM experiment that provides momentum and tracking information of charged particles that emerge from Au on Au nuclear collisions at 10 AGeV. In figure 2.3 the general view of the detector system is shown. It is designed for an average Au on Au nuclear collision rate of 10 MHz, creating an average track rate of 5 billion tracks per second. Design momentum resolution of dp/p ≈ 1.5% is achieved through a pitch of read out strips of 58μm, resulting in a 1 sigma single-hit resolution of about 25μm. In addition, the system is designed to minimize the material budget. It has eight planar stations that include ladders, sensors and front-end boards. The tracker provides an angle of acceptance between $2.5^0<\theta<25^0$ [24].

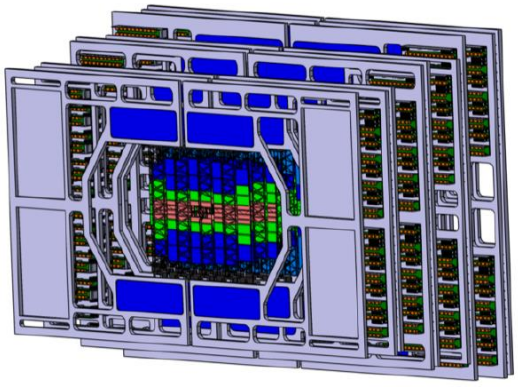

Figure 2.3: General view of the STS system.

The silicon tracking system is placed between a superconducting dipole magnet in a 1T magnetic field (Figure 2.4). For the sensors, different double sided silicon sensor sizes (2.2/4.2/6.2/12.4 cm long) and 6.2 cm wide with 1024 strips at each size are preferred. The smallest one is preferably allocated the inner part of the station close to the beam where the highest hit density is expected. In this inner part, hit rates of up to 250 kHz per strip are expected even for the shortest sensor. At the outer, lateral parts of the detector within the angle of acceptance the particle track rates decline down to a level of about1%. At the outer part of the station sensors of 12cm long strips are used to keep the number of read-out channels at the lowest level [25].

The STS components like front-end electronics, mecanical and cooling infrastructure are planned to placed outside of the acceptance in order to minimize the material budget. 106 detector ladders and a total of 896 modules will mounted in the STS system to form the tracking stations. The vacuum beam pipe that is made from 0.5 mm thick carbon fiber/composite will be installed on the beam upstream side to the downstream STS wall with connection through the MUCH or RICH detectors. In order to decrease the radiation effect near the beam axis that causes leakage current the sensors will be operated at -5 ^{0}C up to 500 V bias voltage [22]. Therefore, cooling part is one of the principal part during the experiment. Alongside the heating suppress of the front end electronics electronics heating supress, the sensor temperature that is

placed inner part of the system must be kept below or at -5^{0}C by using free gas flow with a power of 40 kW. The cooling for CBM expriment is based upon CO_2 evaporation. In order to keep the humidity away from atmosphere nitrogen should include in the closed cycle gas system [21].

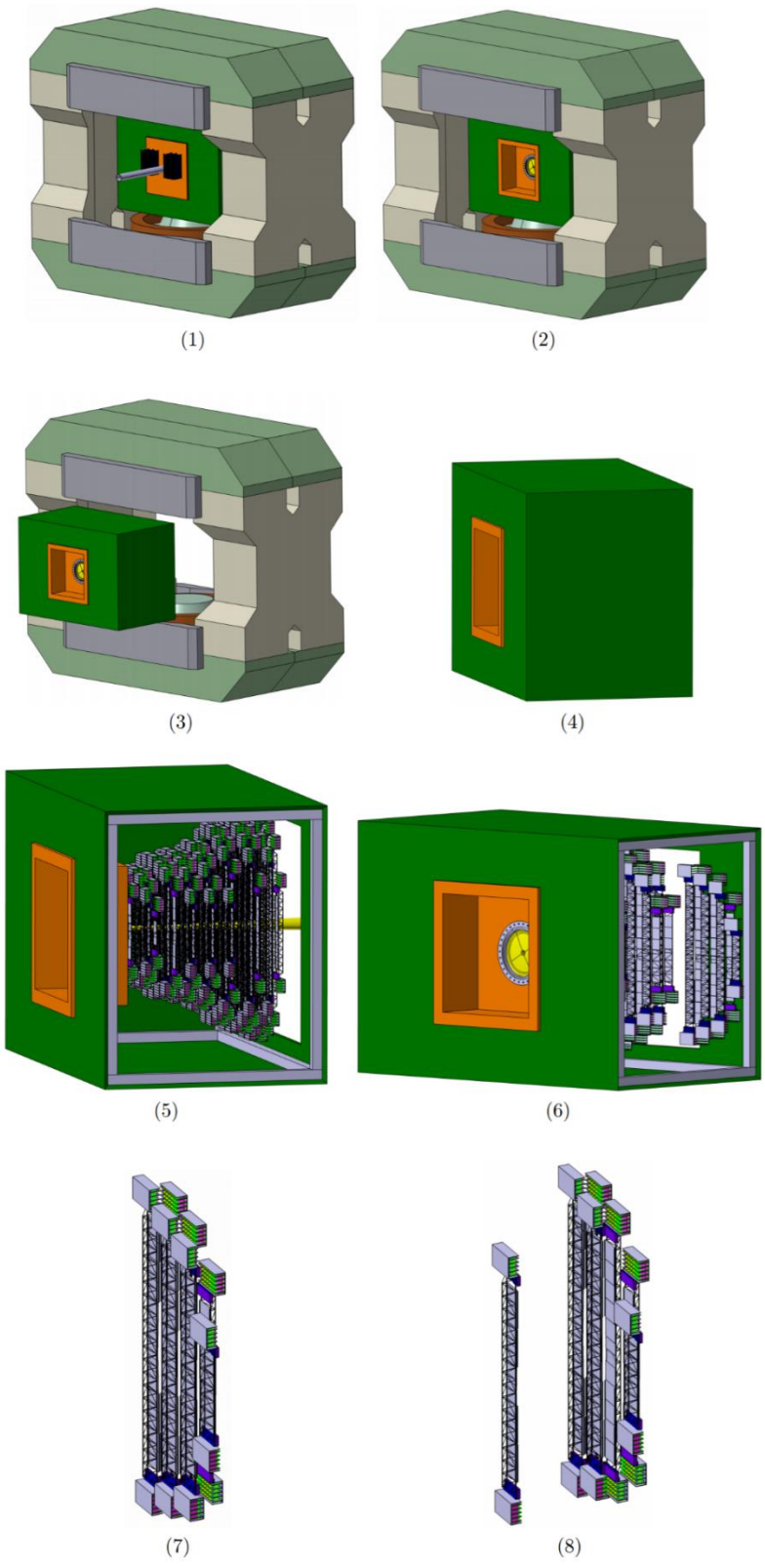

Figure 2.4: Inner part of the STS system.

2.2.1. Silicon Micro-Strip Detectors

In the Silicon Tracking System, double sided micro strip sensors are preferred thanks to their good momentum resolution and best performance in particle identification. The sensors are fabricated from n type wafers and have 300 µm thickness. In the STS module, four type sensors (width of 6.2 cm and 2.2 cm,4.2 cm,6.2 cm and 12.4 cm height) which have different heights but the same width are used. In order to cope with high hit rates and avoid ghost hits generated from simultanous double hits, n side strips have 0^0 angle and p side strips have 7.5^0 angle with the pitch of 58µm [25, 26].

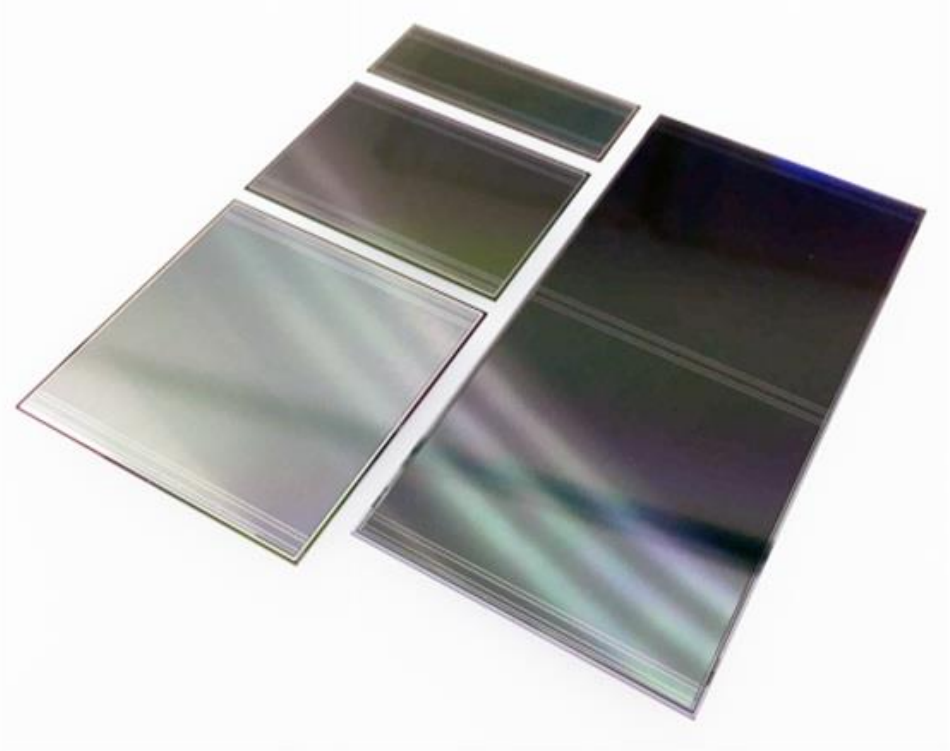

Figure 2.5: Silicon Strip Detectors [28].

The version label CBM06 is the latest and last serial sensor design for CBM since 2017. The sensors were ordered from the following sellers: CiS Forschungszentrum für Mikrosensorik GmbH, Germany [27], and Hamamatsu Photonics K.K., Japan [28].

With the aim to do a two coordinate spatial measurement, p and n strips compose a pixel grid at size $\Delta x = 58\mu m$ and $\Delta y = 58\ \mu m / \tan(7.5^0) = 440.6\ \mu m$. The bond pads for signal read-out were designed on this grid and arranged at the top and bottom edge of the sensor. A bias ring encloses the strips and provides several bias connection pads in the corners and along the edges. There are alignment marks and multiguard rings, and strip numbers on further side. The CiS and Hamamatsu sensors are illustrated in Figure 2.6 and 2.7.

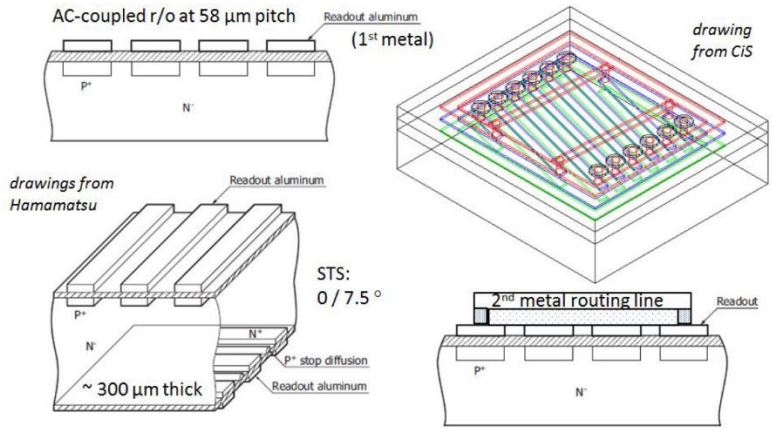

Figure 2.6: Three dimensional model drawings of CiS and Hamamatsu.

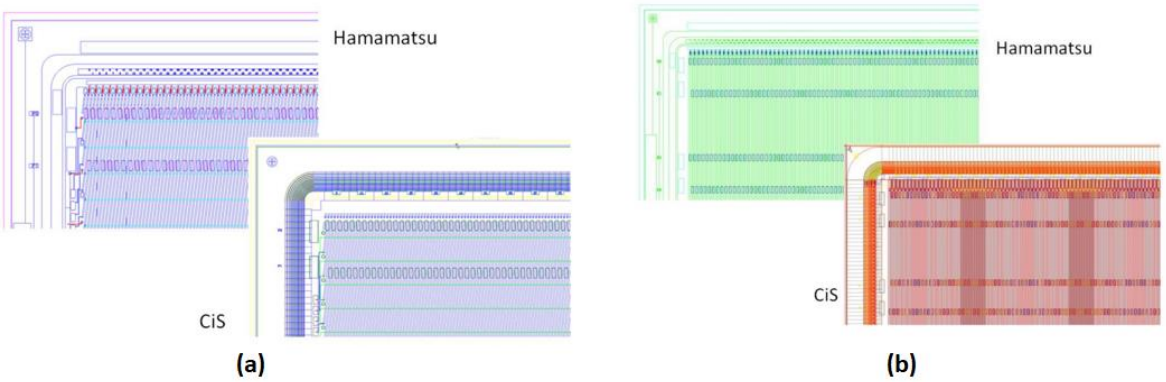

Figure 2.7: (a) Image of the sensor p-side for Hamamatsu (left) and CiS Sensor (right) (b) n-side for Hamamatsu and CiS Sensor.

Both CiS and Hamamatsu sensors were designed to be mutually compatible with module assembly. After some quality tests it was predicted that the CBM06 sensors can be produced with high legibility. For instance, the test results showed less than 0.3% single-strip defects for p and n side (for CiS sensor 6.2 by 12.4 cm data was taken from old prototype). They have high-quality interconnections at the second-metal routing lines. Also strip resistivity, capacitance and bias resistors correspond the essential features [29].

Table 1.1: The technical specifications of the sensors.

Electrical Characteristics	
Parameter	**Value**
at ambient temperature	25C
Full depletion voltage	40-150V
Breakdown voltage, measured on diced sensor	>210 V
Leakage current at bias ring at 200V or 2xfull depletion voltage, measured on diced sensor	1) 6.2x2.2cm: 1.5 µA 2) 6.2x4.2cm: 3 µA 3) 6.2x6.2cm: 4.5 µA 4) 6.2x12.4cm: 9 µA
Bad strips on each side	Maximum 15
Poly silicon bias resistors	5MΩ per strip
Strip coupling capacitance	> 10 pf/cm
Strip capacitance	<1.5 Pf/cm

General Specifications	
Parameter	**Value or Description**
Wafer type	n-type Si, resistivity 2-8kΩcm
thickness	285-320 µm ± 15 µm (optionally 400 µm)
Layout type	CBM06
Total outer dimensions	1- 6.2 cm x 2.2 cm 2- 6.2 cm x 4.2 cm 3- 6.2 cm x 6.2 cm 4- 6.2 cm x 12.4 cm
segmentation	Double-sided, p-strips, n-strips
Number of strips per side	1024-n side 1024-p side+ 42, 88, 134, 274 (for each of the variants 1-4)
Strip pitch	58 µm
n-strip isolation technology	p-spray/stop
Strip angle	0 degree on n-side 7.5 degree on p-side
Second metal routing lines	Between corner strips on p-side
AC bond pads	2x512 AC bond pads in two bond rows for each side; Pad size 60µm by 180µm: Additional spare bond row per side of the sensor; The Largest sensor (12cm) has also central bond rows.

	p-side and n-side pads arranged symmetry-identical
Bias ring	Around active sensor area with multiple bias pads
Bias structure	1 poly silicon resistor per strip, R as large as possible (5 MΩ); 1DC pad per strip for diagnostics
Bias pads size	400 µm by 150 µm
Guard rings	Multiple guard rings
Alignment marks	1 per corner, 3 per middle edge; 100 µm cross
Strip numbers	0-1023, marked close to bonding pads
Stretch marks	For serial numbering

2.2.1.1. Silicon Strip Detector Physics

A system with a tracking detector in magnetic field allows to detect the ionizing particles such as charged leptons and hadrons and to determine their momentums and charge type by measuring the track curvature [30]. As it is seen in figure 2.8, each particle has a unique track in detector system.

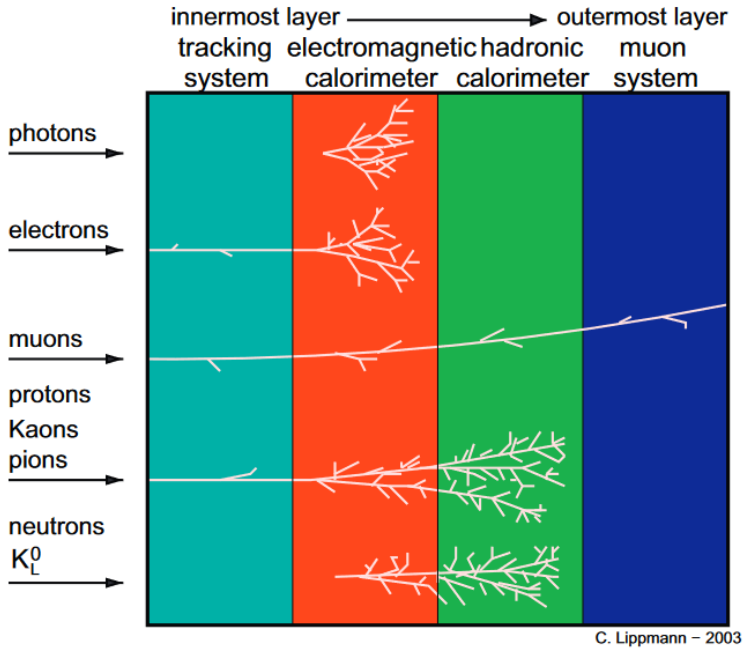

Figure 2.8: Components of a traditional particle physics experiment [31].

Silicon detectors are widely used in high energy physics since they provide a bandgap and depletion zone to create electron hole pair at about 3.6 eV. The difference of this energy to the band gap energy of silicon is disseminate as phonons. The relevant production of electron-hole pairs and phonons lead a decrease in the statistical variance of the created number of electron-

hole pairs. The decrement factor is called Fano factor and for silicon, It has been experimentally determined to be around 0.1 [32]. The sensor thickness that is used in particle tracker varies between 100 and 500 μm. The sensors have considerable advantages like good energy resolution, radiation hardness, fast timing response.

For particle detection some features must be provided as follows: in order to produce electron-hole pairs low values for the average energy is preferable to obtain less fluctuation in total number of electron-hole pairs, collection time of the charge carriers should be smaller than the carrier life time for the aim of completing the collection of free charges and in addition, leakage current that come to exist as a result of high electric field abut 1000V.cm^{-1} must be very small in order to measure the signal from the transient current [33].

In detector system, the leakage current is revealed by a reverse biased semiconductor and it causes noise. The leakage current of semiconductors can be given as below:

$$I_L \propto e^{-\frac{E_g}{2kT}} \qquad (2.1)$$

Where the Eg is the band gap of the material, k is the Boltzmann constant and T is temperature. Furthermore, higher leakage can occurs due to the number of traps in the crystal caused by hard radiation exposition [34].

Compared to gaseous detectors, Instead of tracking the charged particle through the silicon, individual mm sized strips are used for hit reconstruction in Silicon detector systems. It is preferable to have modules as small as possible in order to get a good spatial resolution. For a typical 300 μm thick module, nearly 5 μm spatial resolution is needed. It is also needed to increase the bias voltage to get a higher charge collection. Holes are collecten in about 25 ns while electrons are in about 10ns for a 300 μm thick silicon detector [35]**.** For 2-D imaging double sided silicon detectors is one of the attracted choice. In strip detectors, the second orthogonal set of strips is made on the backside of the detector and when two photons hit the detector at the same time, signals are prodeced in upper and bottom strips. Consequently, two real hits and two "ghost" hits are determined from the hit reconstruction (figure 2.9). In order to minimize the number of ghost hits either radiation intensity must be limited or a fast system need to be used [36].

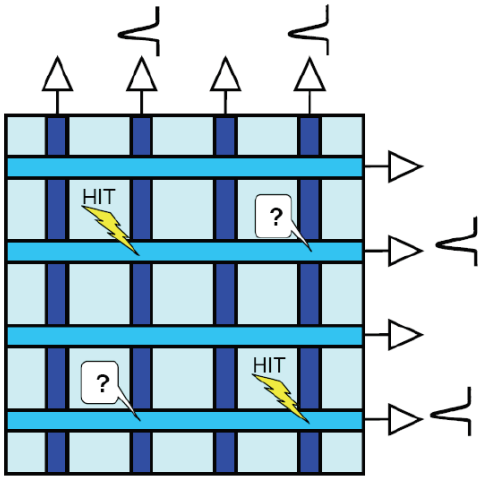

Figure 2.9: Ambiguity of position reconstruction in double sided silicon strip detectors [36].

Detector strips behave like electrodes to collect the charges and they are placed on a fully depleted silicon wafer as one-dimension diodes. Each strip connects to a charge sensitive amplifier. Measurements in two dimensional position can be achieved additionally structure the backside of the sensor with strips. The p-type and n-type doped strips can be arranged orthogonally collecting holes and electrons.

Silicon microstrip sensors include p-n junction and the working principle is basicly based on ionization. A depletion region is created by giving reverse bias voltage to the junctions in order to create a gap for charged particles. Part of their energy converted into electron-hole pairs. Electrons have negative charge and move to the positive electrode meanwhile holes move to the negative electrode. The electric field that is applied to the system prevents a recombining process of the electron and hole pairs [37]. However, the energy loss for minimum ionizing particle is foreseen as 26 keV in the sensor and the deposited charge by a minimum ionizing particle in a typical 300 μm thickness is 22500 electron-hole pairs or 3.6 Fc [38].

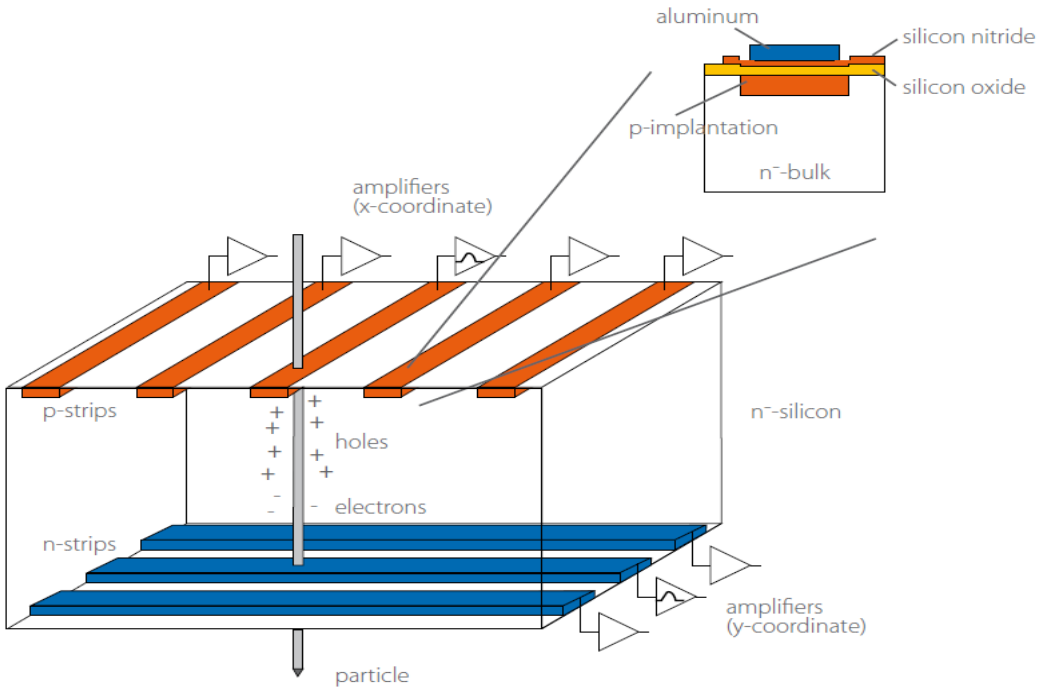

Figure 2.10: Operation principle of a double sided strip detector [39].

In silicon detector consept, for every strip of a silicon sensor a readout channel is provided by a direct connection from the strip to the amplifier input. This means that it is DC coupled and the amplifier must sink a fraction of the detector leakage current that corresponds to the strip. Notably, in irradiated strip detectors this contribution is much higher than the signal current. For the present silicon detectors the DC leakage current pass over a resistor and gather only the AC part over a capacitor by AC coupling. Because the leakage current depends on the applied

bias voltage and the radiation damage and it is difficult to build an amplifier that conduct such a high input current. Meanwhile, the bias voltage is usually decoupled with an RC filter.

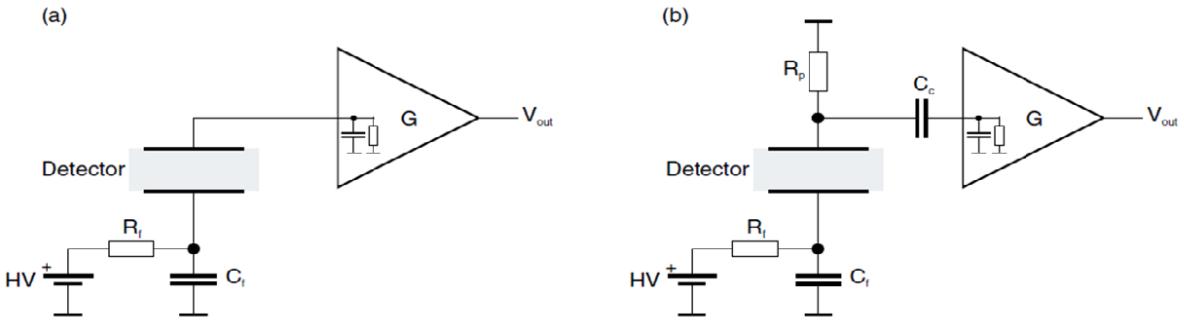

Figure 2.11: DC (a) and AC (b) coupling.

Since a huge number of channels are required in high energy physics experiments high integration should be provided instead of building a discrete amplifier. The front end chips include some functions such as analog bias generators, sample/hold circuits, the associated control logic and a multiplexing output stage that are built into an integrated circuit (IC). The amplifier has a low resistance current input since a semiconductor detector produces a current signal as well as the shape of the current pulse hinges upon the bias voltage. Therefore, it is benefical to measure the integrated current that equals to the collected charge. Thereby the first part of the amplifier is an integrator. Due to noise structure, a shaper in the second stage of the amplifier is used to decrease the noise and CR-RC shaping method as seen in figure 2.12, ensure a semi-Gaussian filter in order to provide easy application [40].

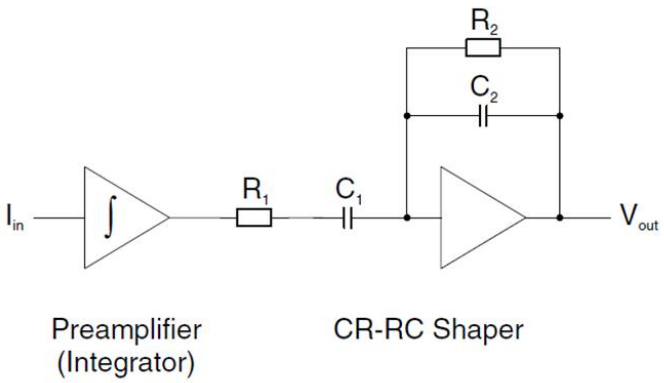

Figure 2.12: Preamplifier followed by a CR-RC shaper.

2.2.1.2. Energy Resolution

If Egap is the energy that is needed to create an electron-hole pair and the number of electron-hole pairs produced by a particle despositing energy E is;

$$N = \frac{E}{Egap} \tag{2.2}$$

As it is presumed that the number of electron-hole pairs excited in the detector gap is a Poission distribution, the fractional variance is;

$$\frac{\sigma_N}{N} = \frac{\sqrt{N}}{N} \tag{2.3}$$

The actual variance is affected by electronic and lattice excitations and this is explained by Fano factor F;

$$\frac{\sigma_N}{N} = \frac{\sqrt{FN}}{N} = \frac{\sqrt{F}}{\sqrt{N}} \tag{2.4}$$

Then the energy resolution can be found by substituting N from above:

$$\frac{\sigma_E}{E} = \frac{\sqrt{FEgap}}{\sqrt{E}} \tag{2.5}$$

Egap is 3.68 eV at room temperature. A 1 MeV charged particle can create about 272,000 electrons and it gives energy resolution about $\frac{\sigma E}{E} = 0.06\%$ [35].

2.2.1.3. Electrical Quality Measurements of The Sensors

Testing the sensor is one of the significant step since the performance of the sensor can be determined with some measurements before and after irradiation. For this purpose, electrical characterization was performed at GSI, Tübingen University and at JINR/Dubna.To determine the electrical characteristics, the leakage current should be measured as a function of reverse bias voltage and the bulk capacitance. In figure 2.13 one example measurement can be seen for those measurements. The leakage current depends on temperature and is normalised to 20 ^{0}C as seen in the plot. Therefore, in figure 2.14, It is also seen that irradiation does not affect the bulk capacitance while the leakage current steps up with a factor of 1000. These measurements result in a determination of the full depletion voltage and breakdown voltage of the sensors [41].

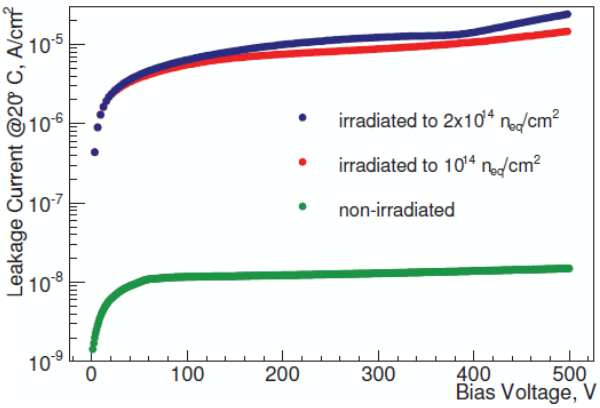

Figure 2.13: Leakage current as a function of the bias voltage for non-irradiated and for irradiated sensors. The leakage current goes up by order of magnitude through irradiation for the depicited it does not scale with fluence as two different individual sensors were characterized.

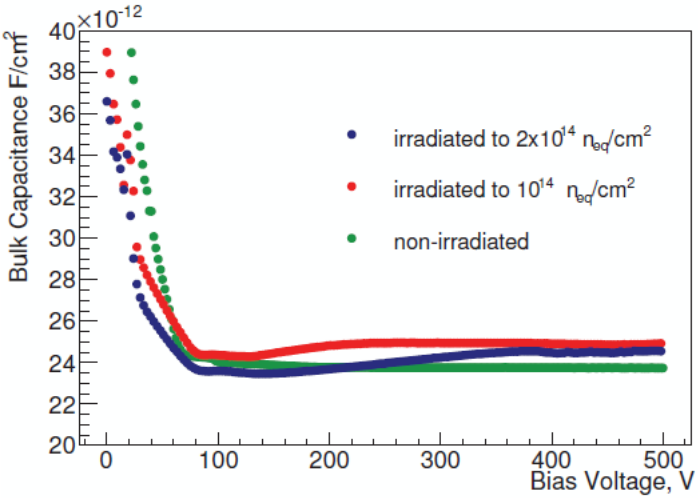

Figure 2.14: Bulk capacitance as a function of the bias voltage for non-irradiated and irradiated sensors. The bulk capacitance is not compromised through the irradiation as long as full depletion is achieved. Differences observable are attributed to different individual sensors.

2.2.2. Microcables

The microcable is the one of most important and key the element that provides connection between read-out electronics and sensors in the STS. A total of more than 32 thousands microcables with the length ranging between 100mm to 500mm will be used in STS module and ladder assembly. They are comprised of a batch of analog signal cables, shield layers and meshed spacers. The analog cables that include 64 signal lines are materialized with 14 μm thick aluminum using aluminium-polyimide adhesiveless dielectric [42].

The conductive layer is aluminum foil and the insulating material is a polyimide film. Kapton is also used for some layers to reduce the capacitance of the cables in the connecting layers. On the other hand, other layers consist liquid film which then solidify to the aluminum sheets. They

are radiation-resistant with a dielectric constant about 3.5 such a good electrical property. The polyimide has 10 μm and aluminum sheet has 14 μm thickness. In addition the metal trace has 30 μm width. External shielding is used in order to minimize the noise level and avoid shorting between the stacks of cables [21]**.**

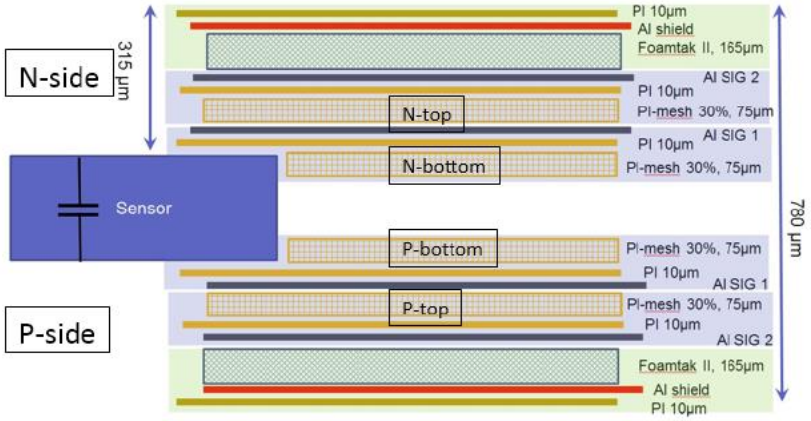

Figure 2.15: The layers of the microcable [43].

The microcables are manufactured by the company LTU to GSI and JINR for tests and assembly. During the assembly and test stages of the STS modules especially for the mCBM setup several development requirements evolved for the microcables. These can be listed as adding chip shielding cables, increasing the width about 15 µm to 155 µm of the opening in the polymide in the bonding area, decreasing the width of traces on analog microcables about 5 µm down to 30 µm in the work area, increasing the width of traces about 3 µm to 45 µm in the bonding area and increasing the length of the shielding layers as well as to allow to cover the sensor.

As a result of these requriments some modifications for 13 pcs cable sets is planning to be done notably in bonding areas. These microcables will be used for mSTS modules and 5-10 pcs cable sets will be produced in order to estimate the impact of raw material on the final yield at cable production by using raw material from different suppliers [44].

Figure 2.16: An example for the microcable with one ASIC.

2.2.3. Read-Out Electronics

2.2.3.1. STS-XYTER ASICv2

The STS/MUCH-XYTER [STS X and Y coordinate, Time and Energy Readout chip] chip is dedicated for signal detection from double sided silicon micro strip detector in the CBM environment (figure 2.17) The self triggering ASIC provides both timing and energy information for each incoming signal in its channels. The ASIC involves 128 read out channels and 2 test channels [21]. The STS/XYTER die size is 10mmx6.77mm includes 288 pads for wire-bonding as well as Pogo Probe landing [45]. The features of the STS/MUCH XYTER ASIC can be listed as follow: 0-12 fC dynamic range, maximum 10 mW per channel and radiation hard design. In addition to those features it is possible to use some tests such as pogo pin tests, built-in calibration [46]**.** The ASIC properties are given in detain in table 2.2.

Table 2.2: ASIC Architecture

STS XYTER	
128 charge processing and 2 channels	5-bit flash ADC
58 µm channel pitch	low power consumption (< 10mW/channel)
Operating with negative and positive polarity	low noise (ENC<1000e^- rms at C_{DET}=30pF)
Radition tolerant design up to 20 kGy	A calibration unit
300µm thickness	15 fC dynamic range
Time resolution < 5 ns	Hit rate/channel: 250 kHz average
Charge sensitive amplifier	Die size: 10mm x 6.77mm
Fast path: CR-RC shaper with tp = 30 ns, discriminator, time-stamp latch, pulse stretcher	Slow path: CR-(RC)2 shaper with switchable tp = 80 ns, 5-bit flash ADC, digital peak detector

ASICs are placed at the end of micro-cables that are connected between the detector strips and the preamplifier. It has 128 channels that comprise a charge sensitive amplifier (CSA), shapers and a flash ADC [21]. The charge Sensitive Amplifier (CSA) is used to obtain suitable gain settings and trimming for STS conditions [47]**.** It integrates the pulse to produce an output that is proportional to the charge into the amplifier input [48]**.** Their design provides stability and low noise as well as an output proportional to the total charge flowing from the detector during the pulse event. Thus, they are preferably used in radiation detection systems when individual detection pulses are needed to be measure with high sensitivity [49]**.** It has a big influence on power consumption, timing properties and measurement resolution. Furthermore, during charge processing, electrons and holes have different signal polarity. Holes have negative polarity while electrons have positive. In order to evaluate the available voltage and unify the polarity, signals from the electrons needs to be inverted before it is transferred to the shapers [50].
In order to obtain maximum hit rate, CSA consists a reset circuit that triggered by a pulse stretcher output signal and also a resistance R_F and a capacitance C_F. The pulse stretcher arranges width and length of the CSA feedback reset control signal and also it is triggered by the discriminator output signal [51].

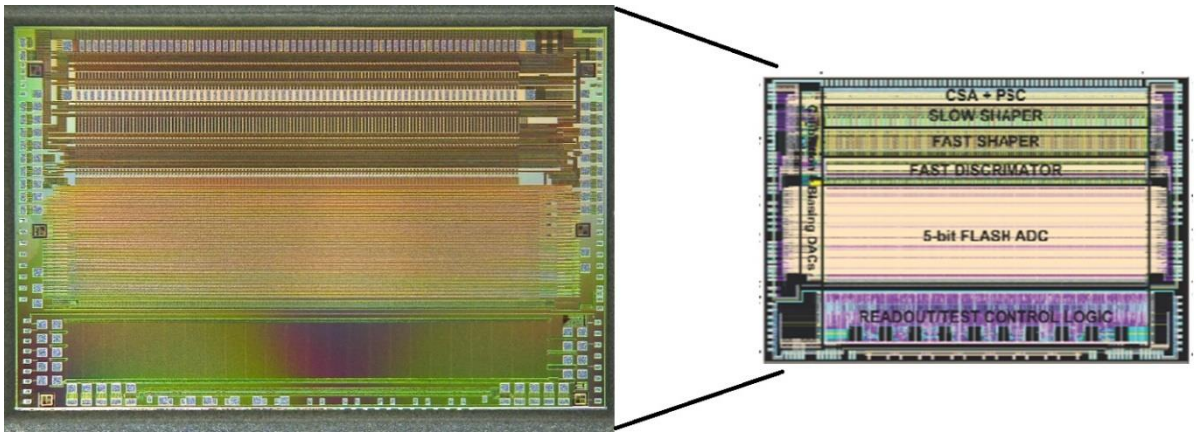

Figure 2.17: STS/MUCH XYTERv2.

The shaper includes a slow and a fast shaper. The fast shaper provides time measurement with 5ns resolution and 30ns peaking time while the slow shaper provides a better measurement of deposited charge signal by allowing a low noise measurement through a 5-bit flash ADC with peaking time as 80ns. All the channels of the read-out ASIC have the slow and fast shaper circuit during charge processing in order to gain a good amplitute resolution and in shapers CR–$(RC)^n$ shapers are preferred since they have less complicated feature for filtering of order n than other shapers as well as they can be characterized by lower silicon area occupation. However, in the CSA feed-back loop set circuits and the CSA and shapers output voltages return to the baseline potentials in a short time when the input pulses arrive [52].

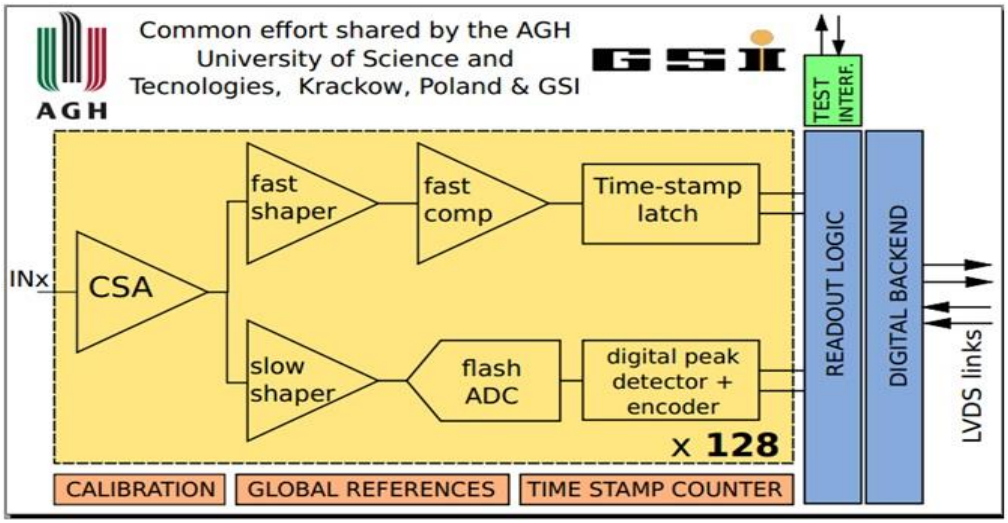

Figure 2.18: STS/MUCH XYTERv2 configuration diagram.

The 5-bit flash ADC in slow shaper comprises 31 discriminators and output of each discriminator is connected to a counter that is used to simplify the offset correction procedure (Figure 2.18) with inchannel 8-bit trimming of globally generated threshold voltages "*V*REF_P" and "*V*REF_N". They are two reference potentials that controlled by DACs and the common, global values are constituted with a resistor ladder stretched between those potentials. Therefore, another reference voltage "*V*REF_T" controls the effective threshold of the ADC and paves the way for calibration. The new Gray-encoded 14-bit timestamp value is stored in

the timestamp latch when the fast comparator fires. As soon as a signal from slow shaper passes through the ADC's first discriminator threshold frequently after a few ten ns, the block_ts signal blocks timestamp latching. In the following several hundreds of nanoseconds the pulse gets at its peak and returns to the baseline. Therefore, the peak detector withholds the maximum of the slow shaper's output as 5- bit. When signal drops below the lowest threshold discriminator, the data_valid flag becomes prominent and the hit data then is written into the 8-word deep channel FIFO, following, signals are synchronized with the back-end clock in the channel logic. As a last step, if the channel is not masked or the channel FIFO is not full, hit is written into the FIFO and the channel is reset when the process is completed so the channel will be ready for the next hit (figure 2.19) [53].

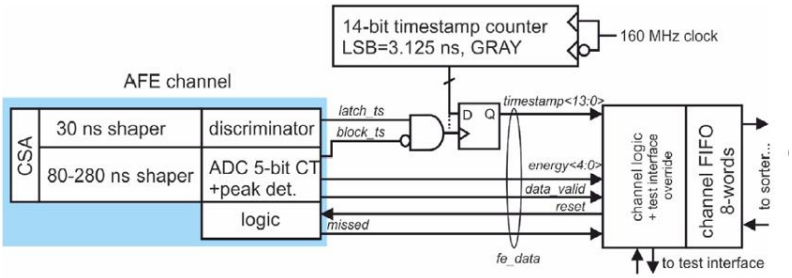

Figure 2.19: Hit generation mechanism.

2.2.3.2. Front End Boards (FEB8)

In terms of electronic boards two version of FEB8 (A and B version) is used in order to placed Asics for read out system (figure 2.20). All the ASICs in 896 modules at the STS system will be fitted with two front-end electronic boards and each one carries eight STS-XYTER ASICs for the read out of the silicon micro-strip sensors**.** They designed symmetric and each version represents p and n side due to the module placement to frame near the cooling part. Each FEB has 8 STS-XYXTER ASIC with 1024 channels.

Figure 2.20: FEB8 with version "A" and "B".

2.2.4. Ladders

After a complete module is assembled and tested, it is transferred to the ladder. A ladder is a Carbon Fiber (CF) space structure which is produced by the winding technique. To glue the sensors on the ladder, we need 4 L-shaped support structures called as “L-legs”. One part of the L-leg is glued to the CF ladder using Araldite- 2011 glue and the curing time for the glue is approximately 24 hours.

During the assembly procedure the assembled STS modules with sensors are placed on carbon fiber ladders so as to fix the module and the tools that called as “L-legs” are glued on ladders to hold the sensors. However, the sensors are glued one by one on the L-Legs in a position of 100 μm [54].

Figure 2.21: Ladder for STS modules.

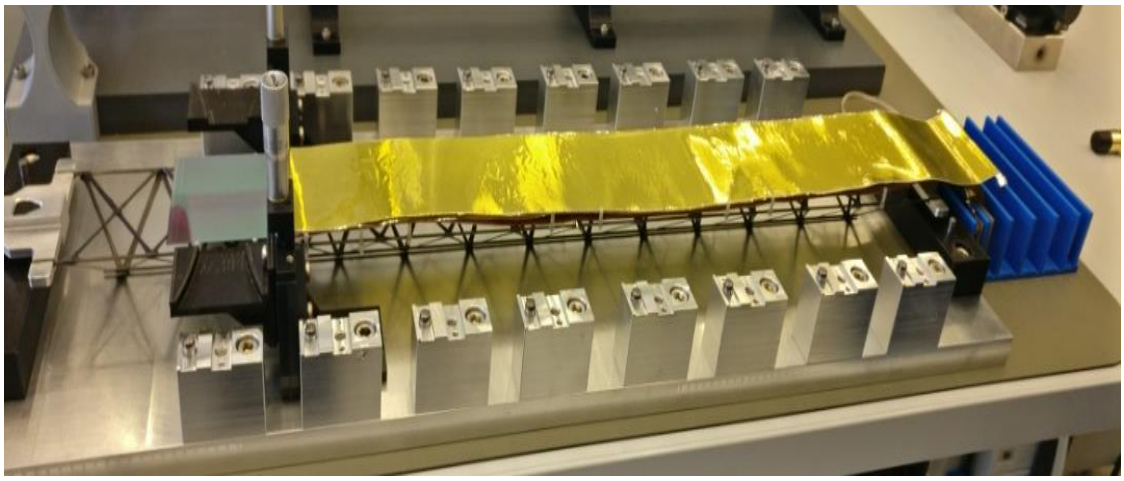

Figure 2.22: Ladder with a dummy module.

2.2.5. Prototype FEB8 and PCB Designs

The FEB has pitch adaptors that provide an electrical connection between detector and analog inputs of the ASIC. It has connectors to ASIC pads. This connection is done by wires which is made by wire bonding machines. On the other hand, detectors are accommodated on the printed circuit boards (PCBs) that can be connected to FEBs by ERNI connectors. So, with the help of those devices it is possible to do some tests in the laboratory without complex connections or real module. Furthermore, it is possible to do quality assurance for different detectors with a FEB connection by this prototype systems.

During the measurements, these systems are put into a metal box in order to provide a shielding to prevent the external electromagnetic effect and light.

Figure 2.23: Test prototype system for FEB-B and Sensor.

2.2.6. Read-Out System

Since the CBM experiment use high interaction rates, detector performances should be fast, as well as there should be strong constraints on the Data Acquisition (DAQ) system capacities. So, the CBM data acqusition (DAQ) will be based on the free-streaming system. This system includes self-triggered front-end electronics, fast free-streaming data transport, online event reconstruction and online event selection. In system, front-end electronic channels are self-triggered which means they digitize and time stamp any signal passing the thresholds. Also noise can increase on a single channel and this lead an overload on all parts of the readout chain

connected to it, thus safety features should be implemented. Also a high bandwidth network is necessary. In CBM network, datas are transmitted asynchronously. Each readout layer constantly pushes its available data to the next level. In order to be able to use a time based tracking and a time based event selection, it is necessary to place all data in a common time frame. This can be provided by time stamping them against a common clock [55].

The read-out chain for CBM experiment can be seen in figure 2.3. In order to collect data from FEBs and to implement an electrical to optical interface, a readout board (ROB) is used. The ROB uses the radiation hard GigaBitTransceiver (GBTX) ASIC and VersatileLink optical modules developed at CERN, because both data aggregation ASICs and optical modules are located close to te active area. It supports up to 6 clocks and downlink for control and up to 42 readout links on 3 GBTX devices. The frontend downlinks are connected to a single optical downlink to the frontend and 3 optical uplinks from frontend to DAQ. In addition, the optical readout connects to a FPGA based preprocessing and data formatting layer “common readout interface (CRI)”. It acts as interface to detector control and to the CBM first level event selector (FLES). This hardware will be installed on the surface of the experimental cave [56].

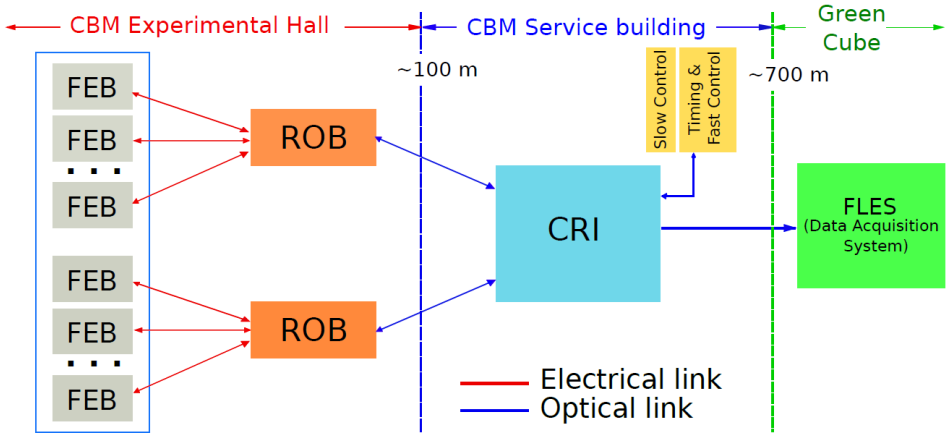

Figure 2.24: STS Readout chain.

3. MATERIAL AND METHOD

3.1. MCBM EXPERIMENT

Performing of the mcbm experiment is a basic first step before the final CBM experiment in order to test quality of the Front-End electronics and all detector systems. The data obtained from mCBM will generate a fundemental basis for the real experiment at SIS100. The detector set up for the experiment is placed downstream a solid target with an angle of 25^0 close to beam pipe. The system also designed to be versatile as required and for the best performance, a high performance free-streaming data acquisition system and first level event selector (mFLES) was used. The mCBM system includes 2 mSTS, 3 mMUCH and 4 mTRD detector in order to provide position information and this detector systems are placed an angle range between 13^0 to 37^0. In figure 3.1, the general concept of the system is given. Since mSTS is placed near bem pipe and is not possible to remove further, the overall acceptance is limited. Likewise the CBM system, a mini electromagnetic calorimeter (mECAL) and for the collision geometry 8 mPSD is placed. In addition to all systems, a T0 detector is needed during the test and calibration phase of time of flight and it is placed to the reference timing for the TOF based particle ID. This counter is equipped with an electronic grade polycrystalline diamond plate of 0.3mm thickness and is used for zero time determination. In addition, a single plate of 20mmx 20mm was placed in a beam-pipe vacuum upstream from the target [3].

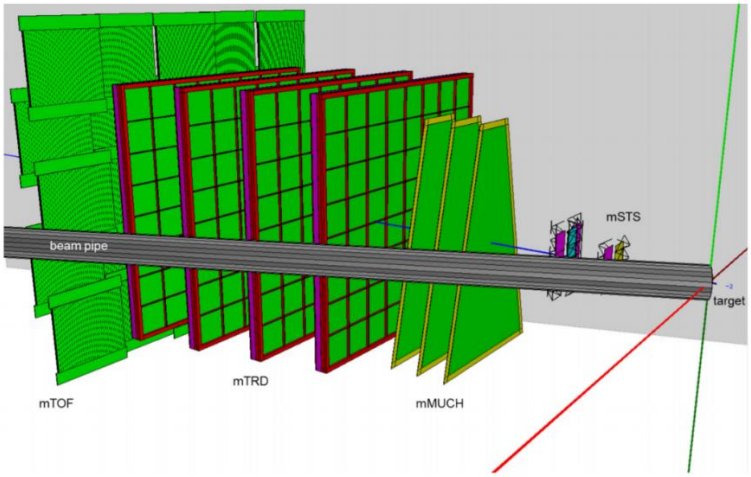

Figure 3.1: Placement of the mCBM detector system.

3.1.1. Mini STS System

The main idea for the mSTS is to build half station reference to the real one. The concept includes a half ladder about 50 cm and each ladder carries two or three modules as it is seen in figure 3.2. Two modules form the first station while other three detector modules create the second station. The module includes totally 13 double sided silicon microstrip sensors that has 1024 strip per side with the dimension of 6.2 cm to 6.2 cm. The sensors have totally 2048 read-out strips with more than 26 thousand channels with strip pitch of 58 microns and while n side has 0^0, p side has 7.5^0. 13 sensors in the modules connected with 26 Front End Board (FEB) for n and p side and FEBs include totally 208 STS/MUCH-XYTER Asics. The mSTS modules were tested inside a special design box. It has a shield against electromagnetic field and light.

Sensors are operated in a special temperature by using a water cooling system inside the box [3].

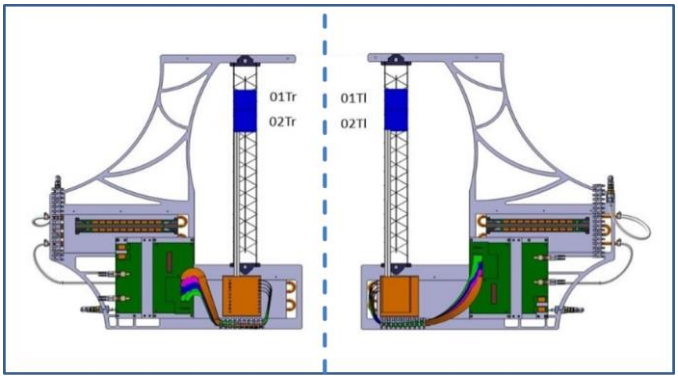

Figure 3.2: mini silicon tracking system.

3.1.2.Detector Modules For Mini STS

mCBM experiment set up consists of 4 mSTS modules named 01Tr, 01Tl, 02Tr and 02Tl respectively for both right and left side of the two ladders. In the modules both Hamamatsu and CiS sensors were used with 50 and 45 cm length signal transmission microcables and STS XYTERv2 ASICs (Figure 3.3). In module assembly, the microcables from LTU/ Kharkov based on 14 mm thick Aluminum, covered with a 10 µm thick insulating Polyimide layer are used. Each cable has 64 Aluminum traces with a width of 30 µm and a pitch of 112 µm. Therefore eight different cable types are needed for one side of the detector and altogether 32 microcables are necessary in a complete module [57].

It is decided to shield the four modules starting from FEB along to sensor in order to decrease the noise structure as seen in the figure 3.4, as well as the placement of the modules to C-frame.

Figure 3.3: One of the mSTS detector module.

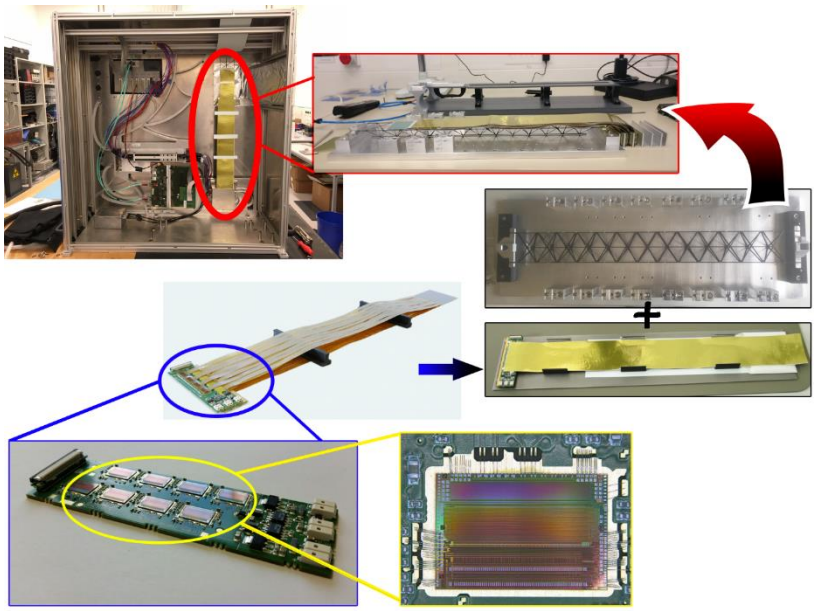

Figure 3.4: mSTS detector module parts.

3.2. STRUCTURE OF THE FRONT-END ELECTRONICS

The front-end electronis are used to shape and finalize the current pulse coming from the silicon detector. The pulse is first integrated in charge sensitive amplifier and a voltage step with amplitude proportional to the total charge generated in the detector is obtained at the output of amplifier. As a second stage the voltage step is processed in shapers with an analog-to-digital converter (ADC) which measure the amplitute of the signal corresponding to each individual photon. Herewith, determination of the time of pulse occurrence is the third stage.

In readout systems, the number of front-end channels is generally correspond to the number of strips in the semiconductor silicon detectors. In order to build larger modules consisting of a few thousands readout channels multichannel integrated circuits are preferably designed as 32,64 or 128 channels integrated circuits in readout electronics [36]. An example for the frond-End Electronics in detector read-out system is represented in figure 3.5.

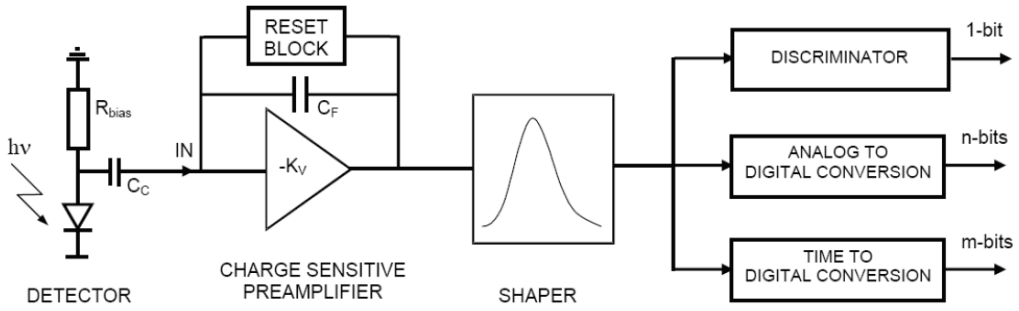

Figure 3.5: An example for the frond-End electronics In detector read-out system.

3.3. FRONT-END BOARD AND COMPUTING SYSTEM

The FEB-B is a prototype test front end board electronic that allows to check the ASIC performance and to couple it to different detectors. It has been designed to carry eight bonded STS/MUCH-XYTER v2 with 128 input channels. On the front end side it has a double ERNI connector for interfacing to the silicon sensors, therefore on the backend side it has a KEL40 connector as E-LINK interface of a single chip. The backend interface implements LVDS signals with 1 clock, 1 downlink for control and configuration and up to 5 up-links for data readout and control responses. After powering on the ASIC, the synchroneous exchange of fixed-length control and data frames between the ASIC and its FGPA backend is establieshed. By accessing a set of multiple chip registers, the analog front end and the digital part of the chip are configured with the correct settings for operation. Among these registers the control of the reference potentials for the ADC and the FAST discriminator as well as the correct polarity selection and the CSA bias current are included [58]. The system design is given in detail in figure 3.6.

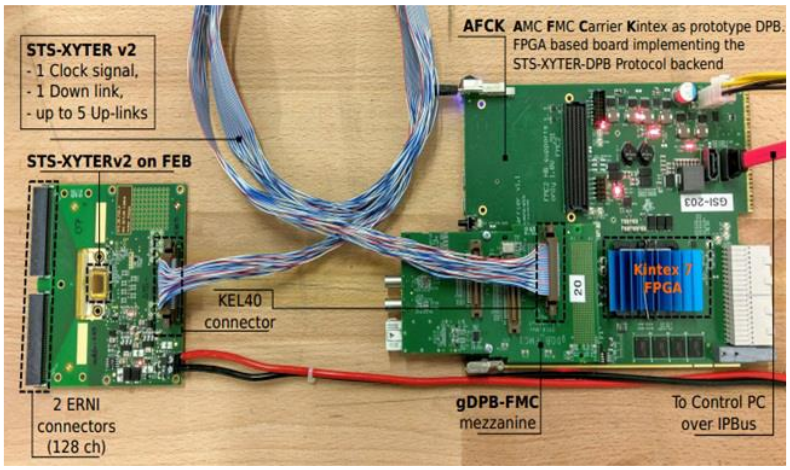

Figure 3.6: Front-end board and computing system.

3.4. POGO-PIN STATION

The pogo-pin is a test station where basic functionalities are checked at the ASIC level and was designed by collaboration with WinWay technology, Taiwan and Aps Solutions GmbH, Munich [59]. It consists of a test socket where you can placed the ASIC by use of vacuum tweezers. The ASIC is powered on and tested through a set of spring-loaded needles which access the ASIC's pogo pads slightly larger contacting pads of size 150 µm x 150 µm. 53 pogo pins are precisely allocated in a precision-made socket. The pogo-pins have a diameter of merely 100 µm. The old version of pogo station that is in figure 3.7 was the first tool for ASIC quality measurements and after a while its needles were broken since it was screwed by hand for each measurement. It is predicted that since one can not adjust the screwing it is possible to damage the needles. New version of the station (Figure 3.9) was designed against that problem has an applicative usage since it has a vacuum structure during placement of ASIC [58]. With new station, needles are easily connected to the ASIC pads thanks to its functional knob.

Figure 3.7: old version of pogo-pin test station

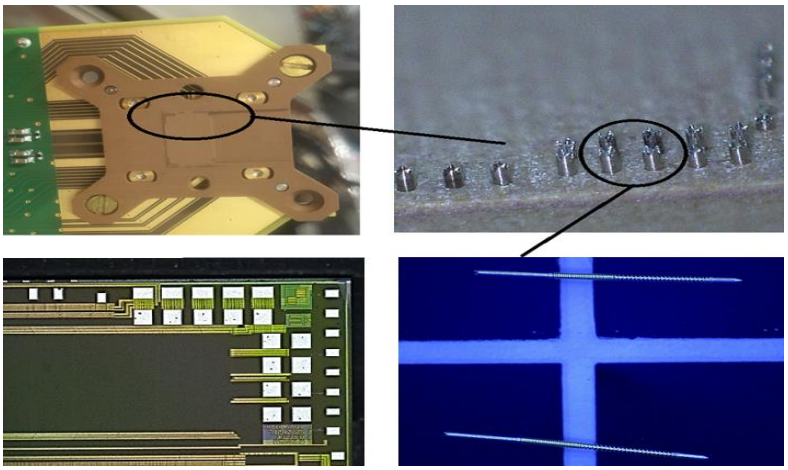

Figure 3.8: Close-up view of the pogo-pins arranged the pogo-pin assembly. One pin has a diameter of 100_m (right below). Corresponding (mirrored) contact area on the STS-XYTER ASIC (left below). Little marks on the square pads indicate that the pogo-pins did indeed have contact.

Figure 3.9: new version of pogo-pin test station.

Before the real experiment, it is benefical to configure the readout chip in order to find a proper measurement characteristics for silicon strip detector. Initially, all the measurements were done manually but for the future all the parameters will be fixed in CBM database.

3.5. MEASUREMENTS

In Silicon detector system, the integrated circuit should be multichannel because of the high density of the read out electronics. The integrated circuit need to be able to timestamp each of the registered events with a time resolution of ~5ns and measure the deposited charges up to 15 fC. On the other hand, the read out electronics should measure both electrons and holes as the input charges. Thus, a self-triggered read out ASIC called "STS-XYTER" was designed at AGH Cracow for all the requimements mentioned below [60]:

For a solid state detectors read out, the pulse processing and digitization can be done in several ways as below:

1- Binary processing: In this process the voltage pulse from CSA is compared in a discriminator with a treshold and when the pulse height exceed this treshold then the pulse can be detectable. But it is not possible to have an exact idea about the amplitute for each pulse.

2- Measurement using ADC: ADC measurement is play a significant role when the pulse amplitute measurement is required. An ADC is implemented for several channels together with analog multiplexer.

3- In the STS-XYTER there is a 5bit-ADC for each channel (there is no multiplexing)

3.5.1. Test Methodology in Treshold Discriminator Systems

In many systems the primary function is to detect just the presence of a pulse. For such a system a threshold sense circuitry is needed. This is called basic treshold measurement and the working principle is based on whether pulses exceed a threshold or not.

During the measurements noise is the most important effect that compromises both resolution of amplitude and the determines the minimum detectable signal threshold. As it is seen in the figure 3.10, when there is no pulse from the detector, the noise will be superimposed on the baseline. That is because, noise pulses have gaussian amplitude distribution and some of them will cross the threshold despite threshold setting. But, the noise rate changes with treshold.

It is possible to decrease the noise hit rate by increasing the threshold, though it cannot be set higher than 1% of the signal pulses are lost. This is illustrated in Figure 3.11 for a Landau distribution for minimum ionizing particles [61].

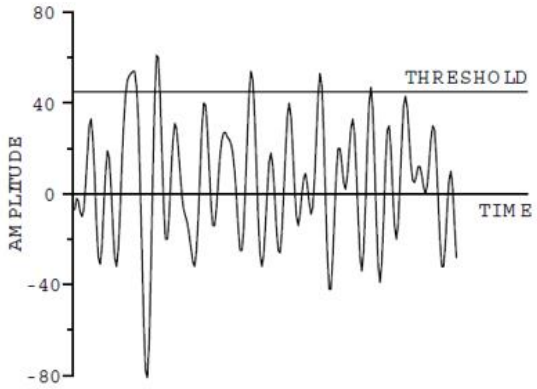

Figure 3.10: Noise pulses dependent on treshold settings.

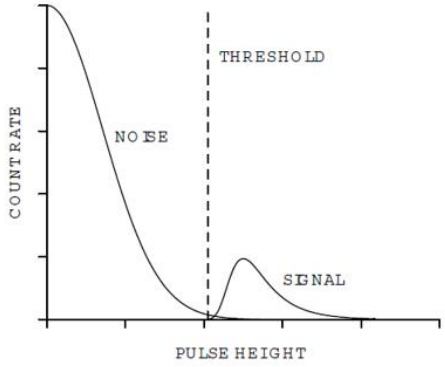

Figure 3.11: Comparison of the noise and signal rate. The treshold setting reject signal pulses but a small amount of noise pulses exceeds the treshold.

The signal-to-noise ratio is one of the most critical problems althouhg the front-end channels are ended with discriminator in the binary readout architecture. In figure 3.12, a typical plot of counts at the discriminator output are given as a function of threshold voltage. As it is seen in the figure a sharp increase of counts is observed for low threshold values especially below 30 mV and this is stem from the noise that contributes to the total number of counts [60].

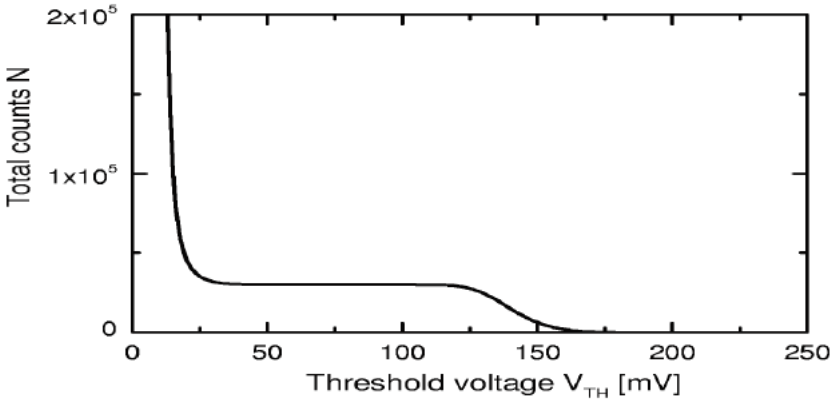

Figure 3.12: Total number of counts at the discriminator depending on threshold level.

When charge sensitive amplifier is used in a detection system, the equivelent noise charge (ENC) is generally used to characterize the noise. Treshold scan is a method to extract the CSA parameters in binary systems to be able to obtain the CSA voltage gain and the ENC. Tests are done by ejecting test pulses with known amplitutes for several discriminator tresholds and then the s-curves can be obtain by recording the registered pulses in the circuit (Figure 3.13).

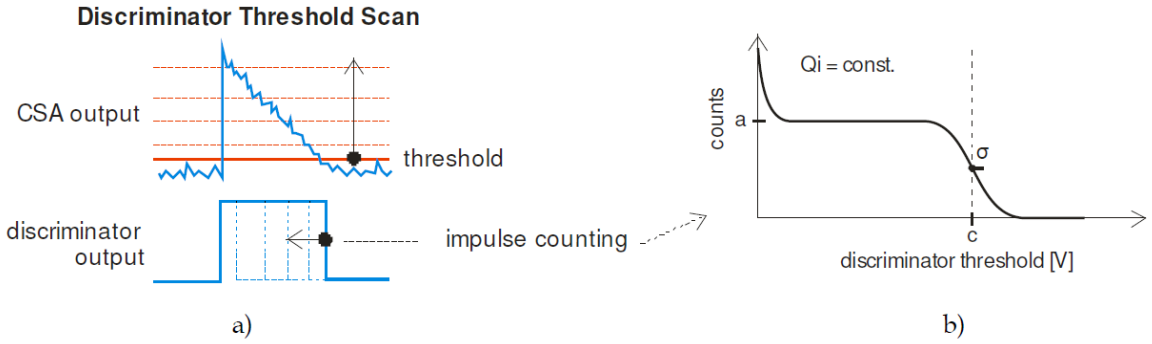

Figure 3.13: (a) Gain of pulses for different thresholds (b) s-curve from threshold scan

The s-curves shows sharp feature (a "step response") when there is no noise in the system. In the contrary when noise is added to the signal then the s-curves becomes slighter. Therefore, pulse amplitute and rms noise can be determined by fitting the modified error function to the s-curve since the noise has a gaussian distribution.

$$y = \frac{a}{2} \times \left(1 - \mathrm{erf}\left(\frac{x-c}{\sqrt{2}\times\sigma}\right)\right) \qquad (3.1)$$

a – nominal number of injected pulses per acquisition, c – scurve transition midpoint corresponding to the pulse amplitude and σ is rms noise voltage.
Taking the s-curve transition midpoints and plotting them versus the input charges provides to determine the voltage-gain characteristic of the CSA (figure 3.8). Then the ENC value can be calculated with the equation [60].

$$ENC_v = \frac{\sigma_v}{A_v} \qquad (3.2)$$

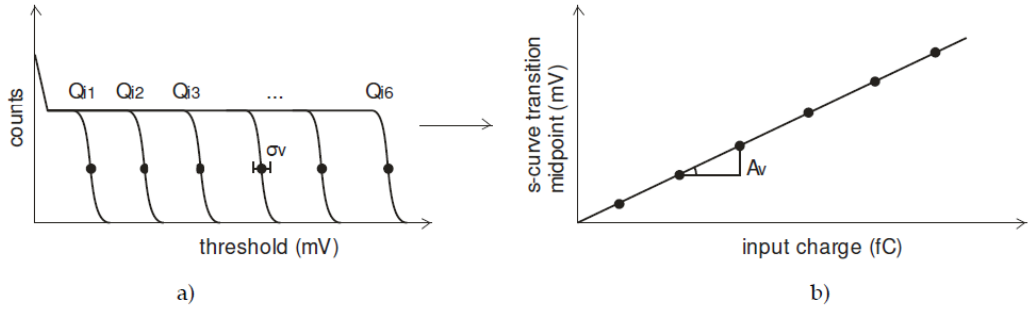

Figure 3.14: (a) several s-curves (b) gain characteristic

3.5.1.1. Internal Pulse Calibration

In order to calibrate the ADC and discriminators as well as to test the analog response of the ASIC, internal pulse calibration is used by generating pulses of several programmable amplitutes. Internal pulse generator is controlled via a DAC register in the backend. The calibration of the internal pulse generator (note: you have to distinguish between (1) the calibration of the pulse generator and then (2) the ADC calibration using the internal pulser) can be done with a connection to a FEB-B via a dedicated PAD routed to a LEMO connector. A Peak Tech 2155 LCR meter is connected at the end of LEMO connector so after different register values are set in the DAC as following the voltages on amp-cal monitor is recorded. Those voltage values specify the pulse amplitutes. In figure 3.15, the expected calibration (1) linearity (red line) and the measured register values can be seen. The slope was calculated about 0.5 mV/register value. It was found that 1 amp cal unit is equivalent to 0.056 fC or 347 electrons [58].

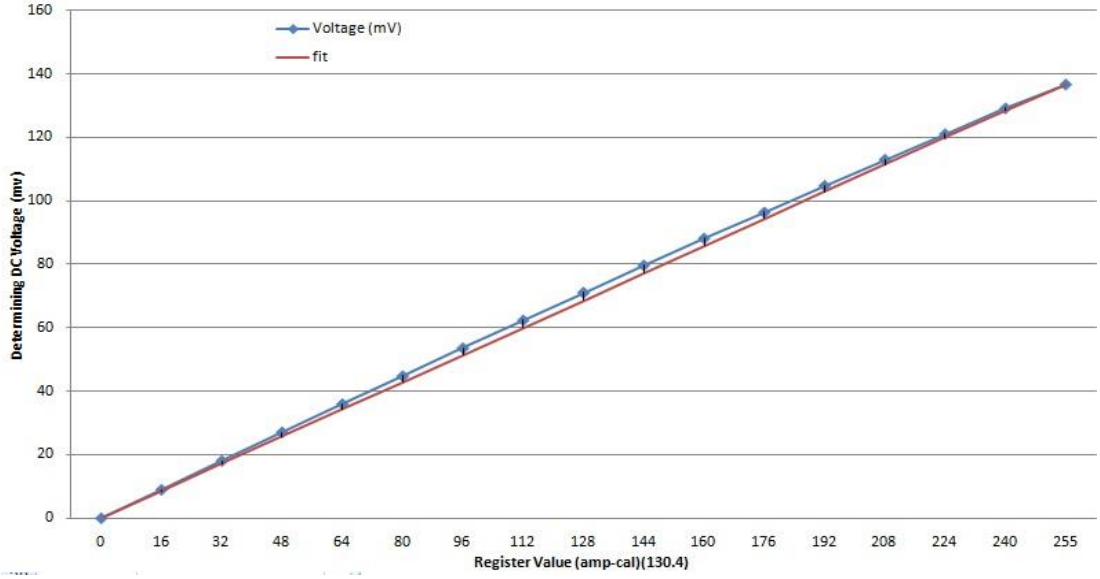

Figure 3.15: Internal pulse calibration

Furthermore, the 59.5 keV line from an ^{241}Am gamma source was used to validate the calibration (2). Preferably, ADC channels were calibrated with a gain of 0.11 fC/ADC amp-cal, a reduced dynamic range of approximately (3.42 ± 0.03) fC and an average offset of (1.52 ± 0.02) fC and in addition silicon sensor with a dimension of 4.2 × 6.2 cm^2 connected to FEBB was used. The n-side of the sensor with 128 strips (128 strips of the sensor connected to the ASIC for readout, the sensor itself has of course 1024 strips) was biased at 150 V for fully depletion. As it is seen in figure 3.16 the 59.5 keV peak position was determined by a Gaussian fit, yielding an ADC value of 10.2 amp cal and the deposited energy can be estimated as (2.55 ± 0.12) fC due to the calibration, in coincidence with the expected value of 2.64 fC. This difference about 2% may be explained with charge sharing between sensor and electronics, a failure charge collection in the sensor as well as charge sharing among strips [62].

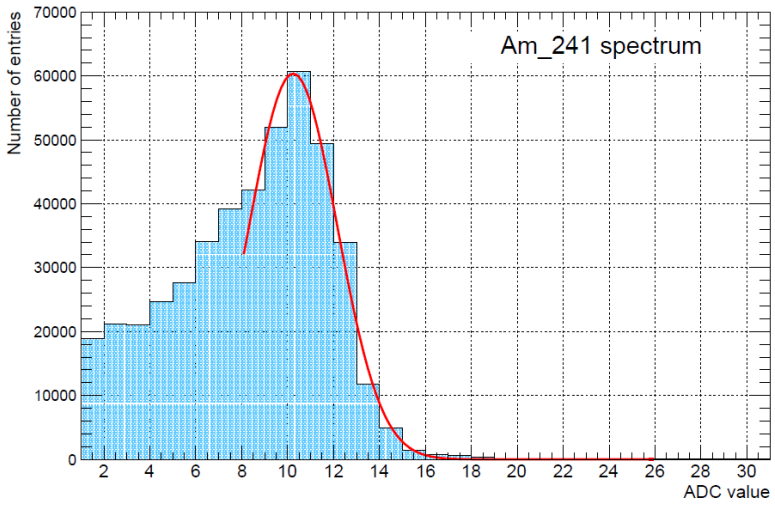

Figure 3.16: ^{241}Am spectrum in a channel of the STS-XYTER v2 that measured with a silicon strip sensor.

3.5.1.2. STS-XYTERv2 ASIC Test

STS/MUCH XYTER test is the first step in the module assembly and it is important to check their quality before bonding them on Front End Boards. In order to carry out this process, dedicated quality assurance (QA) tests were done for 339 individual ASICs with the old and new pogo-station set up mentioned before. A block diagram in figure 3.17 showing the test procedure with pogo-station. In the meantime, during the measurements it is not posible to determine the ASIC number otomatically so they were numbered according to rows and columns in the ASIC storage box as shown in the figure 3.18. The process begins automatically after placing the ASIC into the pogo-pin test socket and last approximatively 5 min per ASIC. In the QA process, tests were done for every specific ASIC. Current values before synchronization and after configuration, reference voltages values, analog response that means the ability of getting a response after applying a pulse to the ASIC and the dynamic range of the ADC for the electron configuration as well as for the hole configuration can be determined from scurves and also the generated hit information were obtained for one specifically chosen channel number “64” one out of 128 channels. As a result, the output of the process is written into a data file that can be accessed later on for all the ASIC.It is expected that after all this measurements the broken channel numbers will be less then %1.

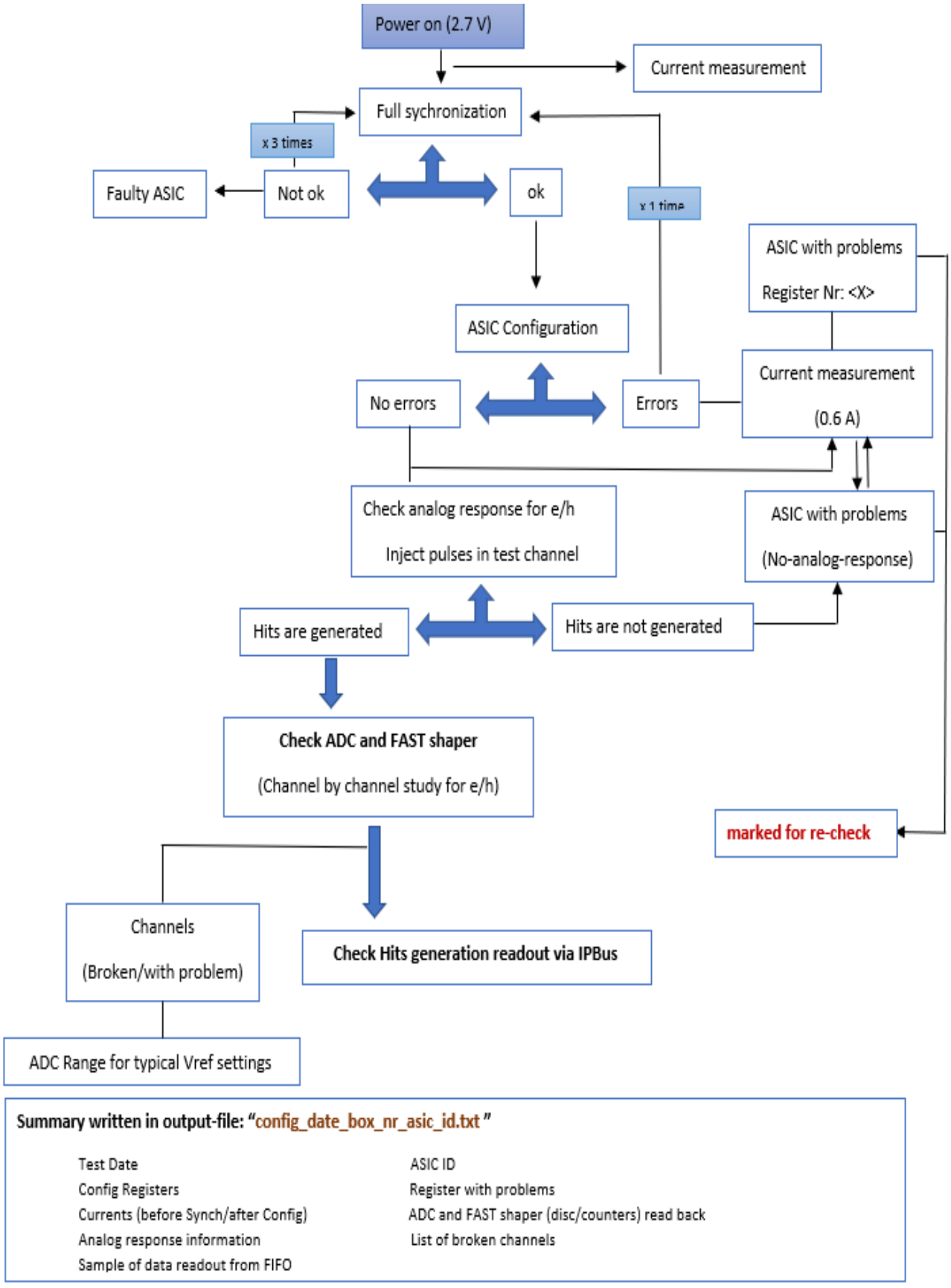

Figure 3.17: ASIC test procedure diagram.

Figure 3.18: STS-MUCH/XYTER ASICs and the numbers given.

3.5.1.3. ASIC Calibration

In STS XYTER all channels includes a 5-bit flash ADC and one discriminator for the fast path. It is possible to arrange the dynamic range of ADC by changing the reference potentials "VRef P" and "VRef N" of the resistors step that equally designed resistors and determines the comparator's threshold. In order to correct the fast discriminator of every channel and to find the appropriate trim values for every channel's discriminator, a scan in which a parameter is varied according to a defined range and step is implemented over the full trim range. The process is basicly depends on an application of a calibrated internal pulse generator and the response of the S-curves that is a 128 × 32 elements matrix with a format of text file. This file includes the configuration values for every channel. In figures 3.19 and 3.20, an example for a ADC linearity before and after calibration also the uniformity of the fast discriminator threshold can be seen. The ASIC ADCs were calibrated with a dynamic range of 12.2 fC corresponds to 20-240 amp cal units [62].

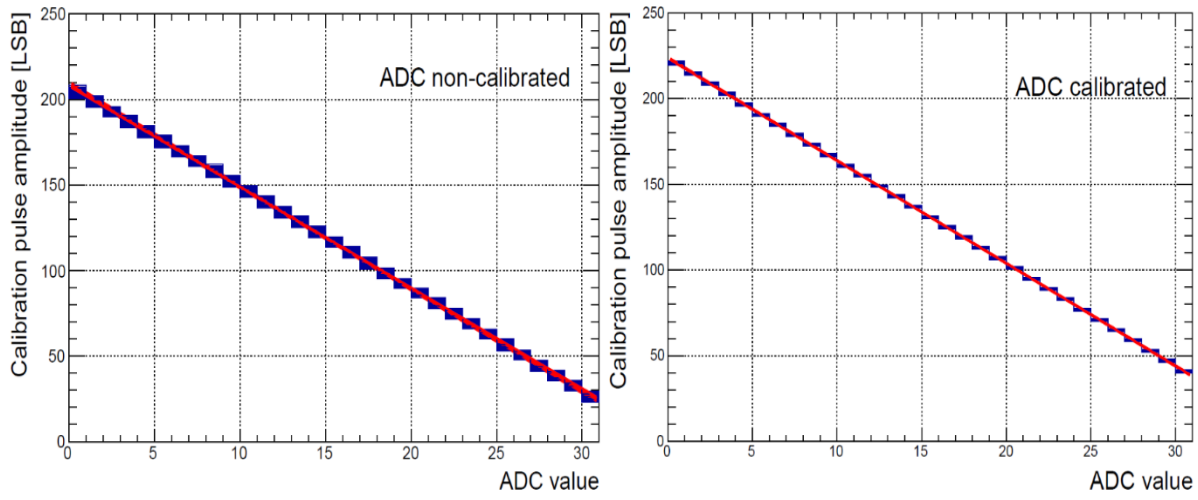

Figure 3.19: ADC values before and after calibration.

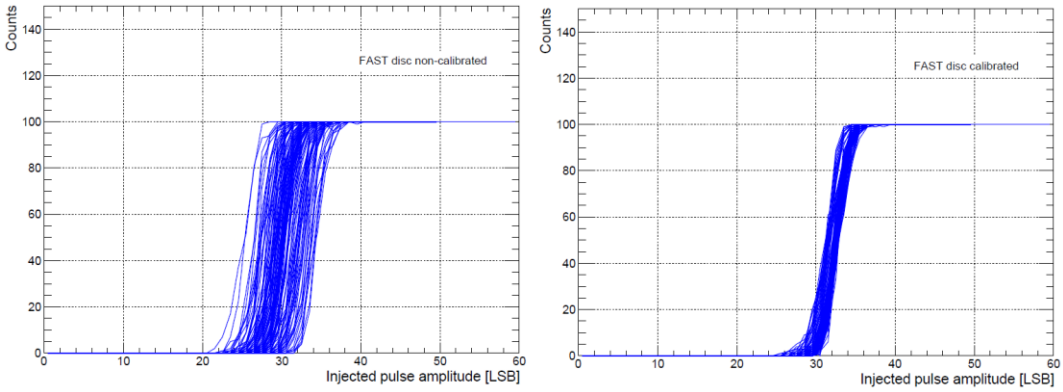

Figure 3.20: "S-Curves" before and after calibration.

3.6.....MCBM EXPERİMENTAL SET-UP ASSEMBLY AND MEASUREMENTS

3.6.1. Assembly of The Detector Modules

The assembly process for the modules is done at cleanroom laboratory at GSI. This process consists of four main steps [57]:

- In the first step, TAB-bonding of the microcables to the 16 STS-XYTER ASICs is done with a F&K Delvotec G5 Wedge Bonder. The STS-XYTER is placed to surface on the device and the bottom layer of the microcable and ASIC are fixed by vacuum on a special fixture. Then the microcable is carefully aligned and an adjustment is done with the help of µm-screws under the microscope. The fixture is then placed on the adapter plate of the bonder, and TAB- bonding process of the 64 channels starts for the first layer if the first bond fits well. The bottom layers are then fixed to the ASICs with a glue line. After curing, another layer of the microcable is bonded to second pad row of the ASIC. After bonding, the microcables are placed on the support plates for P- and N-side, sorted by short and long cables and the bonding rows are protected with glue. During this step a connectivity test between microcable and STS-XYTER ASIC is done.

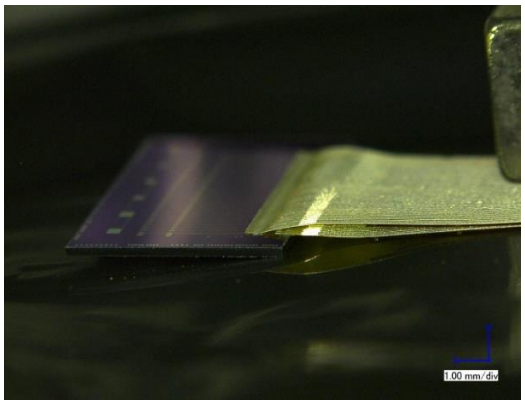

Figure 3.21: TAB-Bonding of the microcables to the STS-XYTER ASICs.

- Second step is to bond the other side of the cable to the sensor for p and n side. Bottom layer of the microcable and the sensor are fixed by vacuum alignment is done with micropositioners and the first layer is bonded to p side of the sensor. Microcable is fixed with a little glue to the edge of the sensor and top layer is bonded to the second pad row of the sensor. As a last step TAB-bonds are glued in order to protect the bonding. Again during this step a connectivity test between microcable, STS-XYTER ASIC and sensor is done.

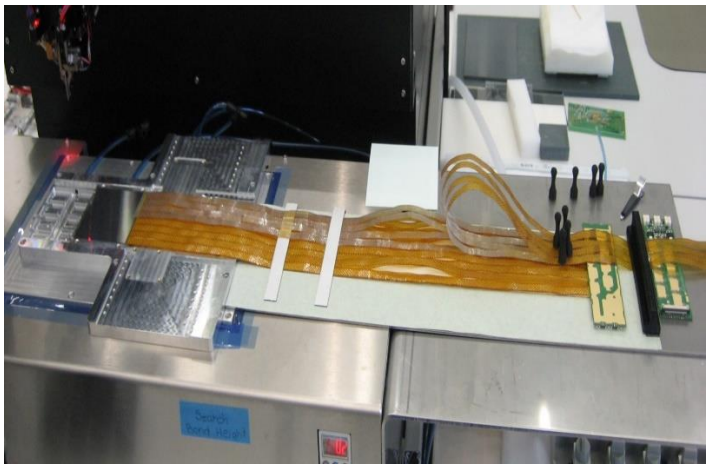

Figure 3.22: Bonding procedure of microcable with ASICs on the sensor.

- Third step is die and wire bonding of the ASICs to the first four row of FEB. Before bonding the FEBs are cleaned in an ultrasonic bath with a dedicated cleaner. After bonding and testing of the ASICs they are protected with Globtop. Then a shielding is done above the signal area of the ASIC by soldering. As a following step, the ASICs with long microcables are wirebonded to the back row of the FEB for P-side. At this moment, the FEB is tested and if everything is good the second row is protected with Globtop. Then the second and third procedures are done for the N-side.

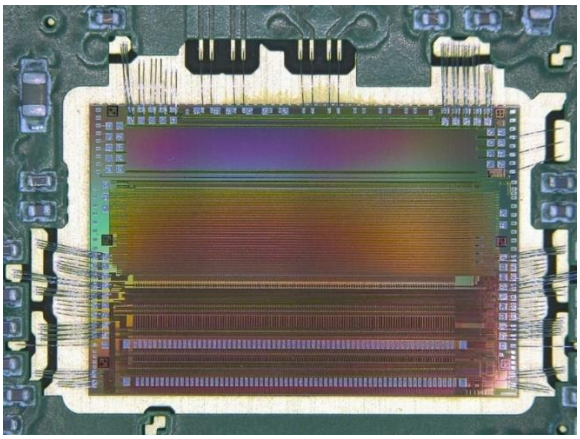

Figure 3.23: A wire-bonded ASIC.

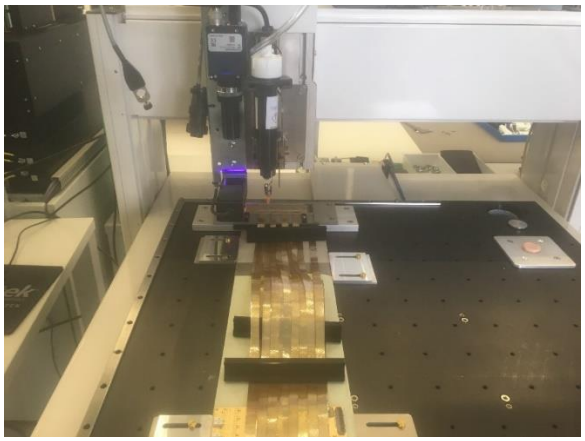

Figure 3.24: Glop-top procedure.

- After having tested the FEB8s, the shieldings are fixed on top of the module on P- and N-side. Shielding is fixed by glue on the Globtop of the FEB. The FEBs are placed in in the cooling box by bending them about 90 degrees and because of this situation the shielding is moving a bit. In addition, the electrical contact is provided by soldering.

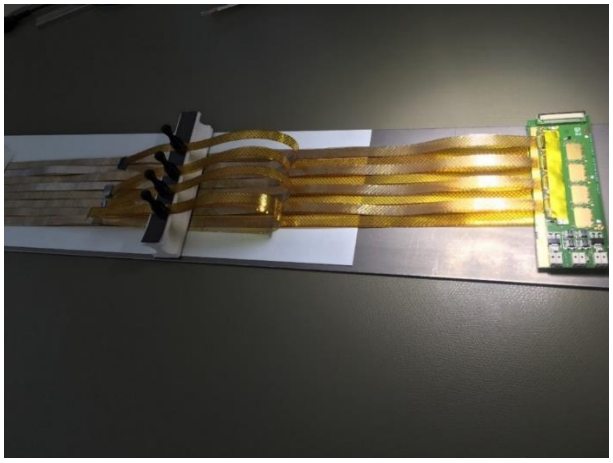

Figure 3.25: Shielding pocedure of the ASICs.

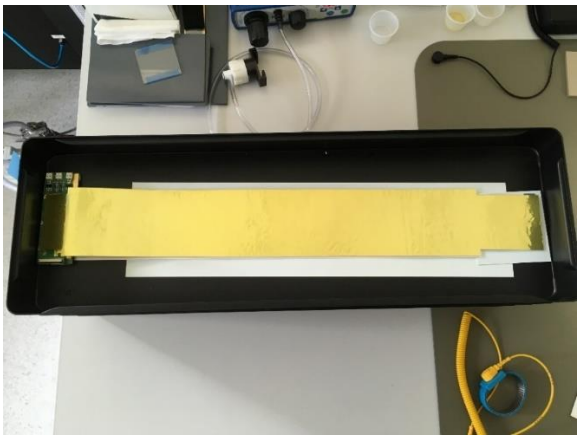

Figure 3.26: STS Module with shielding layer

3.6.2. Ladder Assembly

Assembly of modules on the ladder is the following step after the module assembly. According to the ladder assembly technique used in GSI, modules are assembled on a ladder one after the other and it can hold upto 10 modules. For mCBM modules, half size ladder with the real modules (figure 3.27) was assembled.

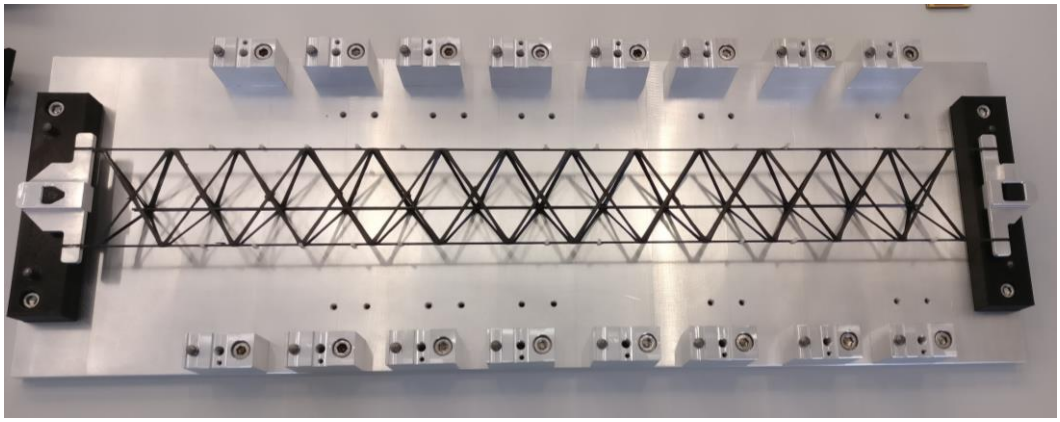

Figure 3.27: Ladder for mSTS

The tools that are used for the assembly of the ladders are simple and based on machining structure. The first step is to assemble the base plate with the ladder bearing blocks. The ladder is then glued onto the grooves of the bearings usimg Araldite 2011 glue. To assemble the modules on the ladder, glass fibre L-shaped structures, known as L-legs, are used to hold the sensors. For each sensor, 4 L-legs are required. The L-legs are fixed for gluing guided by a rail system to the carbon fiber structure. The next step is to clutch all the detector modules with a precision transfer tool and place it on top of the carbon ladder using for consecutive glueing. In order to reach accurate positioning of the sensor (in order of 100 μm) the fixture should be kept at a steady temperature in the environment and after this procedure the position of the sensors has to be measured.

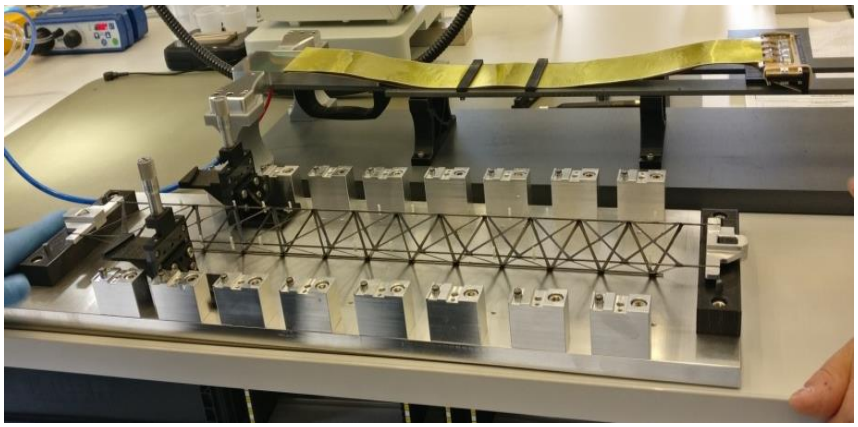

Figure 3.28: Tool that has been designed for the alignment of the modules to the ladders.

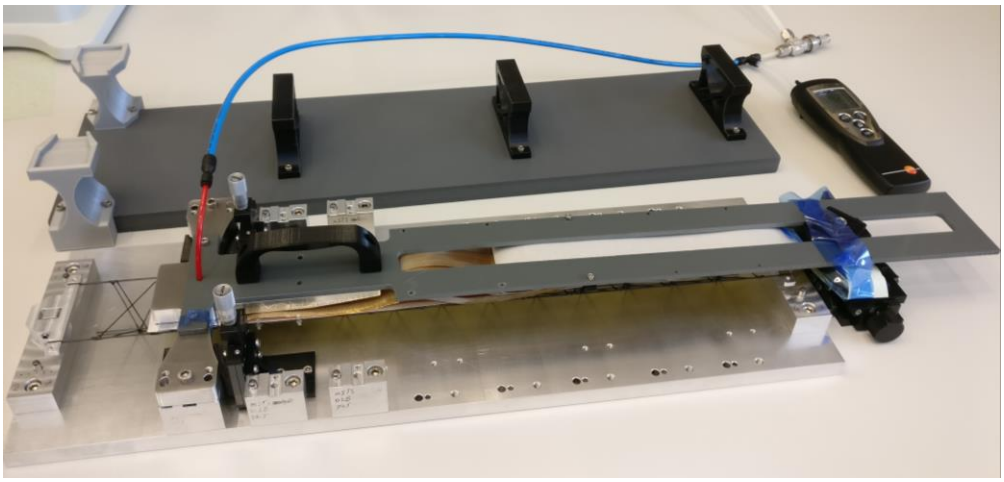

Figure 3.29: Alignment of the STS module

A tool has been designed and produced as illustrated in the figure 3.28. This tool has sensor holder which holds the sensor by applying some vacuum and is extended further which can hold a complete module. After the module is aligned to the tool, it is shifted to the ladder as shown in figure 3.30. The dowel pins inside the positioning blocks helps to provide the right position to the sensors while glued on the l-legs. For the mSTS two 6 x 6 cm^2 sensors can be mounted on the ladder using the same assembly technique. The ladders with modules are then transferred to the C-Frame [63].

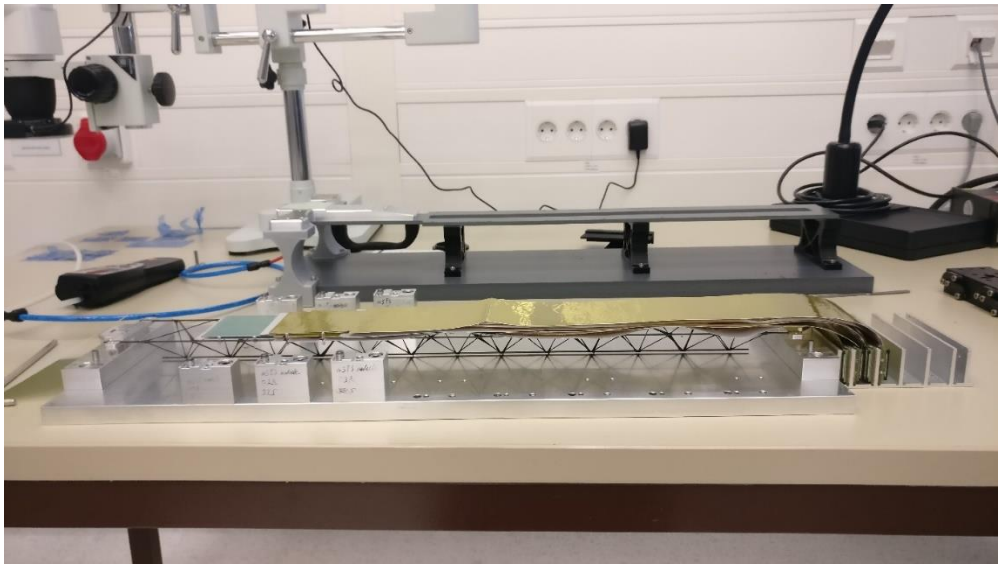

Figure 3.30: An example for a ladder with two mSTS modules.

3.6.3. STS-XYTER ASIC Test For mCBM

During the assembly part of the four modules of the mCBM, ASIC quality assurance should be tested in three step like first ASIC level, then ASIC with microcable and lastly ASIC with microcable and sensor. The primary aim of all those measurement is to check the connection status of the channels. Measurements were done at clean room at GSI. The set up also can be seen in figure 3.31 includes, pogo pin test socket, power supply, an AFCK card with FPGA

board and a dedicated PC. A python script is used in all measurement. In order to place the ASIC a vacuum tweezer is used.

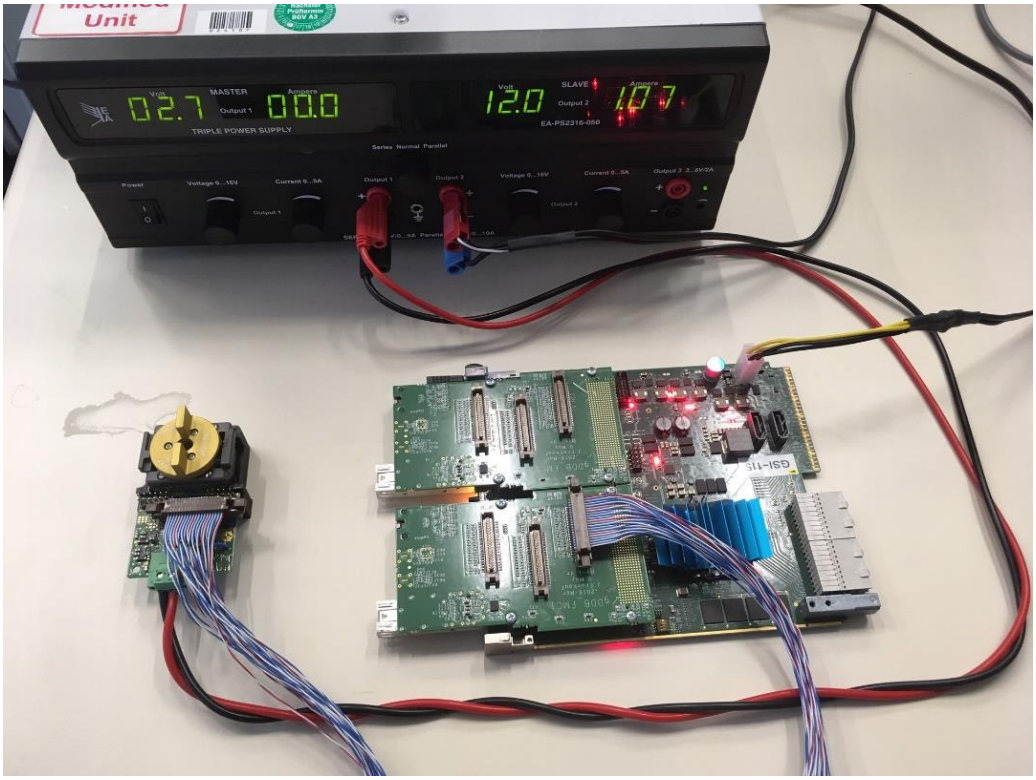

Figure 3.31: Test set-up in GSI clean room.

In measurements, as a first step, the ASIC is tested seperately and totally 98 ASICs were tested seperately for the mCBM assembly. ASICs which showed good quality were given to assembly process for the modules. Following this stage, microcables were bonded to ASICs and since we have two layer cable, in each bonding process we measured the noise level and hit distributions to be able to distinguish connected and unconnected channels. As a last stage microcables were bonded to sensor and again the connectivity was tested from the ASIC side. The noise level of a given channel depends on the input capcitance. This capacitance increases when a cable is attached and later when the sensor is attached. Therefore unconnected channels (Either broken at the ASIC/cable or the cable/sensor interface) can be identified by their lower noise level so unconnected channels were identified by checking the noise hit distributions in one specific channnel as can be seen clearly in Figure 3.32. It represents the connection check result of a spesific ASIC. The unconnected channel became visible as a continuous line when estimating the hit distribution in terms of ADC values. The benefical side of those measurements is the ability of bonding and rebonding the microcables during the assembly part after the pogo pin station measurements. Furthermore, figure 3.33 and figure 3.34 represents an example for second and third stage of the ASIC tests respectively.

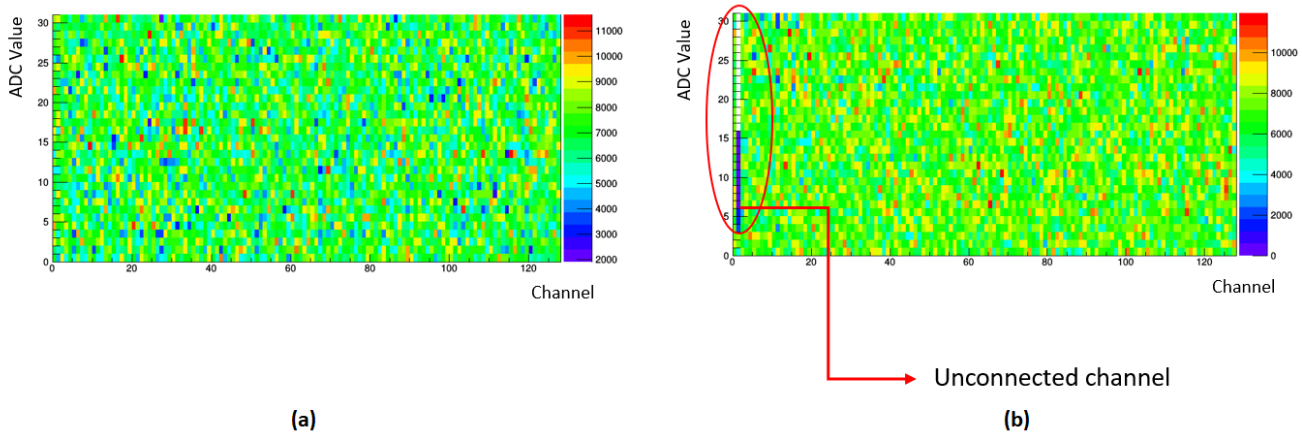

Figure 3.32: Noise hits read at the ASIC's ADC counters.(a) hit distribution for a good ASIC (b) hit distribution for an ASIC with unconnected channel.

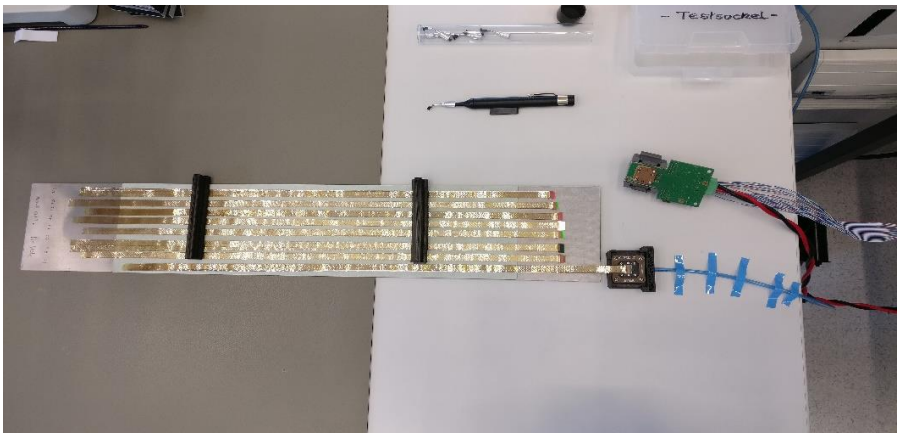

Figure 3.33: Test of connection between STS-XYTER-ASIC and microcable.

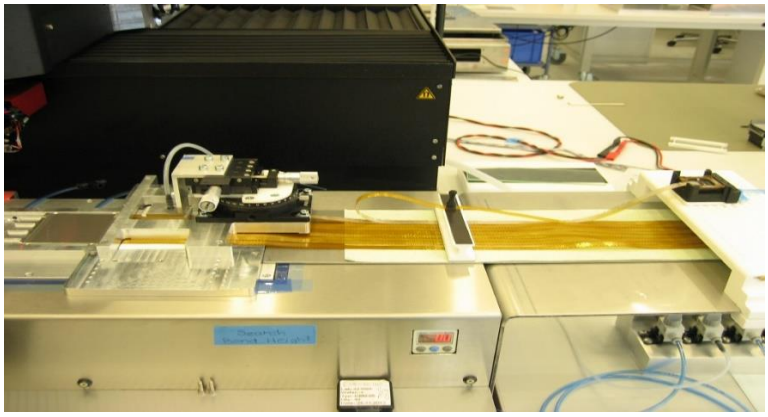

Figure 3.34: Test of connection between STS-XYTER-ASIC, microcable and sensor.

Except for a specific ASIC connection check, determining the unconnected channels are also possible after a noise check for a full module. Figure 3.35 is an example for this measurement and the unconnected channels can be seen easily for p and n side of the sensor at ASIC level.

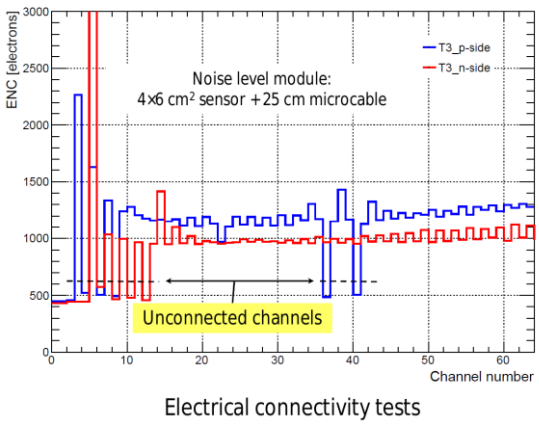

Figure 3.35: An example for the electrical connectivity test for p and n side of a module.

On the other hand, during the measurement, since the needles are very sensitive, it is possible to see some damages on them, so one should be very careful during the usage of the pogo station.

3.6.4. Test Box For mCBM Modules

The test box was design for mCBM module tests at GSI by engineers. The Aluminium box is a rectangle box and has several parts for placement of the full module: Front End electronic block for FEBs, cooling block and sensor holder. Furthermore it has a XY movable Sr-90 source holder for source measurements. The box also equipped with a water cooling for FEB and provides a shielding for the module since the aim to test the modules is to determine the ASIC performances in terms of broken or unconnected channels as well as the noise of the system. Such basic system needs to be used before the full module operation in experiment. As a read-out, a common readout board (C-ROB) was used that using CERN GBTX ASICs for data aggregation and electrical to optical conversion. The optical connections from the CROB go to a DPB (AFCK).

This measurements lead us to investigate the quality asurance of the ASICs after assembly and thus we can compare the results practically from pogo pin station and from the overall system. Beside, after module tests the possibility of termal damage for ASICs prompted us to take into consideration some precoutions for cooling the FEBs.

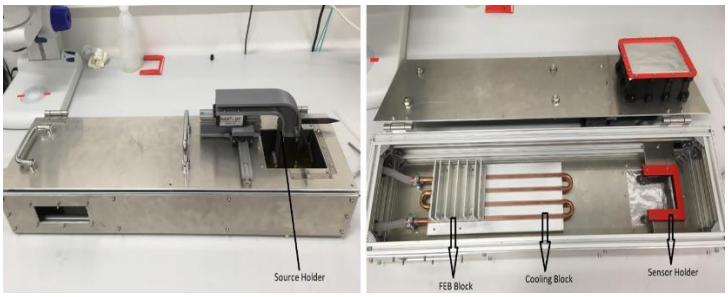

Figure 3.36: Module test box.

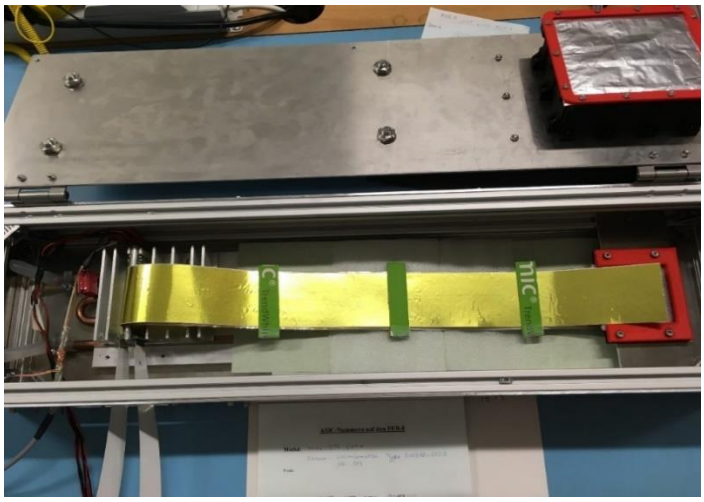

Figure 3.37: Test box with a module.

3.6.5. Powering The Sensor Modules

Due to power requirements of the asics, dimensioning of the power sources as well as the cooling resources were determined. Each of the 8 STS-XYTER asic converts charge pulses of 128 silicon sensor lines to up to five digital data streams (only one is used on the FEB8 at the moment). Two FEASTMP2 modules that DC/DC converters developed at CERN are located on the power board helps to power a FEB8 board. One converter creates the input voltage for the 1.8V regulators while the other creates the input voltage for the 1.2V regulators of the FEB8 board. In addition, a high voltage source need to be connected between n-side ground and p-side ground of the sensor in order to supply sensor bias. In addition, between the grounds of the two FEB8, a high voltage capacitor was placed to reduce the noise by providing a low impedance return path for AC signal currents [64].

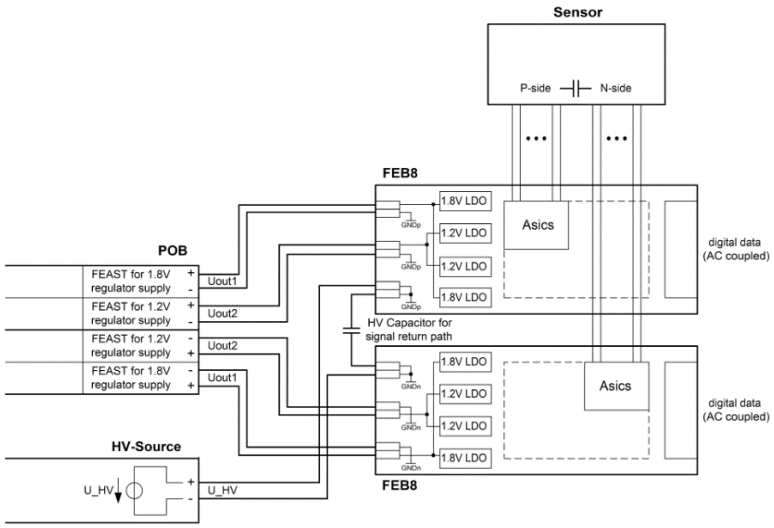

Figure 3.38: Schematic view of the STS module setup.

4. RESULTS

4.1. STS-XYTERV2 ASIC TEST RESULTS

For the quality assurance and module assemly, a total of 339 STS-XYTER v2 ASICs were tested. The results for bare ASIC measurements are shown in the Figure 4.1. The first histogram (a) represents the supply currents for all ASICs, before synchronization (red) and after full configuration (blue). The current before synchronization is one of the start-up parameter for the ASIC after power-on. This is, in most of the case, not well defined; around 3000 configuration bits in the chip may be in arbitrary states. The current value after configuration is expected to be around 0.6 A. After configuration some ASICs appear to be above the average, a little far from the central power consuption. Therefore, 20 ASICs show some problematic features out of 339 ASICs. Among those 20 ASICs, 5 of them have a broken channel, but nevertheless, they were taken into consideration for the statistics. Other ASICs have several problems such as no analog response, several broken channel and synchronization problems (figure 4.2). These plots are significant to understand the working principle of STS-XYTER ASIC and enable their assessment. The figure 4.1 (b) represents the statistics of the ADC range for the channel number 64 for electrons and holes. Measurements were taken at the same reference potentials for the ADC. The values are calculated based on the extraction of the lowest and highest discriminator threshold values from the selcted ADC channel.

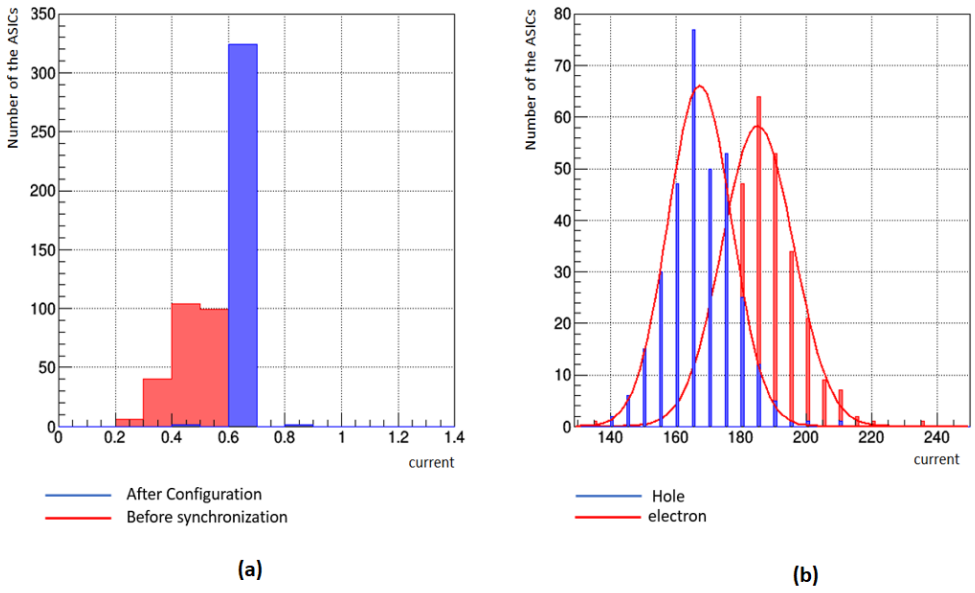

Figure 4.1: ASIC tests results for electron and hole configuration. (a) Current configuration (b) ADC range configuration.

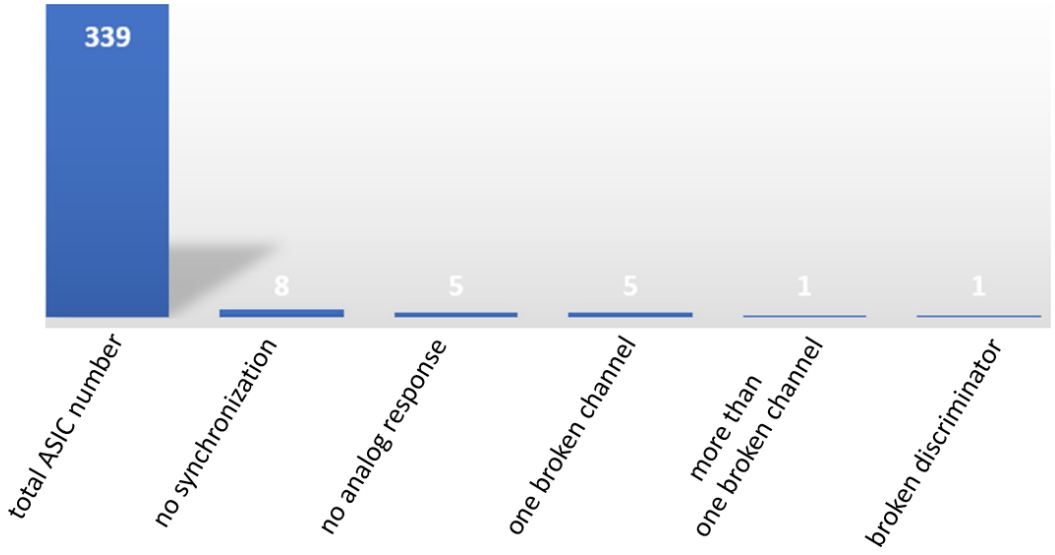

Figure 4.2: ASIC test statistics.

It's possible to determine the ADC gain settings. The parameters for both electron and hole configurations were determined in terms of amp-cal units and presented in the table 4.1. The ADC range parameters are used to determine the calibration range for both configurations.

Table 4.1: ADC Range and Gain results for electrons and holes.

	Electrons	**Holes**
ADC range(register value units)	185	167
ADC range(mV)	92.5	83.5
Amplifier gain(ADC Units/mV)	0.33	0.37

The ASICs that have shown good performance, were wire bonded to the Front End Boards (FEB) and after this procedure, the operative FEBs with a single ASIC were tested following the same conditions explained above. After the measurements, FEBs which show good performance are selected for glop-top process. The bonded chip with its filigran bond wires is covered with glue to protect the ASICs. As result, a total of 138 FEBs out of 146 have passed the measurement process. The results are shown in table 4.2. The measurements reveal some variations in the ASIC operation after being connected to the electronic circuit. The measurements show that 146 out of 162 ASICs randomly picked out of the production batch worked as expected. The yield is 91% and the result were satisfactorily high.

Figure 4.3: Prototype FEB-Bs with STS-XYTERv2 ASIC

Table 4.2: FEB test statistics.

Total Number of Tested FEBs	146
Number of FEB with problematic performance	8
- Very high current	2
- No analog response	1
- No fast discriminator response	1
- One or more individual broken channel	4

4.2. TEST RESULTS DURING MSTS MODULE ASSEMBLY

Additional tests were done during the mCBM module assembly. A total of 48 ASICs were chosen for assembly four mSTS modules (01Tr,01Tl,02Tr and 02Tl). Test results can be seen in Table 4.3. Due to technical problems with the pogo-pin station, some ASICs were not fully tested.

Table 4.3: ASIC test results during the mSTS module assembly.

ASSEMBLY STAGE	**Number of tested Asıcs**	**SETUP REQUIREMENT**	**TEST PURPOSE**	**TIME**	**Number of Problematic Channels**
Module 01T-r	16	Pogo pin station	Check electrical connections	5 min	3
Module 01T-l	8 (p-side)	Pogo pin station	Check electrical connections	5 min	-

Module 02T-r	16 (only test with microcable)	Pogo pin station	Check electrical connections	5 min	2
Module 02T-l	16	Pogo pin station	Check electrical connections	5 min	-

The ADC gain and current consumption statistics are also shown in figure 4.4 and table 4.4 before calibration. Only two modules were fully tested during assembly and the number of unconnected channels were five. However, for module 01Tl, only p side was tested. For module 02Tr, the ASICs were tested after they had been bonded to microcables. When assembly process were completed, some ASICs did not give any response. It has been realize that an excess of measurements might damage the bonding areas of the ASICs. It's result in a connection block between FEB and ASICs.

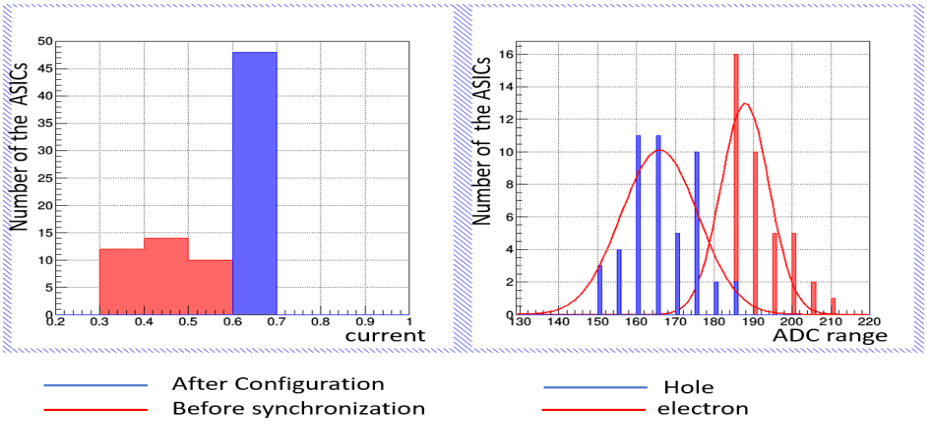

Figure 4.3: ASIC QA test results for electron and hole configuration

Table 4.4: ADC Range and Gain results for electrons and holes before calibration.

	Electrons	**Holes**
ADC range(register value units)	187	165
ADC range(mV)	93.5	82.5
Amplifier gain(ADC Units/mV)	0.33	0.37

Testing the ASICs for several times can lead a damage on bonding. The closeness of conductive lines to bonding pad areas can cause some shorts on ASICs. This critical line can be seen in the figure 4.5. This is one of the reason of the problems that we have been facing during assembly.

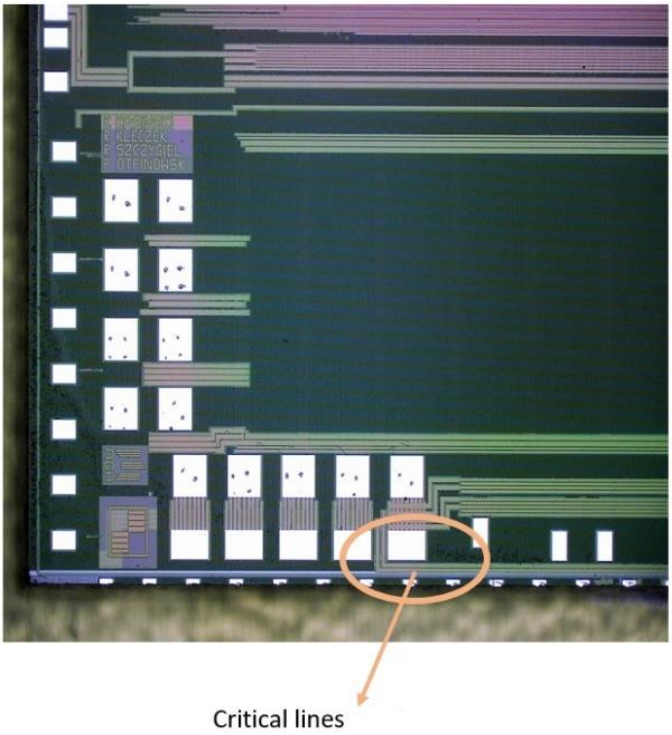

Figure: 4.5: Critical bonding area for the STS-XYTER ASIC.

For preventing those problems, a study is currently going on. It can be easily studied by connecting the FEBs to a readout board. The process consists of checking the synchronization function in order to check the communication between ASIC and FPGA backend and power consumption measurement. With these tests it is possible to see both proper functionalities of the readout interface, and the working situation of ASIC powering.

4.3. NOISE MEASUREMENT WITH STS-XYTER ASIC

The noise level in the electronic system is a critical issue in the STS expriment due to the self trigger electronics. Differents sources like cable length, ground skins and read-out chain in general can affect the noise performance of the system. Several measurements must be performed as a reference before getting the system ready for oparation. In those cases, the noise was measured for single ASICs and, in order to clarify the structure, different microcable settings were used and bonded to the ASICs. In the figure 4.6, the first plot (a), represents the noise measurement for a single ASIC and the second plot (b) represents the noise results for the ASIC with 12 cm microcable. The noise structure without and with microcable shows an expected degradation. It has additionally two unconnected channels. The edges structure for the external channels, in the second plot, can be explained base on insufficient shielding of the microcables.

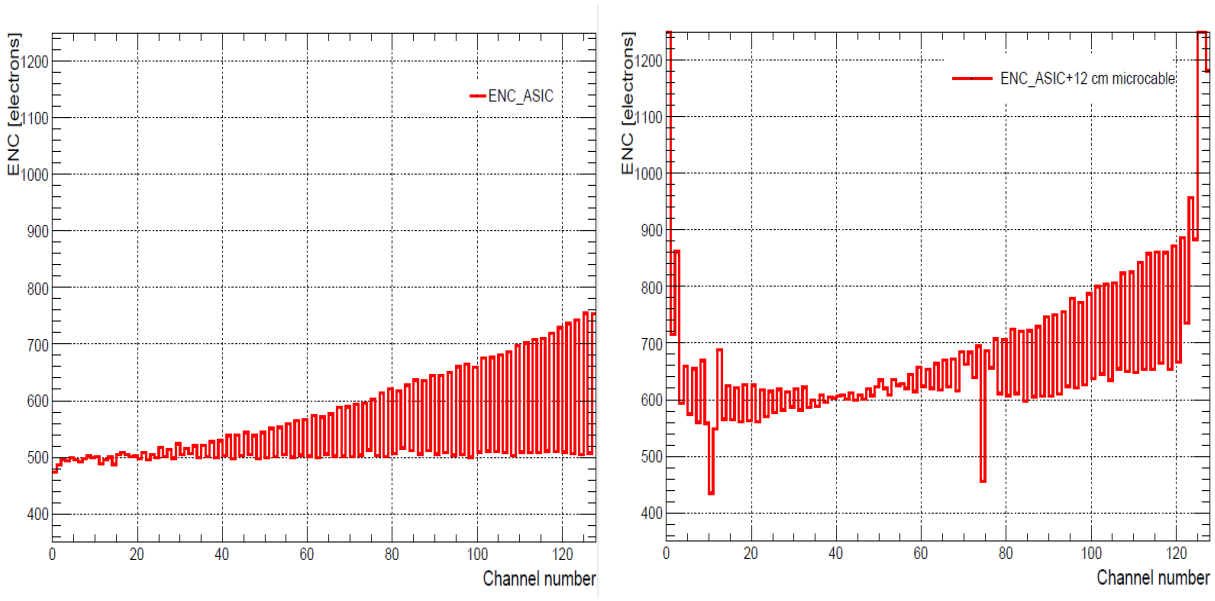

Figure 4.6: Noise structure for STS-XYTER ASIC for diferent configurations. (a) Single ASIC with front-end board type B. (b) ASIC+front-end board type B+ microcable

Meanwhile, noise measurements for ASIC with three different microcable length (12cm, 25cm, 50cm) were studied (see figure 4.7). The noise results in ADC and fast discriminator depend on the cable length and microcable capacity. As a result, noise obtained is proportional to the cable lengths that is clearly seen in figure 4.8.

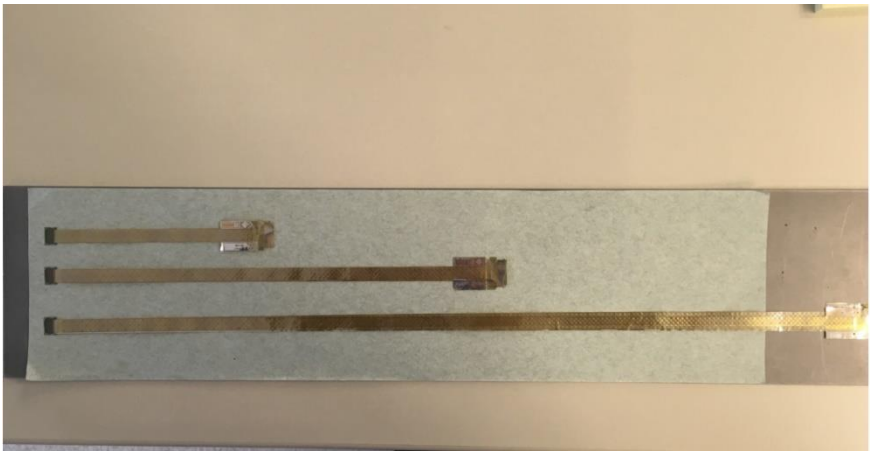

Figure 4.7: ASICs with three different microcable length.

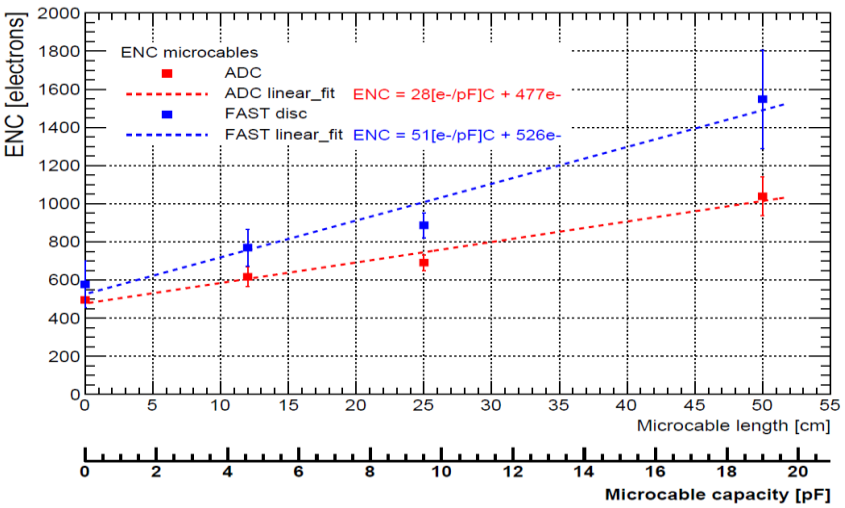

Figure 4.8: Noise results for three different microcable length.

4.4. TEST RESULTS FOR THE MCBM MODULES

One of the most significant process is the test of the mSTS modules, with a close to the final STS-CBM detectors design. At this point, the performance of the STS/MUCH- XYTER ASICs and the noise structure of the module is very important. Several tests were performed in order to study four modules of the mini STS. Exceptionally, the first module of the mCBM could not be fully tested and the calibration was done later due to a lack of pogo-pin station. It has been seen that ASIC performances were different compare to the results in the prevoius state of module assembly. Since some ASICs shows a short cut problem and also it is not possible to communicate with them Some ASICs show no connections with microcables and the edge part of the graphs shows more noisy structure due to of the distance from the bias line. Noise tests were performed with 500 V with and without biasing voltage. In each module were read-back 1024 channels of the p and n side of the sensor. The noise performances of the full modules can be seen in the figure 4.9 and 4.12. It can be seen clearly that the noise performance is not very good, in addition one ASIC from both n and p side was dead and both sides have some unconnected channels. The edges shows some fluctuations dependent on shielding which also seen in ASIC+microcable noise test. In order decrease the noise levels, some procedures were implemented to detector system, such as shielding and filtering. When there are two or more devices in the system, this can lead a ground loop which affects the measurement accuracy due to slight differences in the actual potential of each ground point generate a current flow from one device to the other. This current, create a voltage drop reflected in the noise and lead an inaccuracy in the measurement at the ADC input. In order to reduce the noise levels, the ground loops and at least shield on the devices should eliminate [65]. So, the system were shielded from FEB through to microcables and sensor.

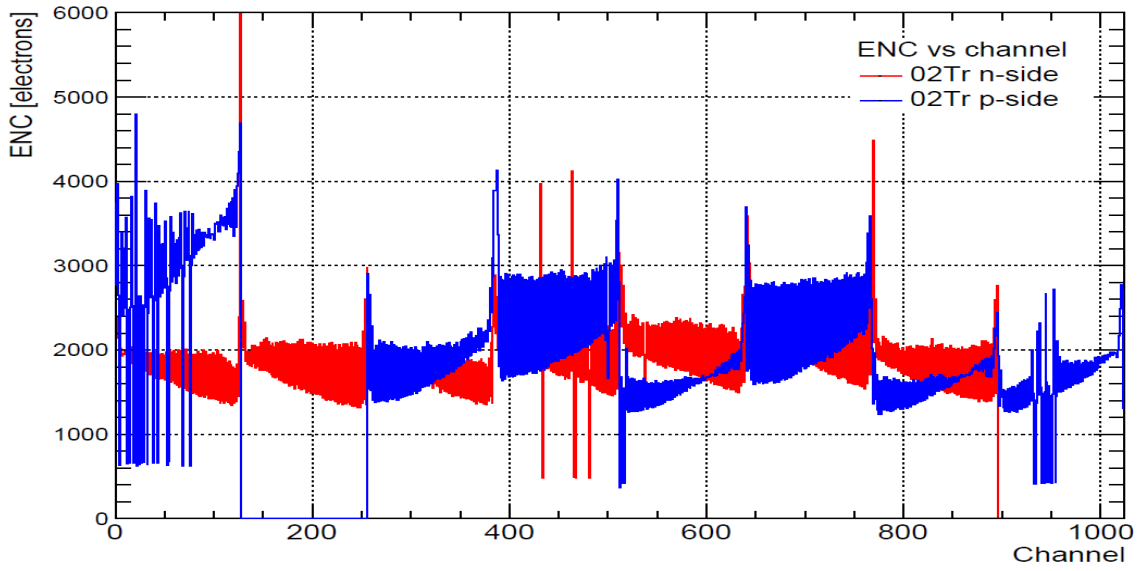

Figure 4.9: Noise measurement of module "02Tr" for n and p side.

One significant issue, that need to be mentioned, is the ADC gain spread for all channels. In figure 4.10 and 4.11, the ADC gain can be seen for "02Tr" module as reference. The n side of the module shows more deviation in the gain spread so in figure 4.11 we can see more narrow peak on p side.

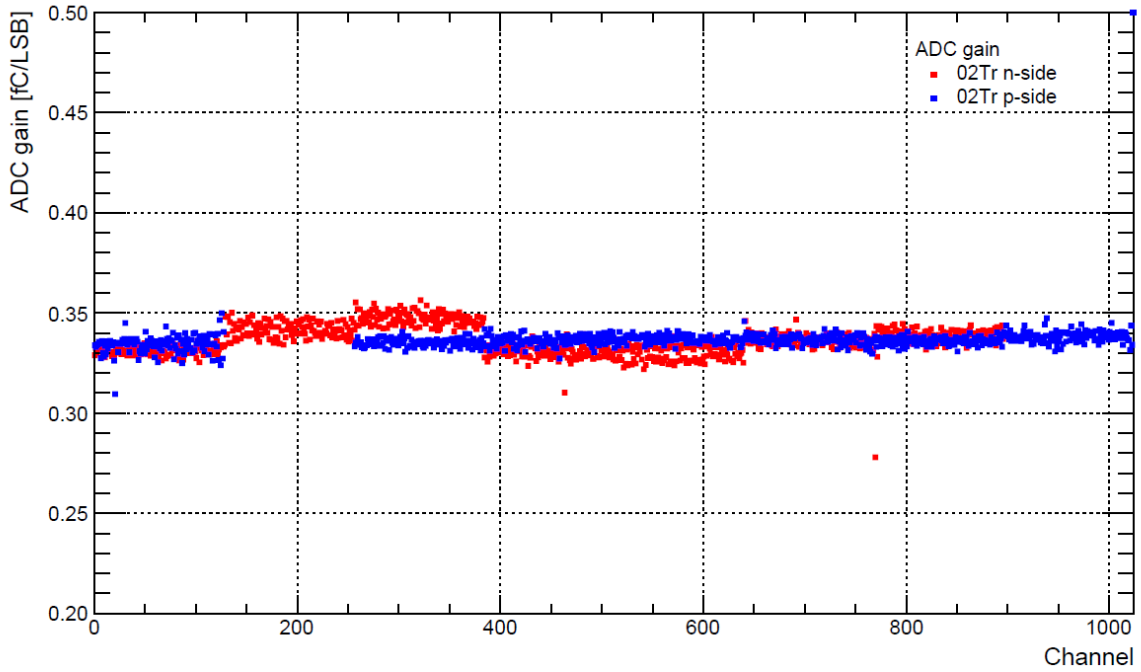

Figure 4.10: ADC gain spread for 1024 channels.

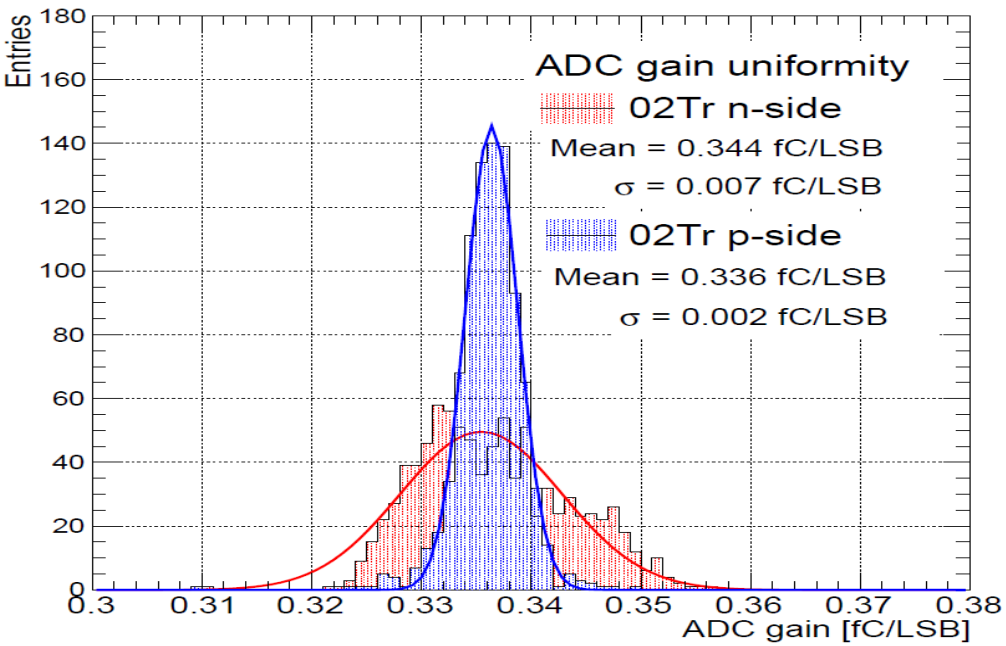

Figure 4.11: ADC gain for 02Tr module.

Likewise, figure 4.12 represents the noise performance of module "01Tr", two ASICs from n side and one from p side were dead and both sides have some unconnected channels.

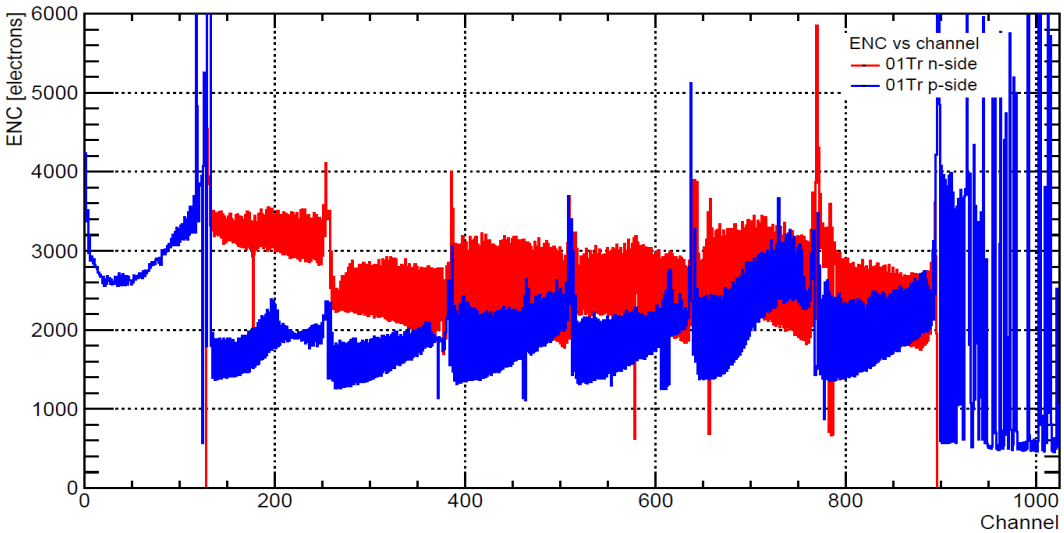

Figure 4.12: Noise measurement of module "01Tr" for n and p side.

However, ADC gain spread for all channels is given in figure 4.13 and 4.14 for "02Tr" module. The n side of the module shows more deviation in the gain spread so in figure 4.14 we can see more narrow peak on p side.

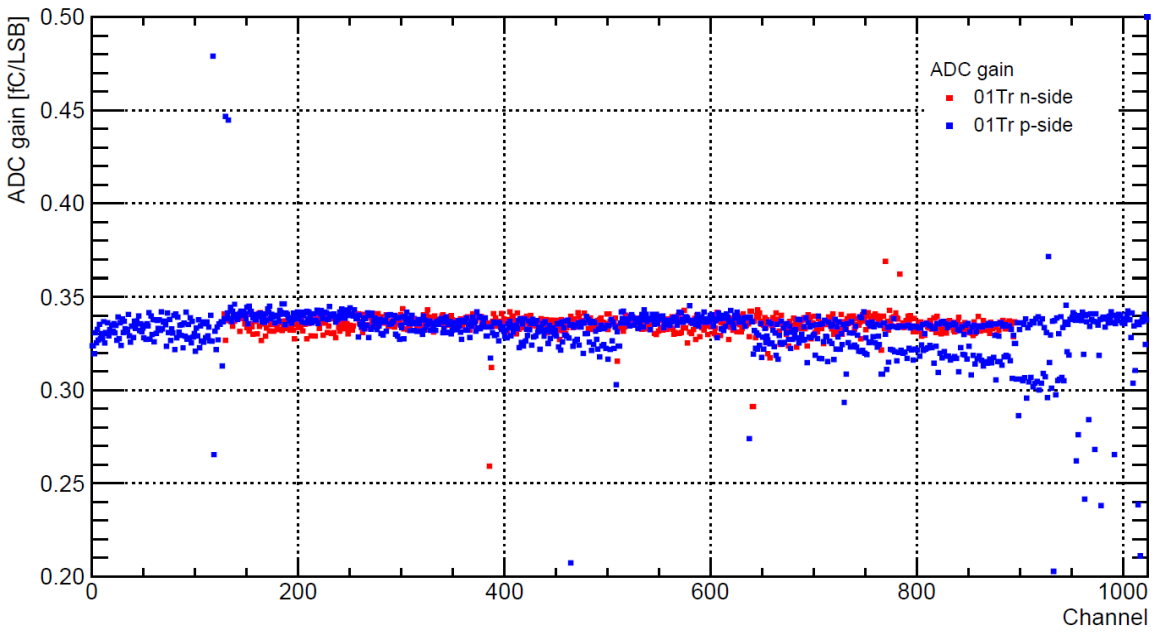

Figure 4.13: ADC gain spread for 1024 channels.

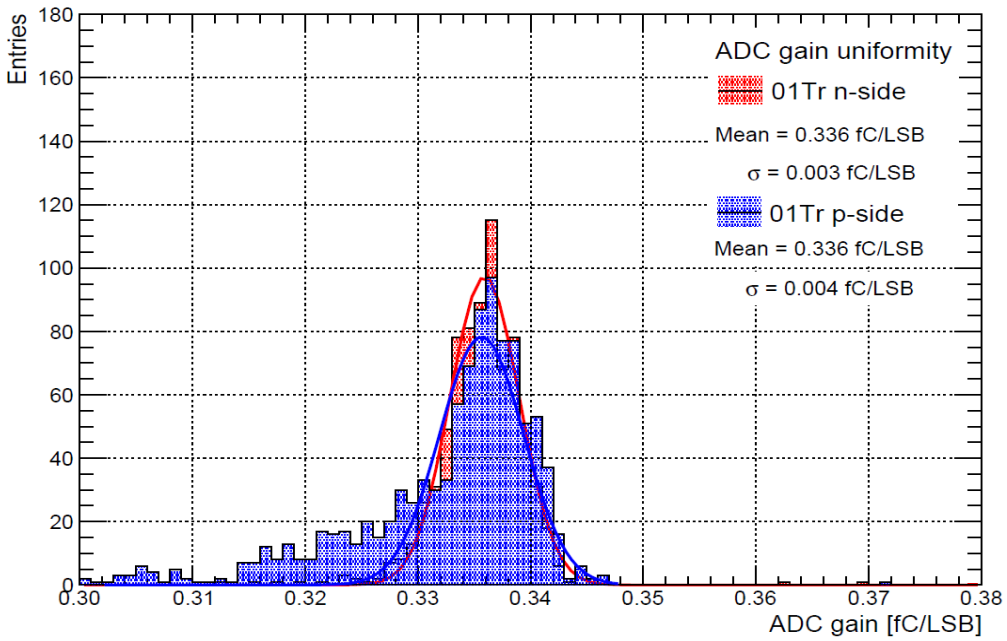

Figure 4.14: ADC gain for 01Tr module

As a summary, the statistics for the two mCBM modules was represented in table 4.5 in terms of broken ASICs, broken channels and equivalent noise ratio for electron and hole configurations.

Table 4.5: Module test statistics.

	Faulty ASICs		Faulty-broken channels		ENC [e-]	
Module	**N-side**	**P-side**	**N-side**	**P-side**	**N-side**	**P-side**
01Tr	2	1	264	139	2684	2188
02Tr	1	1	133	155	1948	2078

4.5. FIRST BEAM RESULTS FOR MCBM EXPERİMENT

First system integration was done (figure 4.15) as well as first beam was taken in December 2018 for mSTS, mMUCH, mTOF and T0 detectors. Ag (45) at an energy of 1,2 AGeV was used as a beam at SIS18. Even though there was some problems in software and detector systems, the detector system worked reasonably good.

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Figure 0.1: mCBM system in the cave.

For the mSTS case two module of the right orientation were mounted on a mechanical Aluminum C-frame. The longest module has a 50 cm longest micro-cable. A prototype STS power board was provided with low and high-voltage supply systems. Among two module there was one problematic FEB which has one side non-operative. Data were taken with only the n side of the Module “01Tr” and only 3 ASICs were functional. The read out of this module was functional when it was tested in STS test box so it is thought that there could be a thermal damage during the measurements in the test-box. For the module “02Tr” p side was fully operational and from n side 7 ASICs were functional. The system had very noisy structure. Noise increased when both side were operated and it was higher than the test box in the STS

lab about a factor of 5. So, maximum tresholds were set it high for the module, in order to be able to get a proper read out. Furthermore, strong odd-even channels difference was observed.

Table 4.6: ASICs functionalities during mCBM run.

	module 01Tr	**module 02Tr**
n-side	*3 ASICs are functional*	*7 ASICs are functional*
p-side	*no read-out*	*all ASICs are functional*

Figure 4.16 and 4.17 show the hit distributions per channel. Notably, the odd-even channel effects can be seen clearly in figure 4.16. As it is represented in both figures but it can be seen in detail in figure 4.17, around channels between 129-260 there is a faulty ASIC from which no read out were obtained.

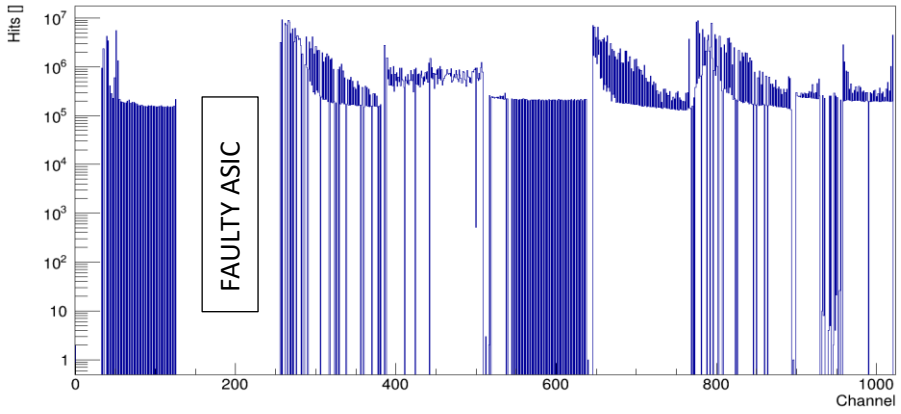

Figure 4.16: Hits per channel.

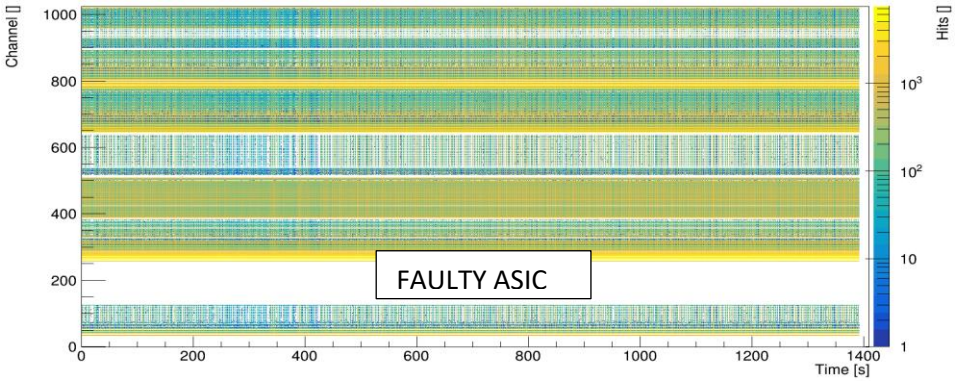

Figure 4.15: Channel rate evolution.

4.5. RESULTS AND DISCUSSION

The Compressed Baryonic Matter (CBM) experiment will be one of the foremost experiment of the future Facility for Antiproton and Ion Research in FAIR. The aim of the CBM is to explore the QCD phase diagram in the region of high baryon densities using high-energy nucleus-nucleus collisions.

The Silicon Tracking System (STS) is the core system for particle tracking of the CBM detectors. Since high beam intensities will be provided, self-triggered electronics need to be used to read-out detector systems for CBM Experiment. The developed STS-XYTER ASIC is the dedicated electronic for the read-out system from double sided silicon micro strip sensors. Thus, it is the fundamental requirement to do quality assurance tests before the system integration and basic ASIC functionalities like current, performance 0f each channel and ADC range can be checked with a prototype pogo-pin station. The characterization of these ASICs have been done for the first time in this thesis. As a first step quality assurance tests was done for the 339 ASICs as well as for the prototype FEBs that allows to check the ASIC performance. As a result the percentage of 94 was obtained as a yield. Together with ASIC tests, another quality assurance measurements for sensors and other detector systems are being in process and great improvements were achieved. These studies will constitute one of the fundemental process for the upcoming CBM experiment.

On the other hand, a mini version of the CBM experiment were planned to test the quality of detectors and electonics and it is called “Mini CBM” experiment. The first prototype modules for mini CBM were assemblied and tested in the GSI laboratory. Quality assurance of the electronic system as well as noise performance and the complete detector modules were studied in order to establish the reference values for such system. The noise measurement results seems to be below 3000 e^-, more stable for p side, which is sufficient for the tracking but not enough and need to be reduced.

First beam was taken for mCBM with SIS18 at GSI in December 2018. In addition, first resutls shows that detector systems still need some improvements in terms of noise. So, adding some extra shielding for read out part and additionally adding two more module to the C-Frame was decided.

Further studies are still being developed and studied for the detector modules in order to apply best simulations to the real CBM Experiment. In addition for the real experiment other further studies will be as below:

- The installation of the mCBM detector system is completed substantially with detector and front-end electronic tests as well as the installation of test modules.
- The test phases for the CBM Experiment are ongoing and the system installation is planned in 2022.
- The experiment will start out in 2024. However, the mini CBM experiment was planned as a preliminary stage. The mCBM is built to define the full functionality performance of the detector test, data collection and analysis components under the conditions of the SIS18 accelerator of GSI and is a test setup of the CBM.

- The installation of approximately 896 detector modules and the further improvement of operational performance will be a pioneering reference for those who wish to work with such systems.
- With the implementation of the CBM Experiment, a large scale and complex detector system will examine the structure of the matter in the early universe and it will be the first system that provides a more detailed information for long-term studies.

As a conclusion, characterization of prototype systems is a necessary step in order to run a system consisting of multiple detector components such as CBM. In this thesis, the assembly processes of the STS detector system are given. In addition, the characterization of STS-XYTER ASICs, which constitute the most important part in the electronics and provides the data acquisition from silicon micro-strip detectors, has been studied. It is important to carry out these test steps so that the CBM test can be carried out at full performance, as well as a preliminary experience of the problems that may be encountered in the test.

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