Front-end electronics of the CBM Silicon Tracking System

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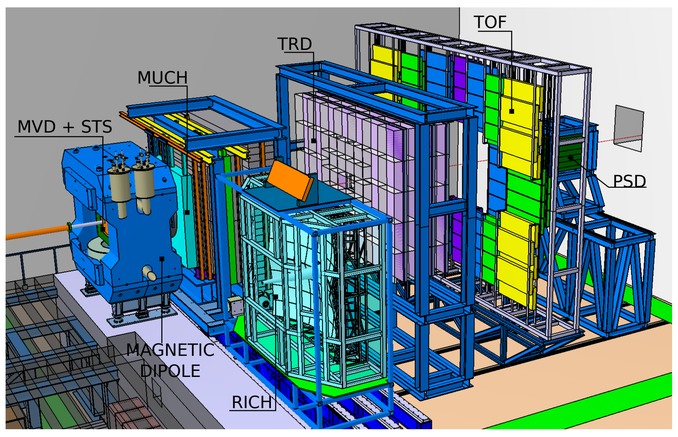
The Compressed Baryonic Matter (CBM) experiment & the Silicon Tracking System (STS)

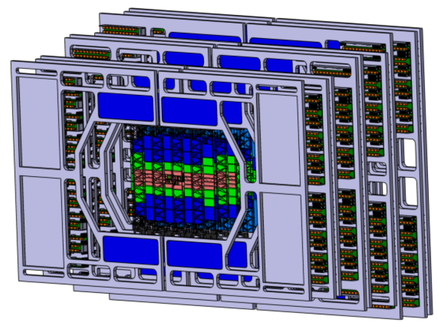
The CBM experiment:

- Explore the QCD phase-diagram at moderate temperature and high density.
- Au + Au @ 2-11 AGeV (SIS100) at 10^5-10^7 interactions/s.
- Fast self-triggering electronics and time-stamped readout.
- High speed data processing and acquisition system.
- 4D event reconstruction and fast selection algorithms.

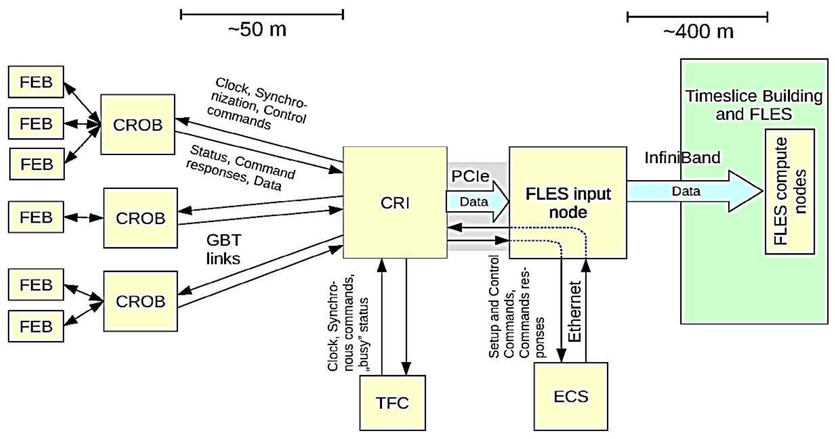


STS features & requirements:

- 8 tracking stations inside 1 T field.
- Double-sided Si micro-strip sensors ~300 μm thickness and 7.5° stereo-angle between front and back side strips.
- High efficiency and momentum resolution.
- Tracking up to 1000 charged particles/collision.
- Radiation hardness: 10^{14} 1 MeV n_{eq}/cm^2.
- Low mass: material budget per station in the range $0.3 - 1.5\%$ X_0.



The Silicon Tracking System Readout Chain



Block diagram of the STS Readout chain

Front End Board (FEB)

Part of a functional module, where 2 FEB with custom designed ASIC are connected via microcables to a Si sensor.

- Every FEB contains 8 STS-XYTER ASICs for reading out 1024 channels.
- Provides digitized hits.
- Located close to the Si sensors.

Read out Board (ROB)

- Data aggregation from several ASICs.
- Optical readout interface.
- Control and clock distribution.
- Based on CERN GBTx and Versatile Link components.
- Located inside STS box.
  → Limited space.
  → Radiation hardness.

Common Readout Interface (CRI)

CBM DAQ layer with common hardware platform.

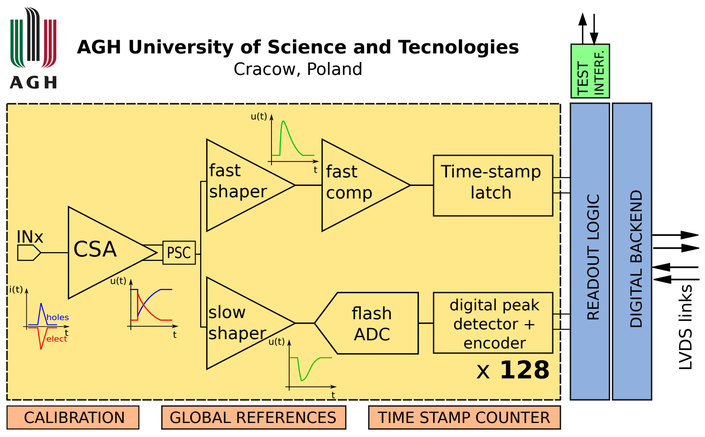
- FPGA based.
- Timing and control interfaces.
- Data preprocessing.

First Level Event Selection (FLES)

- Time slice building & full event reconstruction.
- Online event selection.

Front-end Electronics & Full Detector Modules

STS-XYTER → **S**ilicon **T**racking **S**ystem + **X,Y** coordinates + **T**ime and **E**nergy **R**esolution
Low power, self-triggering ASIC dedicated for reading out the double-sided Si sensors.

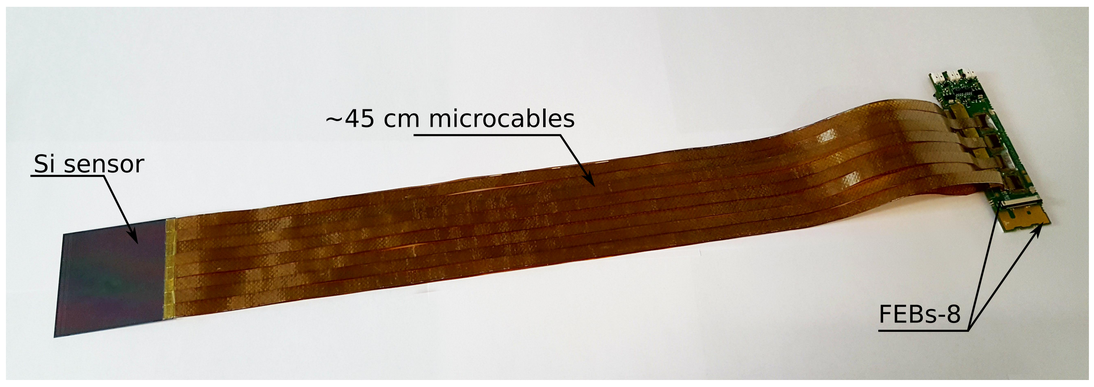


STS-XYTER functional blocks.

STS-XYTER features:

- 128 readout channels + 2 test channels.
- Time resolution: ~5 ns.
- 14 bit time stamp.
- 5 bit flash ADC/channel.
- 15 fC dynamic range.
- Radiation hard layout.
- Digital backend compatible with the CERN GBTx data concentrator.

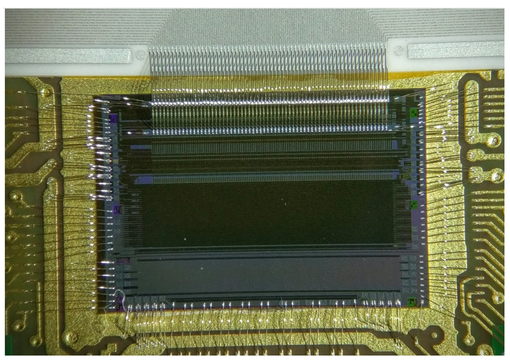
Full Detector Module Prototype → 6.2×6.2 cm^2 silicon micro-strip sensor + 45 cm microcable.



ASIC Startup and Basic Functionalities

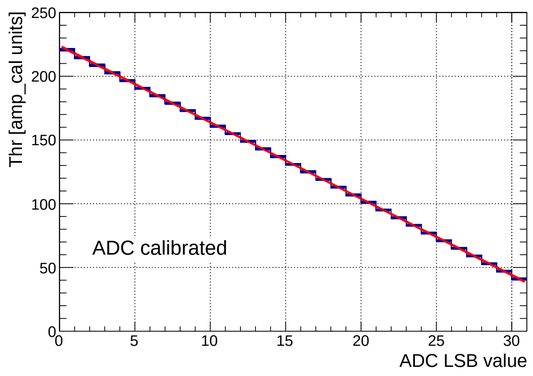
Test of comunication & backend interface:

- Communication interface.
- Synchronization protocol.
- Device access and configuration.
- Register access (Write/Read).
- Generating and reading out test hits.



STS-XYTERv2 prototype.

Calibration:
Development of test procedures to calibrate and evaluate in-channel ADCs .



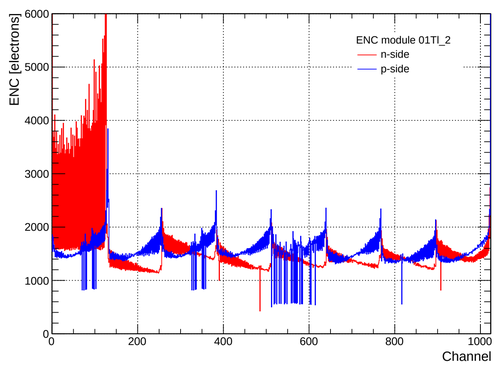
ADCs linearity for 128 channels.

Features:
-Internal pulse generator (range up to 15 fC)
-Global registers set ADCs range.
-Every ADC channel has 31 discriminators with individually adjustable threshold (8 bit).

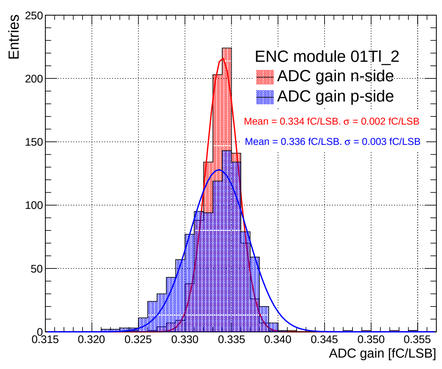
ASICs and Module Tests

Module readout & Equivalent Noise Charge (ENC):

First test of a fully assambled module.
Estimated noise level per channel

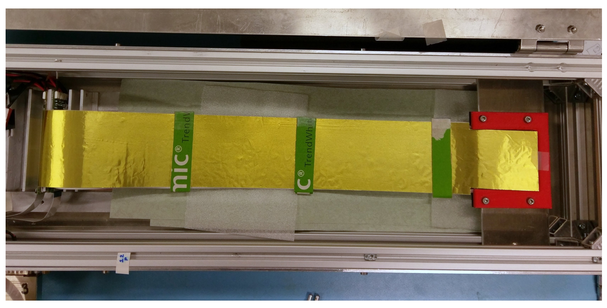


Distribution of the ADC gain for both polarities.



Stability test and ENC as function of time:

Test box designed for testing and cooling a full detector module.



ENC measured as function of time for electrons & holes.