Conversion time limited VME readout and signal exchange

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NUSTAR DAQ

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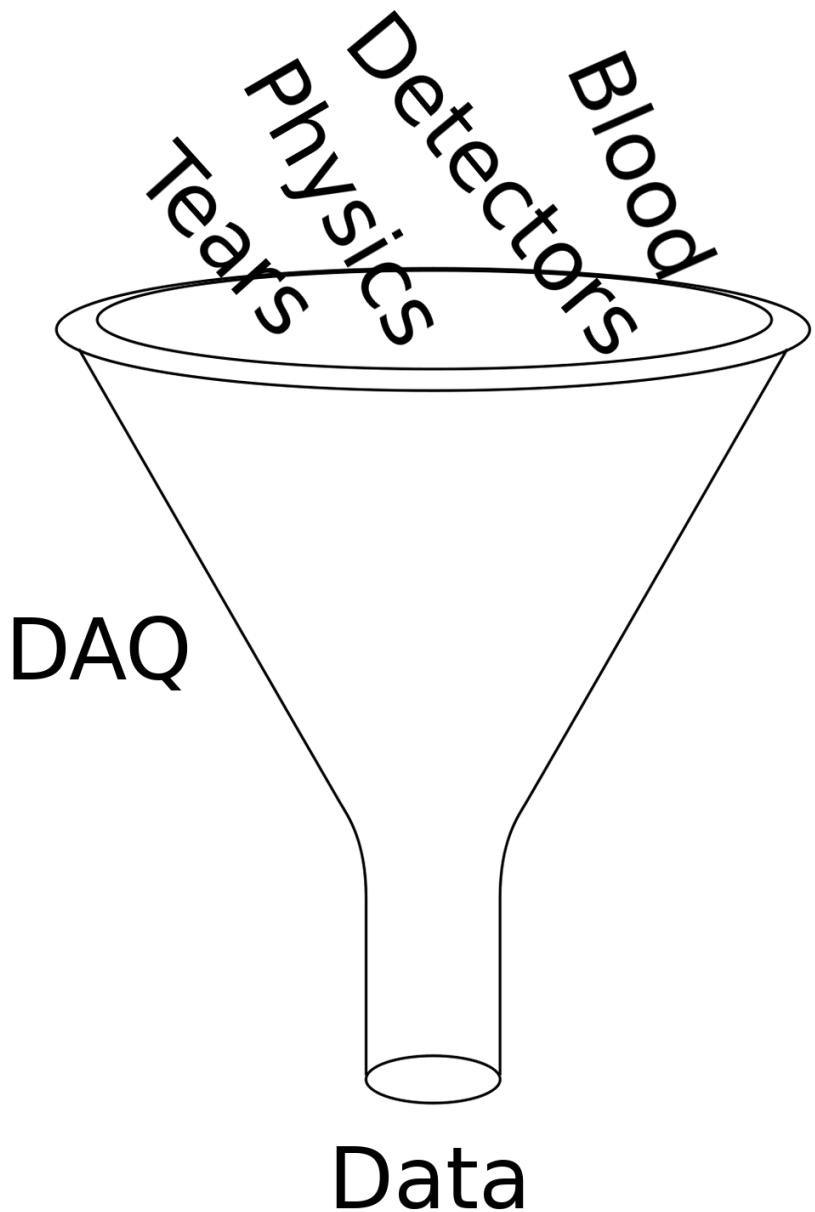
Glowing backplanes

In collaboration with:

J. H. Jensen (AU), B. Löher (TUD/GSI), H. Törnqvist (TUD/GSI), H. T. Johansson (Chalmers)

Experiments



Truth

More (good) data

$=$

easier (better) analysis

Constraints

Man power

Aarhus $\sim$ 5 people
ATLAS $\sim$ 3000 (scientific) people
NUSTAR $\sim$ 700 (scientific) people

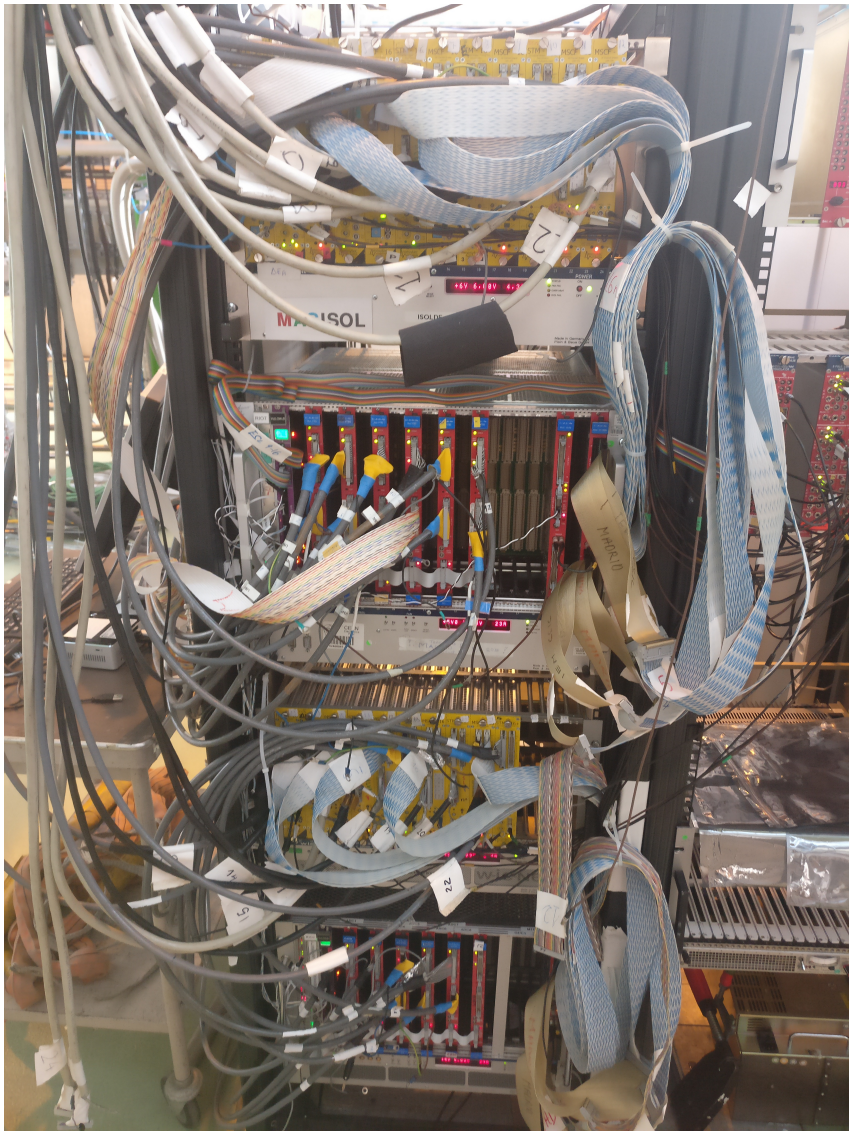
Money

Aarhus $\sim$ 0.5 M€
ATLAS $\sim$ 500 M€
NUSTAR ?

Solution?

Modular electronics chain

Detector $\rightarrow$ Preamp $\rightarrow$ Amp $\rightarrow$ ADC $\rightarrow$ PC



VME

More (good) data

$=$

easier (better) analysis

$\Downarrow$

Push the modules

Bottleneck I

Digitization time

CAEN v785 $\sim$ **7us**

Mesytec MADC32 $\sim$ **2us**

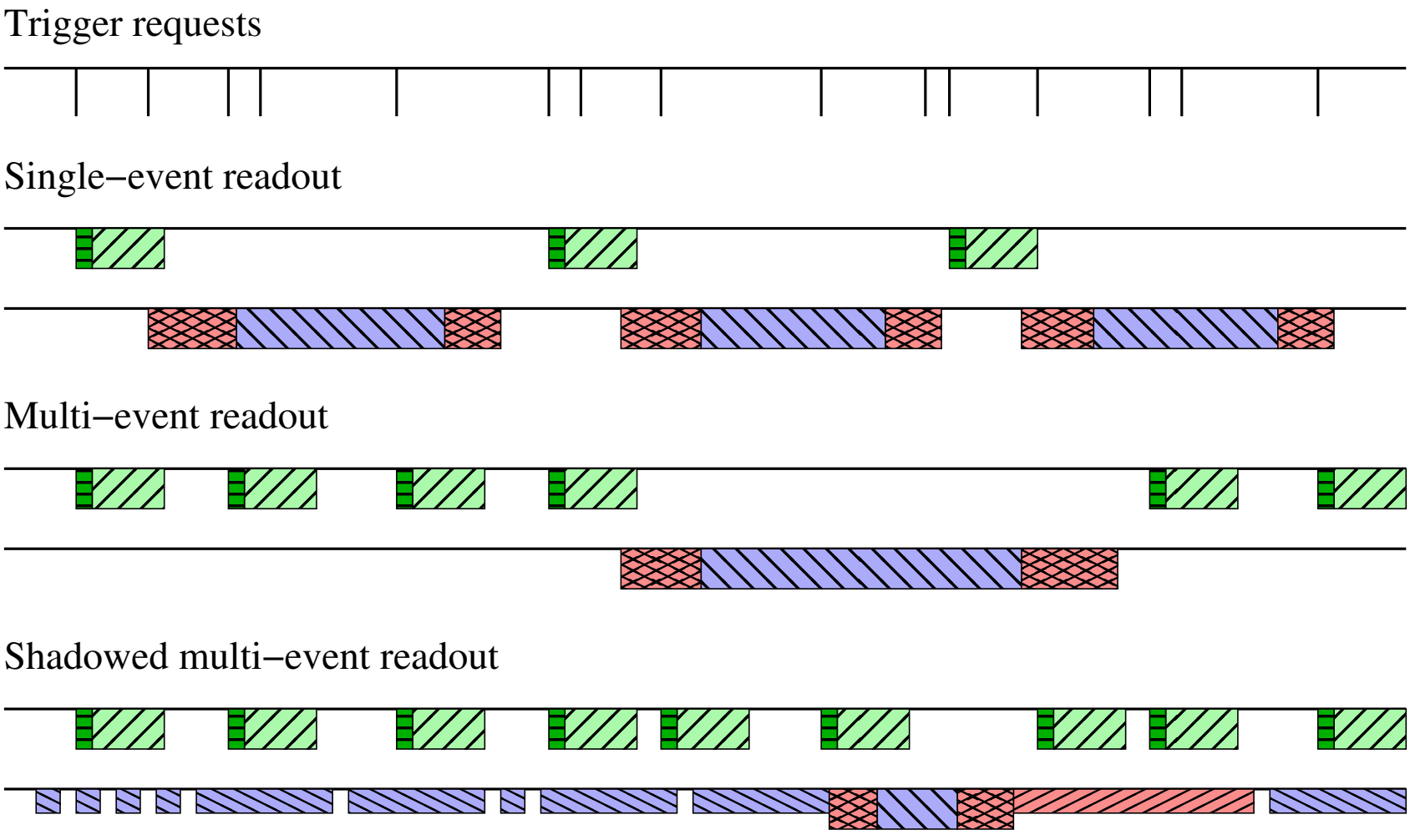
Readout time

Motorolla MVME $\sim$ **1.3us/word**

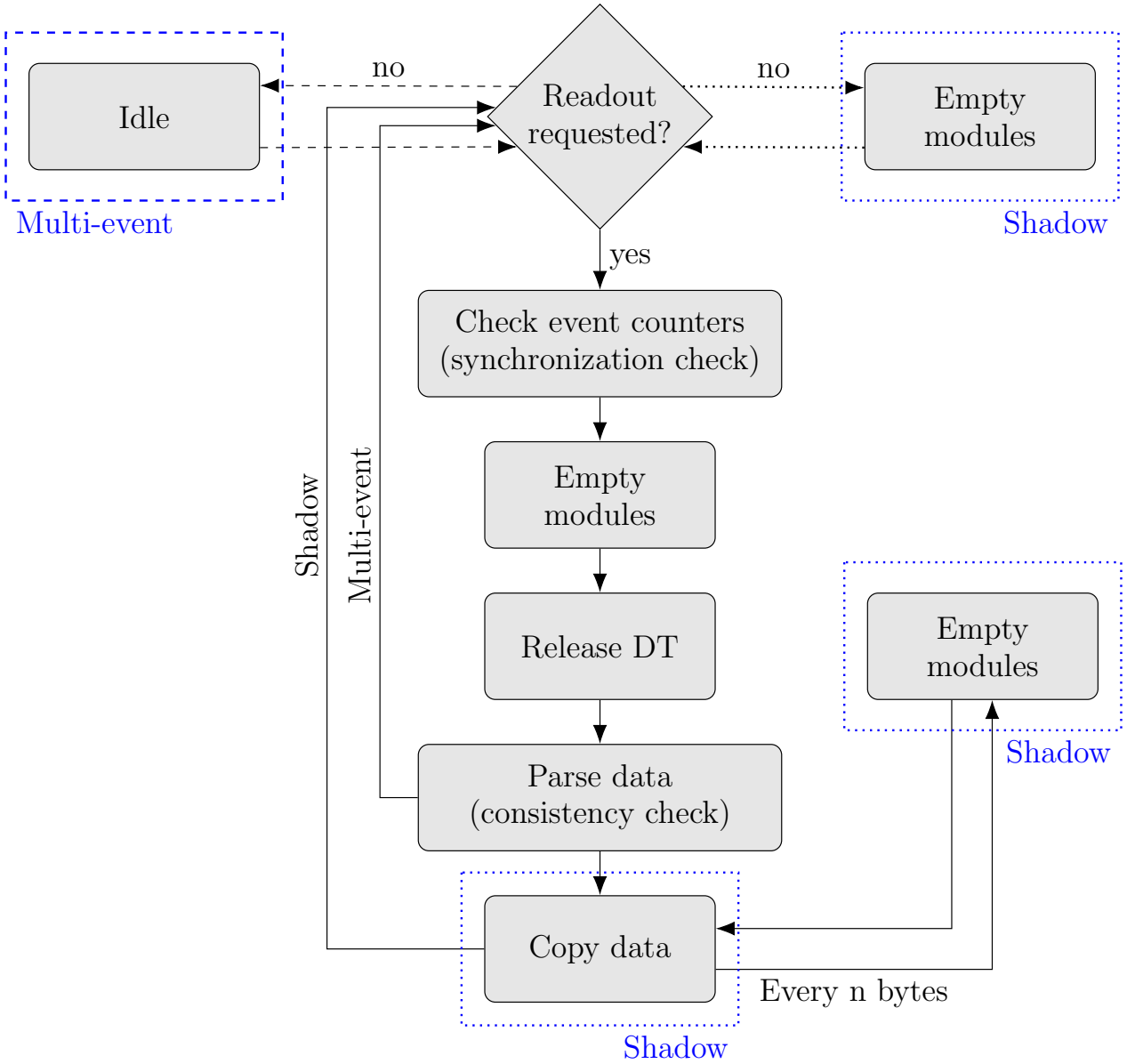
CES RIO4 $\sim$ **0.5us/word**

Readout time $\gg$ digitization time

Bottleneck II

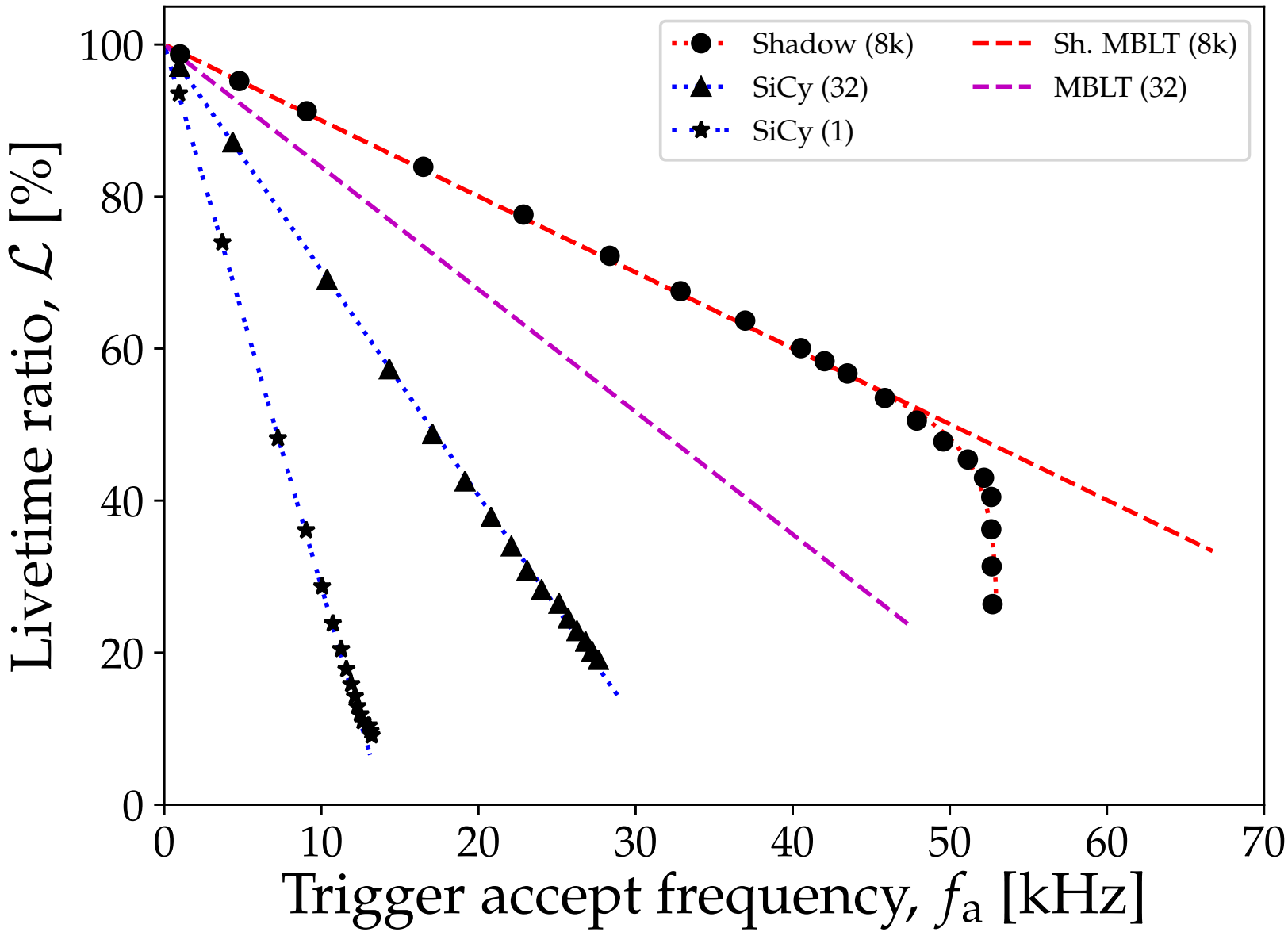


Software


Idle
Multi-event
no
Readout requested?
no
Empty modules
Shadow
yes
Check event counters (synchronization check)
Empty modules
Release DT
Parse data (consistency check)
Copy data
Shadow
Multi-event
Empty modules
Shadow
Every n bytes
Shadow

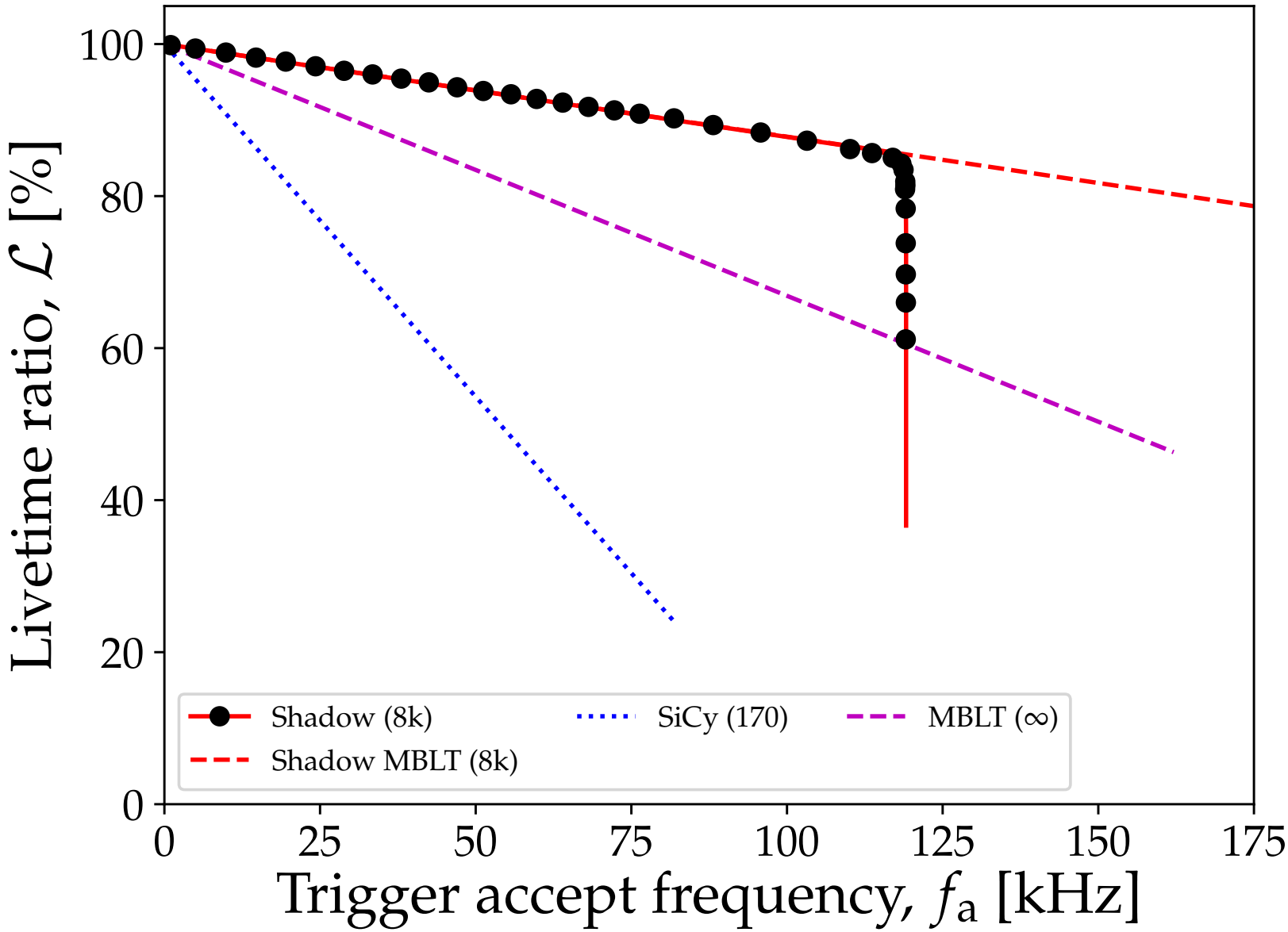
Benchmark CAEN v785

33 words per event



Benchmark Mesytec MADC32

17 words per event



Conclusion

Optimized readout software

$\Downarrow$

Factor ≥ 2 higher throughput.

Details $\rightarrow$ arXiv:1810.03574

NUSTAR signal exchange

In collaboration with:

H. T. Johansson (Chalmers), A. Heinz (Chalmers)

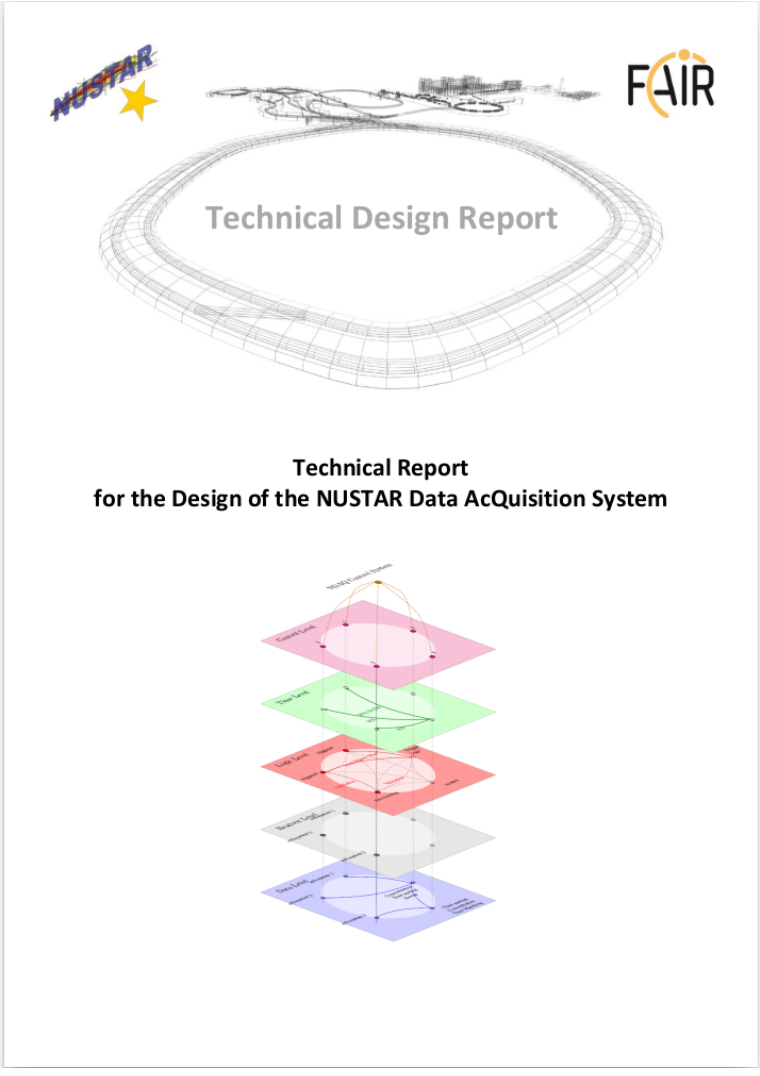
Backbone

- Triggers (from all detectors)
- MASTER START (to all detectors)
- BUSY (from all detectors)

Challenge

- NUSTAR consist of N detectors
- Not all N detectors are used for all experiments
- Requires recabling (error prone)
- Ground loops! (already inside caves)
- Large distances within same experiment (SuperFRS)

Solution

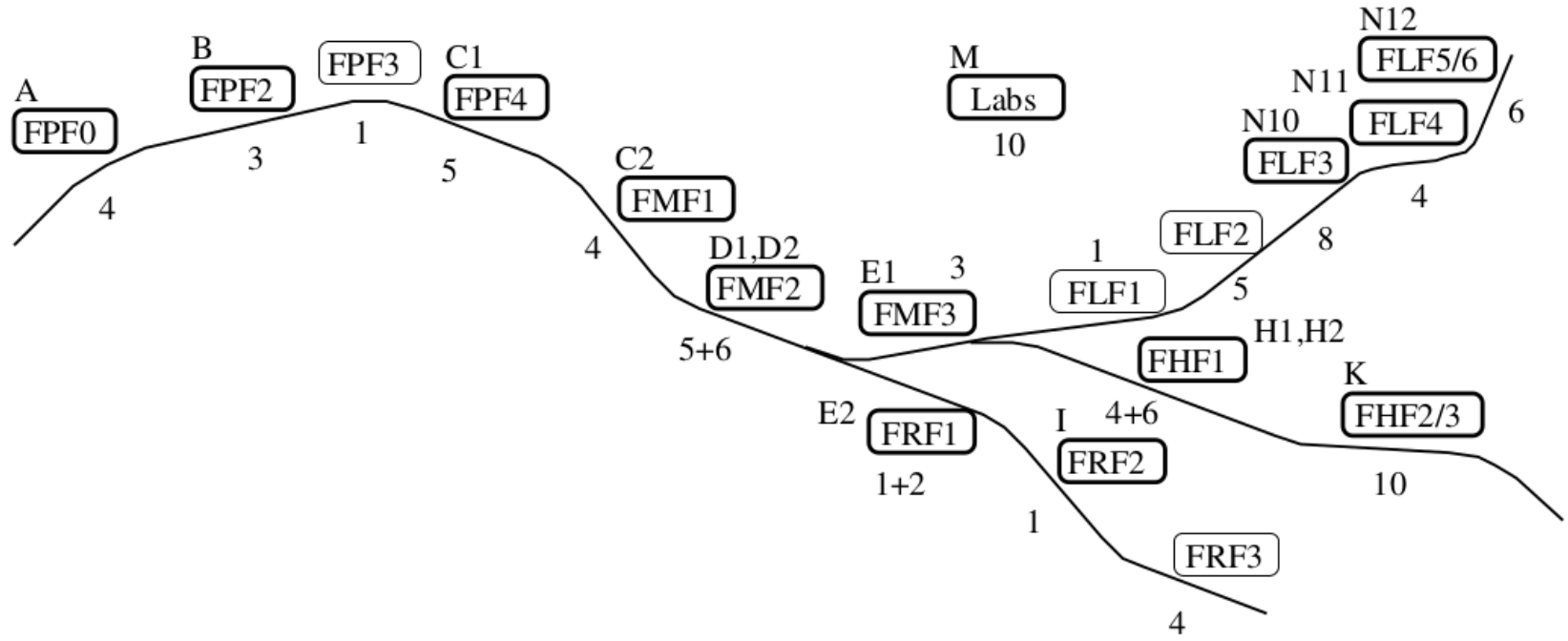


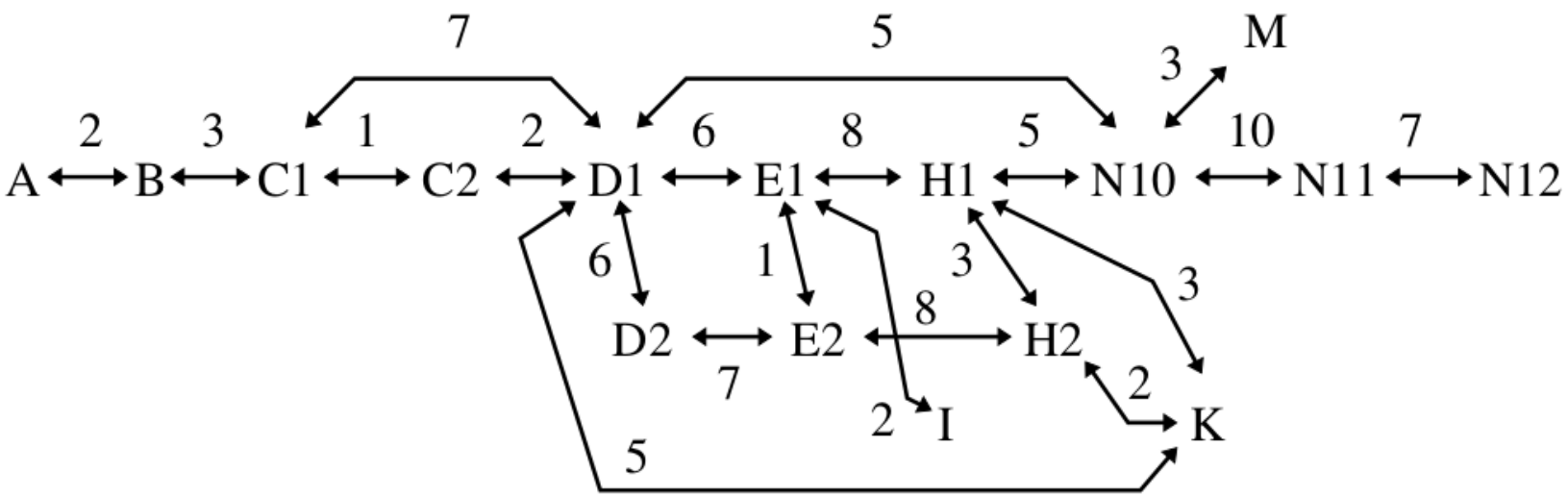
https://edms.cern.ch/document/2024803

Signal Exchange Network

- Fixed infrastructure
- Software defined routing
- Entirely optical
- Builds upon VULOM + TRLO II experience
- Swedish inkind

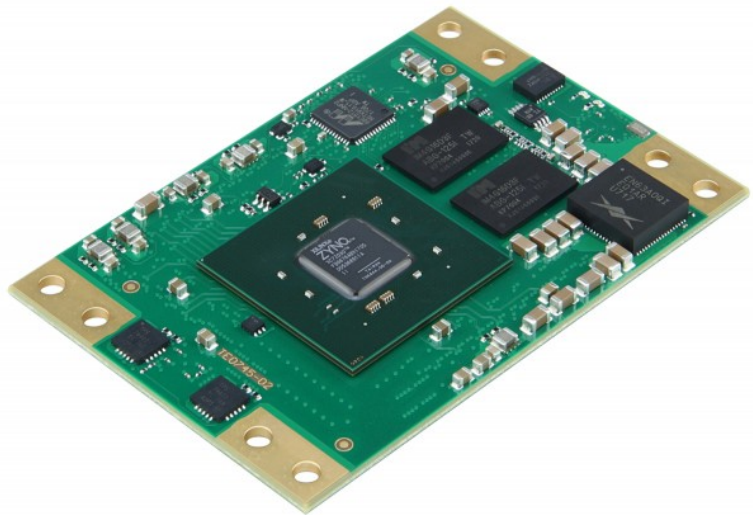
Network


A
FPF0
4
B
FPF2
3
FPF3
1
C1
FPF4
5
C2
FMF1
4
D1,D2
FMF2
5+6
E1
3
FMF3
M
Labs
10
1
FLF1
FLF2
5
8
N10
FLF3
N11
FLF4
4
N12
FLF5/6
6
H1,H2
FHF1
K
FHF2/3
10
E2
FRF1
1+2
I
4+6
FRF2
1
FRF3
4

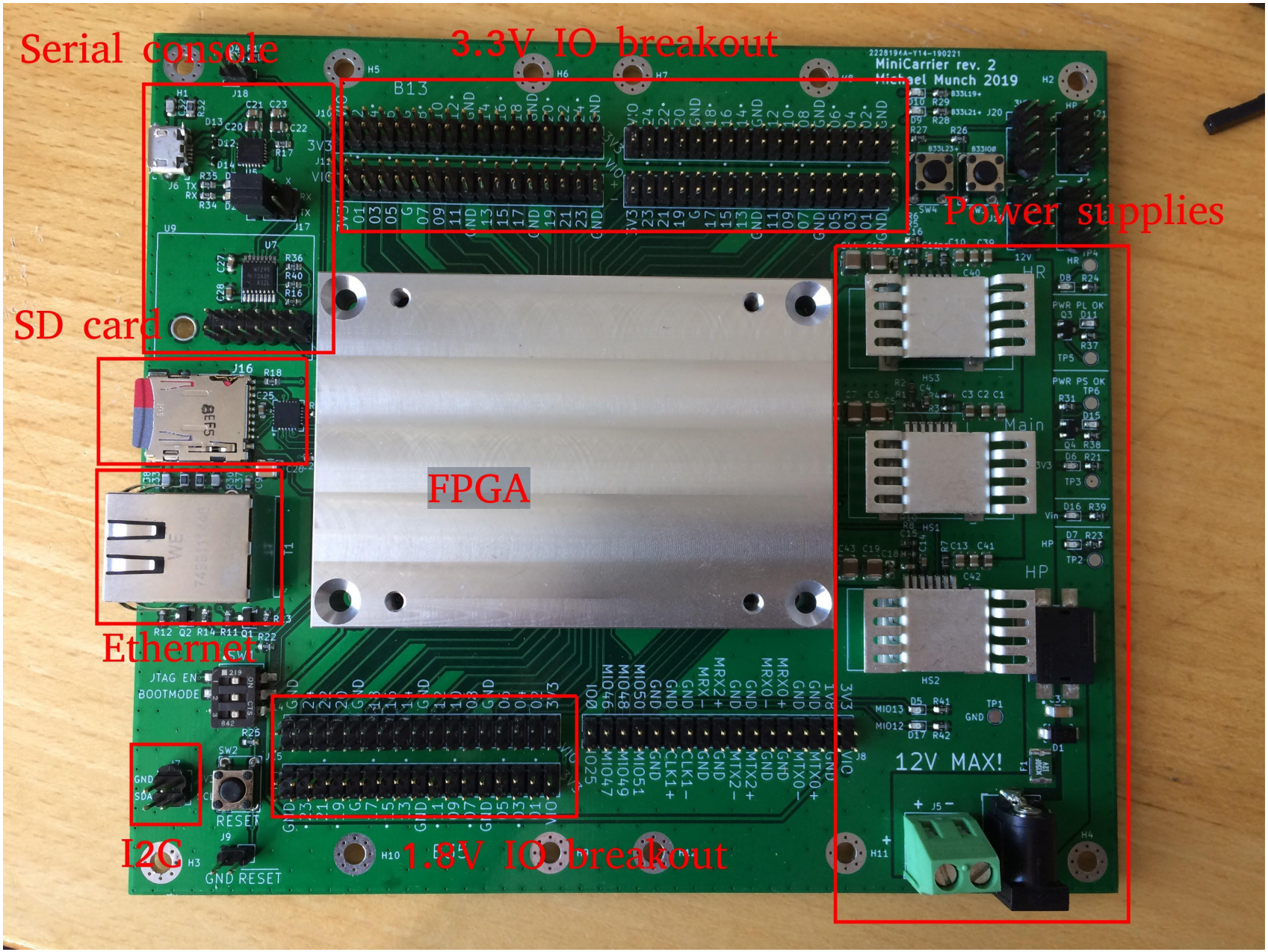

A
B
C1
C2
D1
E1
H1
N10
N11
N12
M
D2
E2
H2
I
K
2
3
1
2
6
8
5
10
7
7
5
3
6
1
3
8
3
7
2
2
5

Work horse

- Xilinx ZynQ SoC
- Dual ARM Cortex-A9
- Kintex FPGA
- 1GB RAM
- 250 FPGA IO
- 1Gbit ethernet

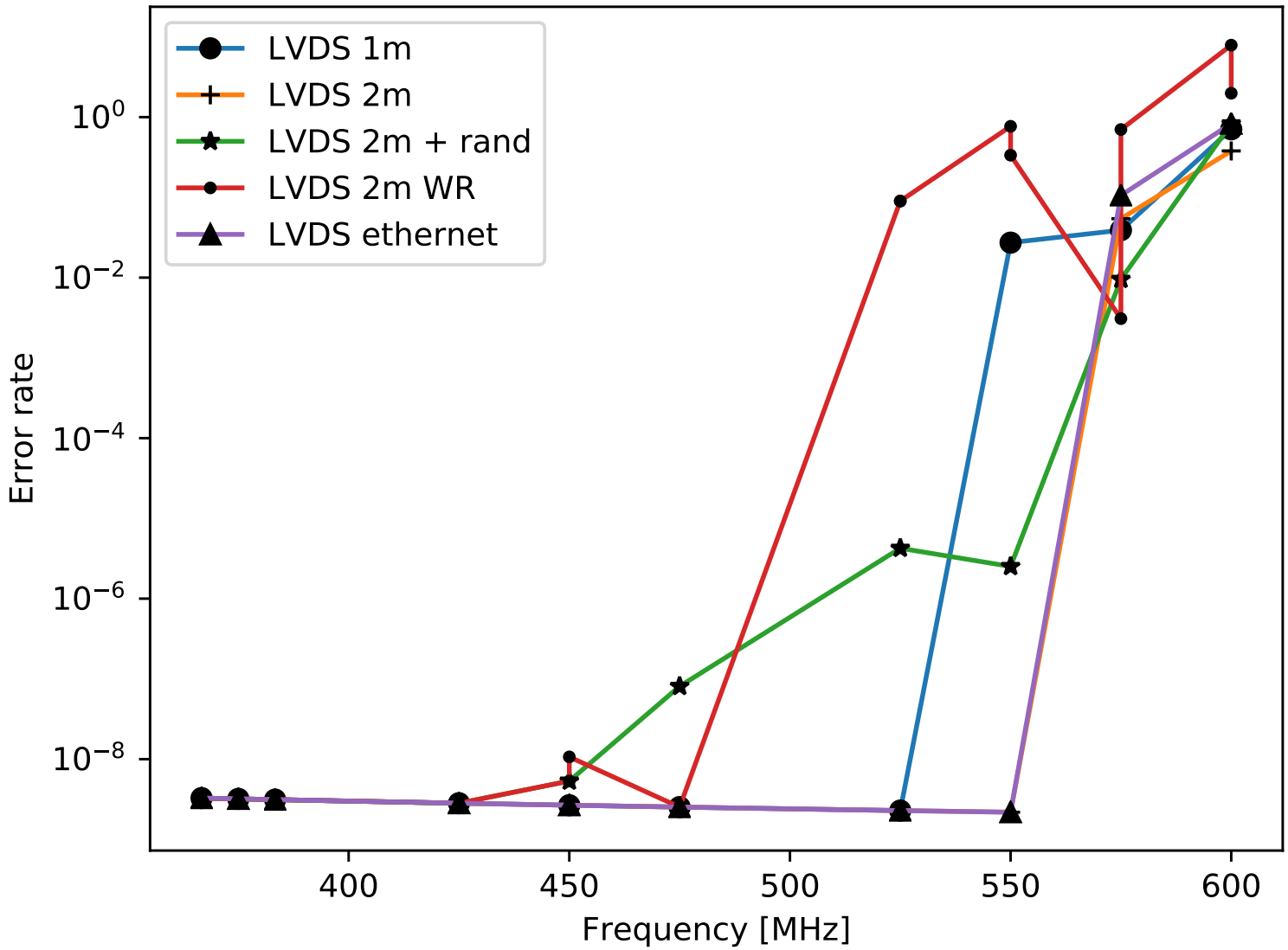


Demonstrator I



Demonstrator II

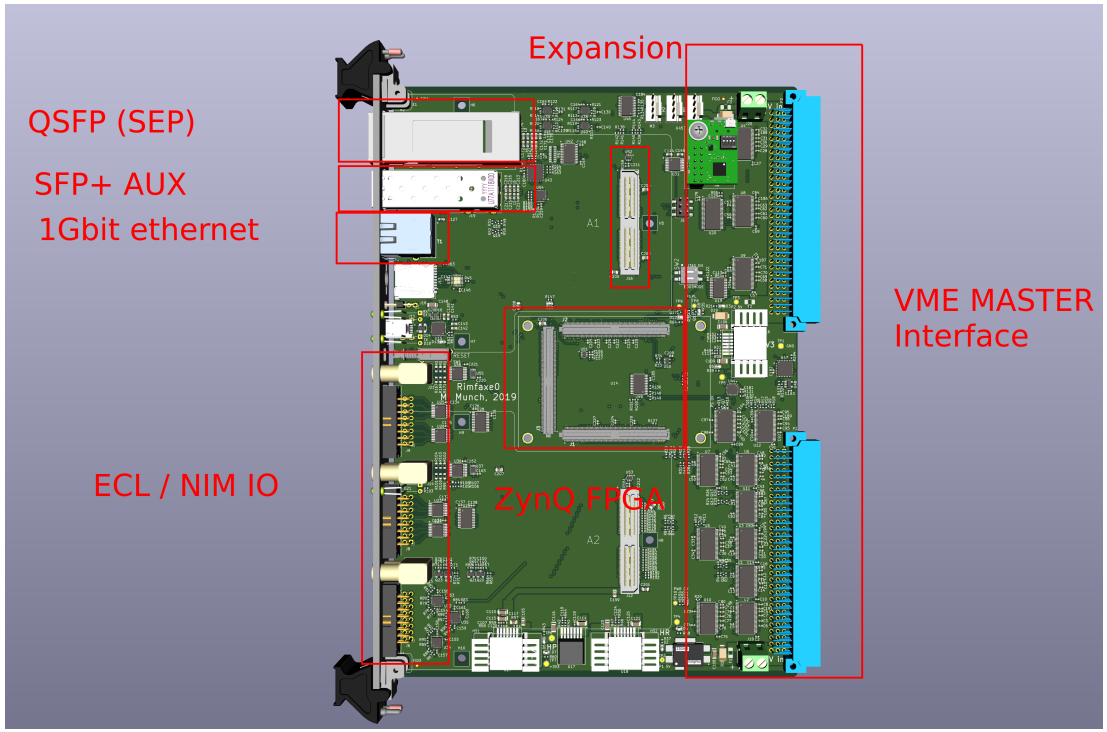
Possible to send serially with $\geq 400\,\mathrm{MHz}$



VME module (Rimfaxe)

Interface from detector to SEP network
Rimfaxe $\approx$ RIO4 + VULOM4
Work in progress

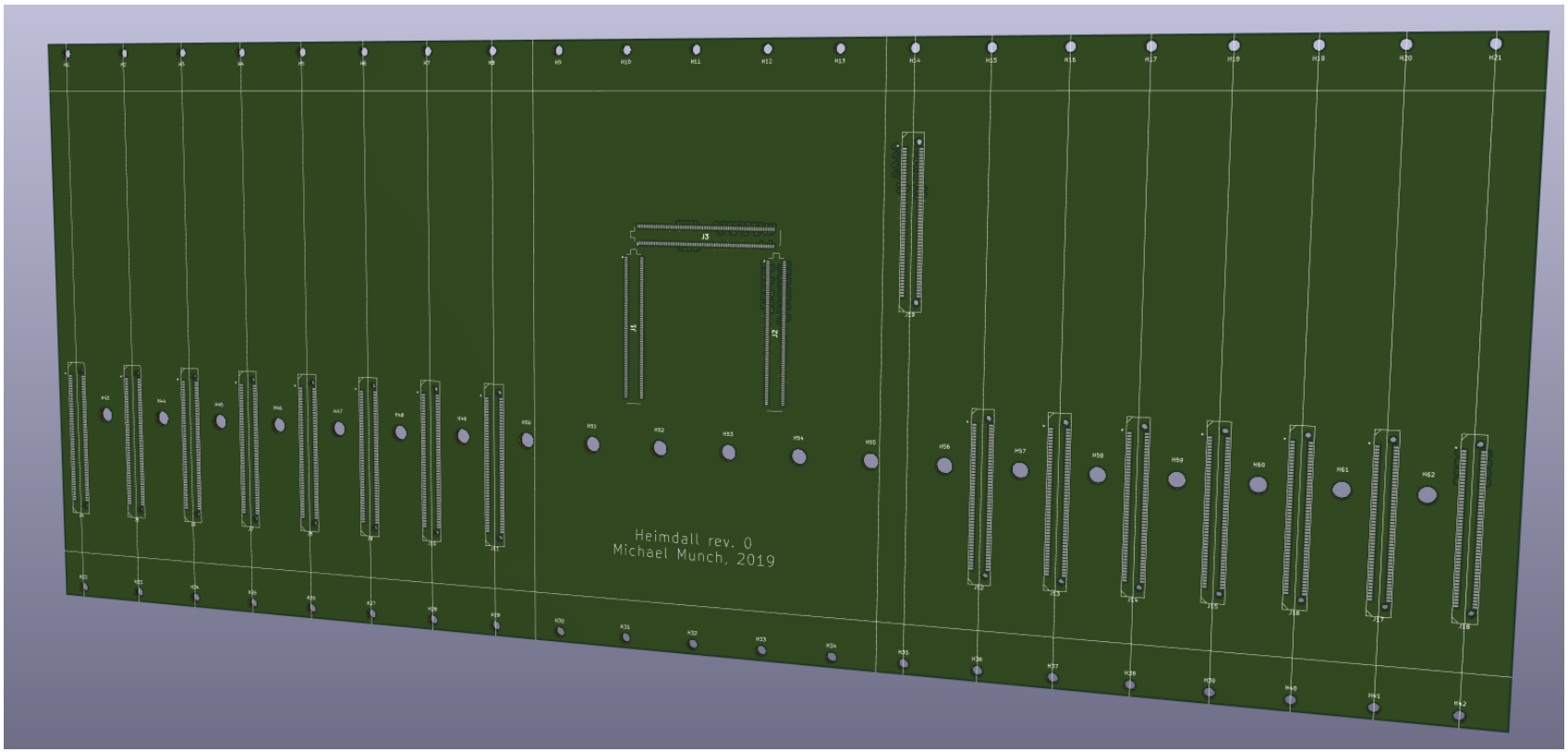
- VME master
- 1GBit ethernet
- QSFP (SEPNET)
- SFP+
- 24 ECL (IN/OUT)
- 6 NIM (IN/OUT)
- 72 IO expansion



SEP crate (Heimdall)

HW design in progress

- Relay in the SEP network
- 19" 4U crate.
- 8 IO per card (1 QSFP)
- 15 cards

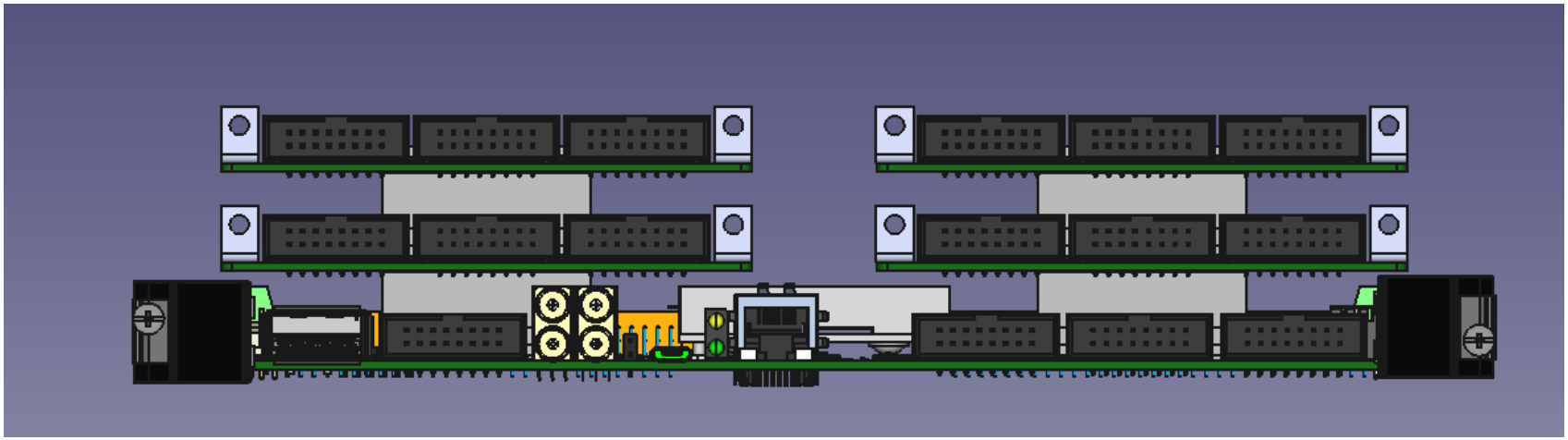


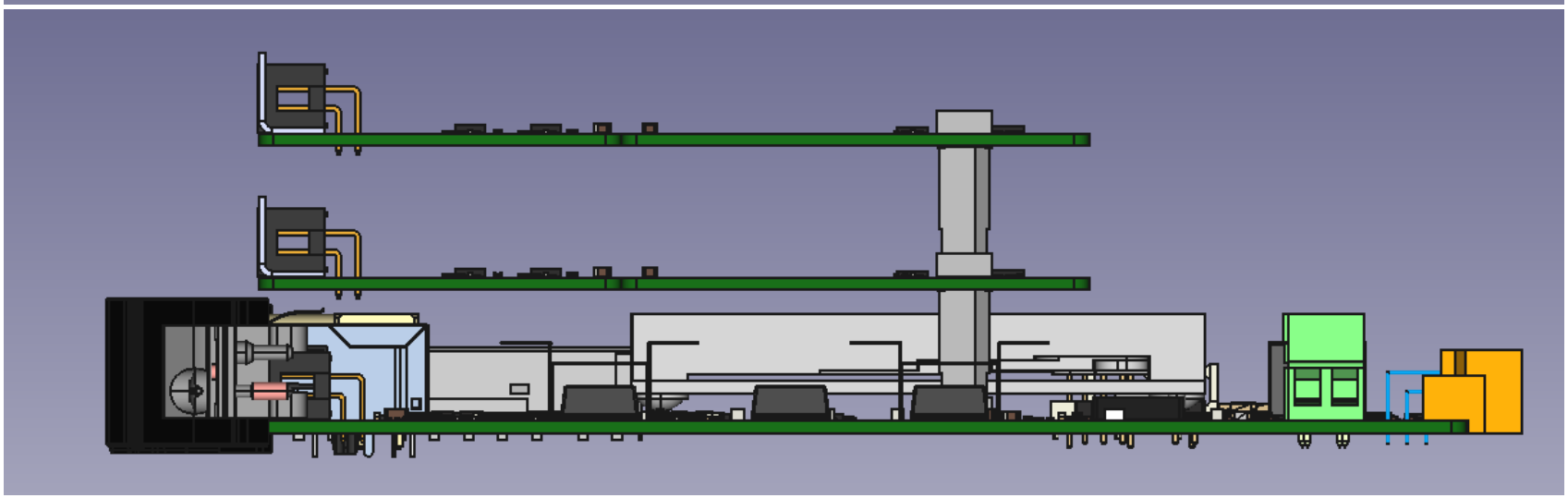
Status

- Successfull demonstrator
- Possible to send serially with $\geq 400\,\mathrm{MHz}$.
- First prototype of VME module in 2 month
- HW design for backplane in progress

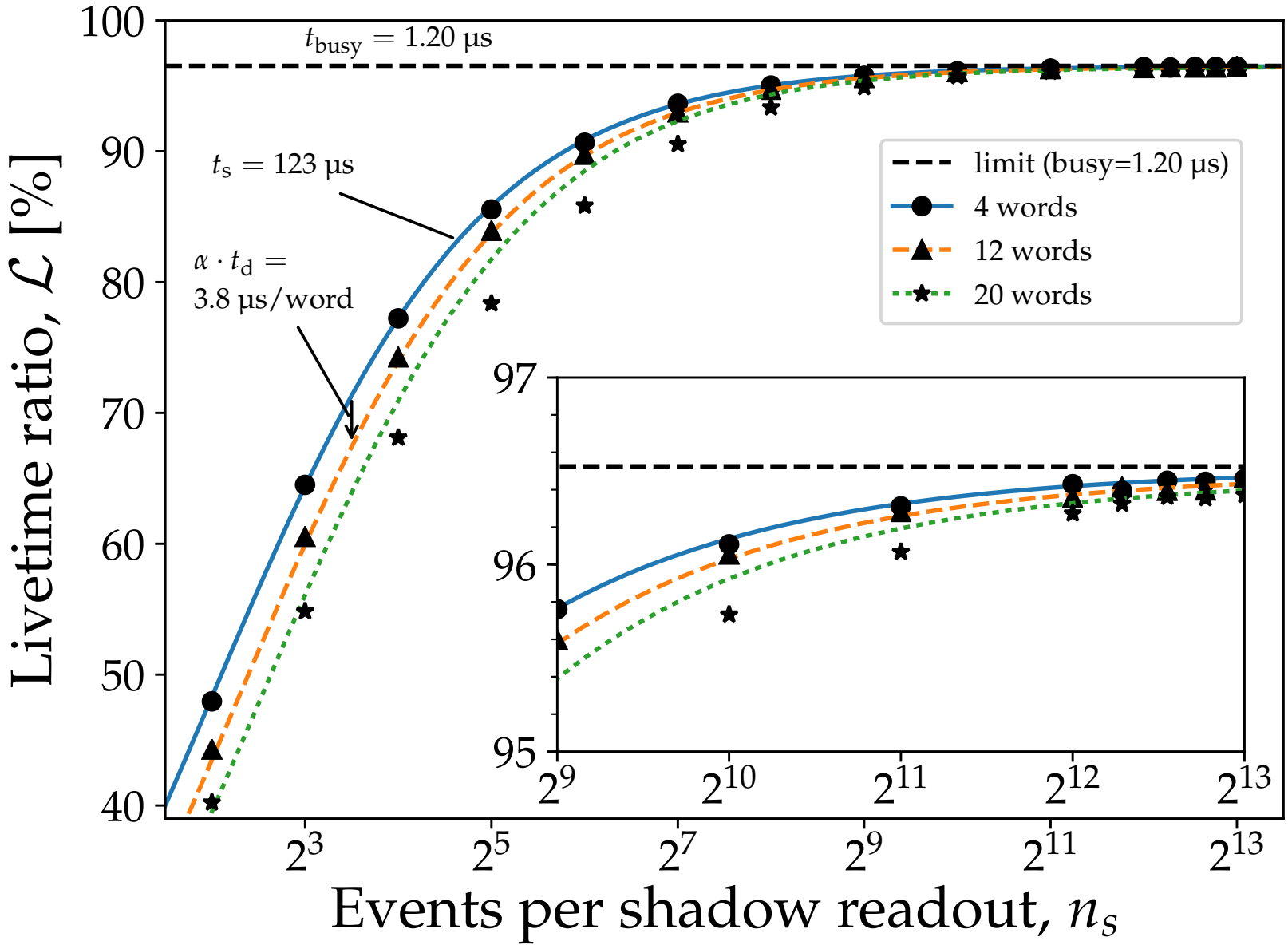
Bonus

Rimfaxe B2B





Convergence



Nomenclature

- Livetime, LT : Time where triggers are accepted
- Deadtime, DT, Δt : Time where triggers are *not* accepted
- Livetime fraction, $\mathcal{L}$: Fraction of events accepted
- Deadtime fraction, $\mathcal{D}$: Fraction of events rejected
- Trigger request frequency, f_r : Frequency of total triggers
- Trigger accept frequency, f_a : Frequency of accepted triggers

$$\mathcal{D} + \mathcal{L} = 1$$

$$\mathcal{L} = \frac{1}{1 + f_r \Delta t}$$