# Minutes of the STT Readout Meeting (SRN) on November 28th, 2018

Participants: Tassos Belias, Andreas Erven, Holger Flemming, Marek Idzik, Ljuba Jokhovets Gregorz Korcyl, Pawel Kulessa, Krzysztof Pysz, Piotr Salabura, Lars Schmitt, Valeriy Serdyuk, Peter Wintz.

Meeting web page with program and presentation slide: https://indico.gsi.de/event/8139

Topics of the meeting were the discussion of the recent STT readout decision taken by the PANDA Collaboration Board, the readout meeting continuation and status reports of the PASTTREC-ASIC/TRB3 system and the ADC-based readout.

First, Peter informed about the decision of the PANDA Collaboration Board to use the PASTTREC-ASIC/TRB3-TDC system as readout, both for the STT and FT in the Day-1 start setup of PANDA. It was stated that for the later PANDA experiment phase with full luminosity, an upgrade of the STT readout system is foreseen with higher bandwidth of the data links. The ASIC/TRB3 components will be then transferred to the FT5/6 stations, which will be not present in the Day-1 setup. The ADC system with full waveform sampling is then a serious option for the upgraded STT readout, in particular in case of better PID results, which have to be demonstrated by the current ADC system setup. Piotr remarked, that also an upgraded better TDC/TRB solution is not excluded for the later experiment phase. Peter showed then a brief status overview of both readout systems and the final testbeam results of spatial resolution and separation power for PID for the ASIC/TRB3 system.

Next, Marek reported about the PASTTREC-ASIC status and important news. The chip production is very time critical because the ASIC AMS 350nm technology expires soon, maybe end 2019. This requires to order the final and for the future sufficient number of chips for STT and FT in the first half of 2019. In total about 5000 ASICs are planned to order as an AMS 350 engineering run. Cost estimate is roughly 120 kEUR. Piotr reported that also the MDC group at HADES plans to order a similar number of PASTTREC chips for their readout upgrade. The PASTTREC design was verified in various test systems in the past years. It was agreed that the AMS engineering production run should be submitted as soon as possible since there are only few certain production run times per year. Aim is to place the ASIC order in January if budget is available.

Andreas reported about the ADC system status. The hardware design of the ADC/FPGA board and amplifier board was tested by the April 2018 beam time and verified. Only a minor change at the amplifier board (connector, grounding) is necessary. It was re-stated that the next plan is to set up a larger demonstrator system with 300-400 channels and with a system controller for board readout and synchronization via the backplane. At current, the data processing concept in the FPGA (firmware) is renewed and in progress. The next step will be cosmic runs and later in-beam tests to measure the separation power for PID. Pawel asked about a next beamtime. It was decided that first the ADC system has to be set up and pre-tested with cosmics before submitting a dedicated beam time request.

The series of STT readout meetings was initiated in January 2017 for the readout decision process. It was agreed to continue with these meetings on a regular, roughly one- or two-monthly basis.