MVD SPD

Sezione di Torino

Status report
of the readout architecture design for the silicon pixel detectors

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Outline

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- "Hiccups" in the technology and CAD updates
- ToPiX version 3 architecture
- Data transmission
- Power supplies – news from TWEPP 2009
- Clock frequency issues

"Hiccups"

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- Technology : from LM to DM flavour
  - → *LM metal layers : 6 thin + 2 thick*
  - → *DM metal layers : 3 thin + 2 thick + 3 RF*
  - → *more analog-oriented : problems in digital routing*
- CAD tools : Cadence has changed its database format : from CDB (IC v. 5.1) to OA (IC v. 6.1)
  - → *the translation tool has several problems...*
- Standard cells and pad libraries + design flow :
  - → *Old tools from ARM and Manhattan Routing*
  - → *New tools from IBM and Cadence*

ToPiX specs

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- Pixel size : 100 μm × 100 μm
- Chip active area : 11.4 mm × 11.6 mm (116 rows, 110 cols)
- dE/dx : Time over Threshold, up to 100 fC
- Analog noise floor : < 32 aC (200 e^-)
- System clock frequency : 155÷160 MHz
- Max event and data rates : 12.3 MHz/cm^2 - 815 Mb/s/chip *(?)*
- Power consumption : < 500 mW/cm^2
- Total Ionizing Dose : < 100 kGy
- Equivalent neutron fluence : < 5·10^{14} 1MeV n_{EQ}/cm^2

ToPiX v2

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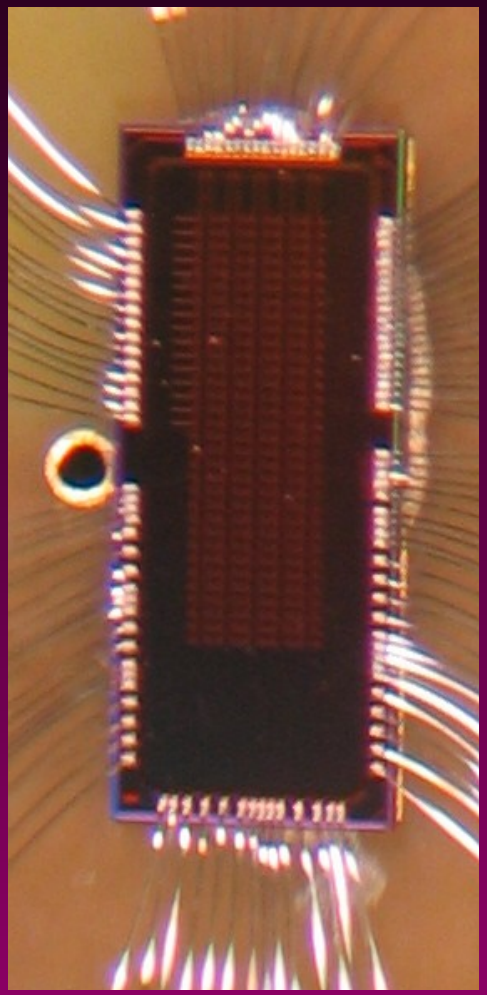

- Full pixel cell (analogue + digital)
- Two folded columns with 128 cells
- Two columns with 32 cells
- 5x2 mm^2 die area
- CMOS 0.13 µm LM technology
- Working frequency : 50 MHz
- Dice-based SEU resistant FFs
- Tests :
  - → test bench
  - → with a sensor and a radiation source
  - → TID and SEU

ToPiX v3

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New prototype in 0.13 μm under development – main changes :

- BEOL option : DM
- Standard cells library : IBM
- Clock frequency : 155÷160 MHz
- SEU protection : triple redundancy
- More compact analog part

LM vs DM

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	LM	*DM*
Analogue features	☹	☺
Routing density	☺	☹
Power distribution	☹	☺

LM vs DM routing

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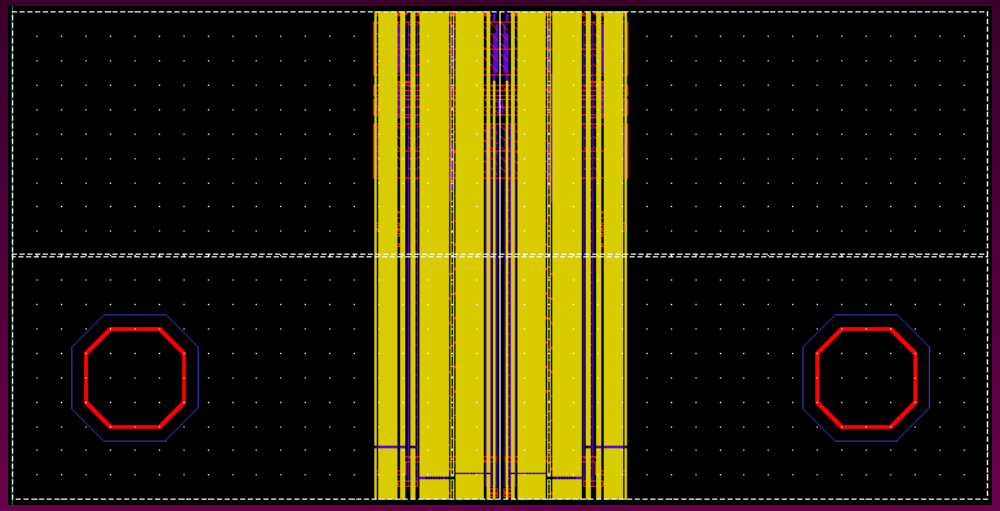
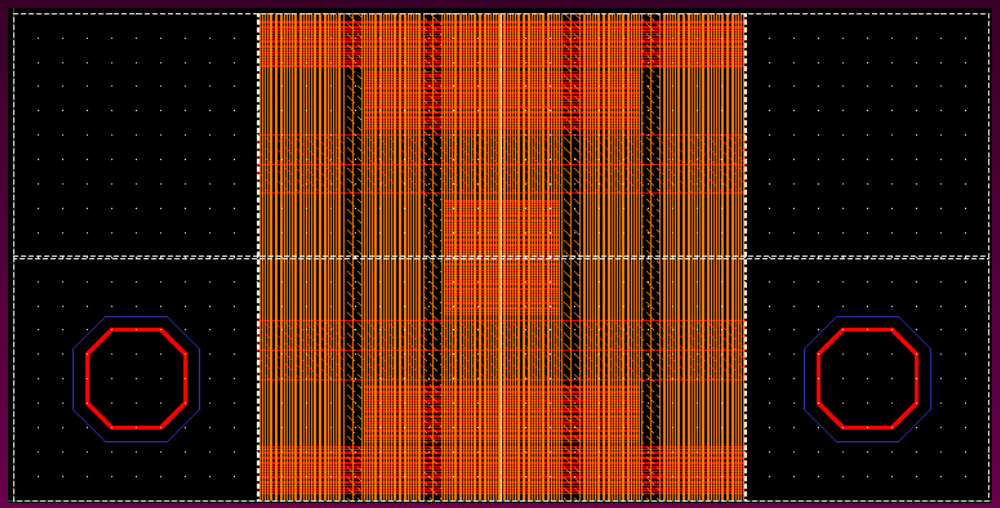
LM pixel buses



Bus routed on M4 and M6
Minimum bus pitch 0.4 µm
Wire resistance : 64 Ω/□
1 readout bus per pixel column

DM pixel buses



Bus routed on MG only
Minimum bus pitch 0.8 µm
Wire resistance : 37 Ω/□
1 readout bus every 2 pixel column

System aspects

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- Time resolution : 1.8 ns r.m.s. @ 160 MHz
- Pixel readout time : 8 clock cycles (50 ns)
- ToT gain : 62.5 ns/fC
- Pixel dead time @ 1.3 fC : ~90 ns
- Pixel dead time @ 100 fC : ~6 μs
- Chip active area : 1.32 cm^2
- Bits per event : 50

Event loss probability

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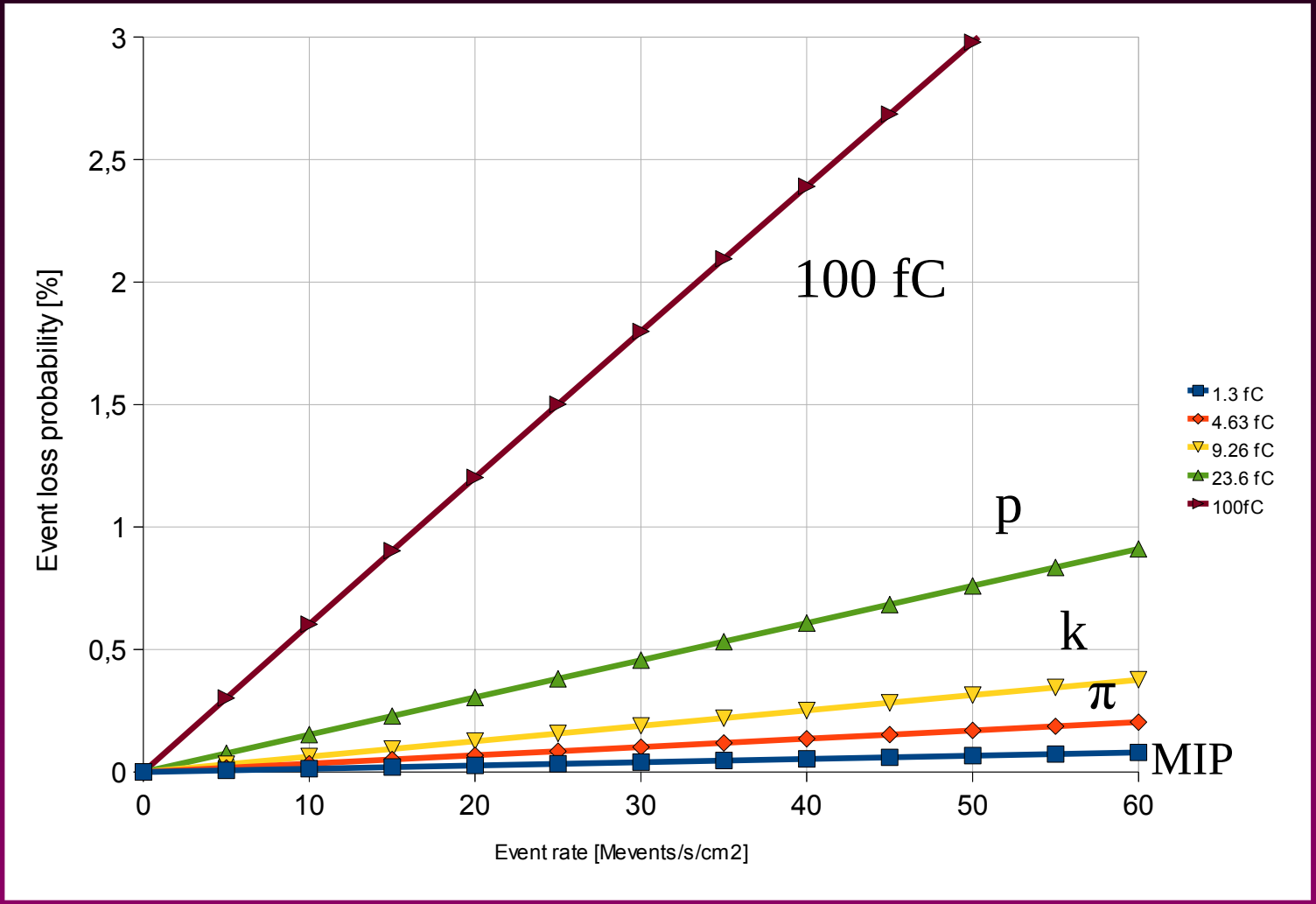

Data transmission

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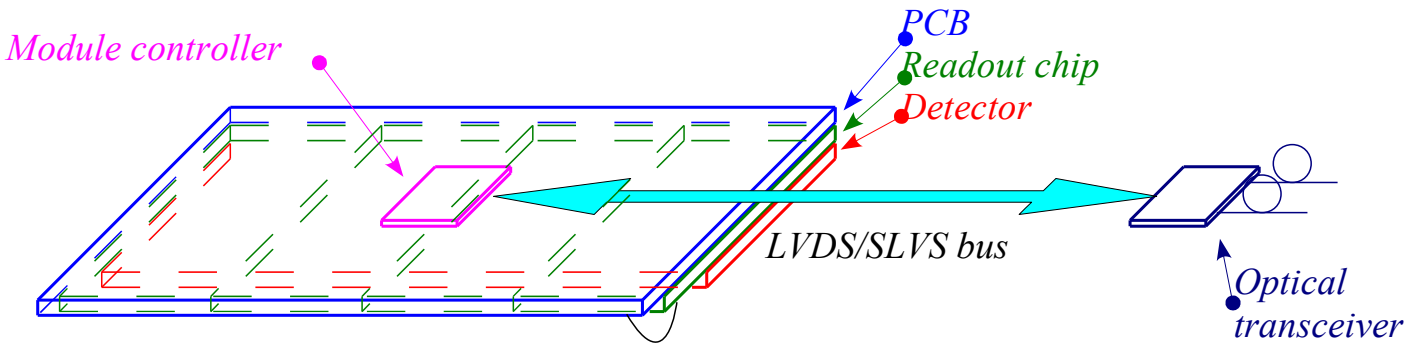
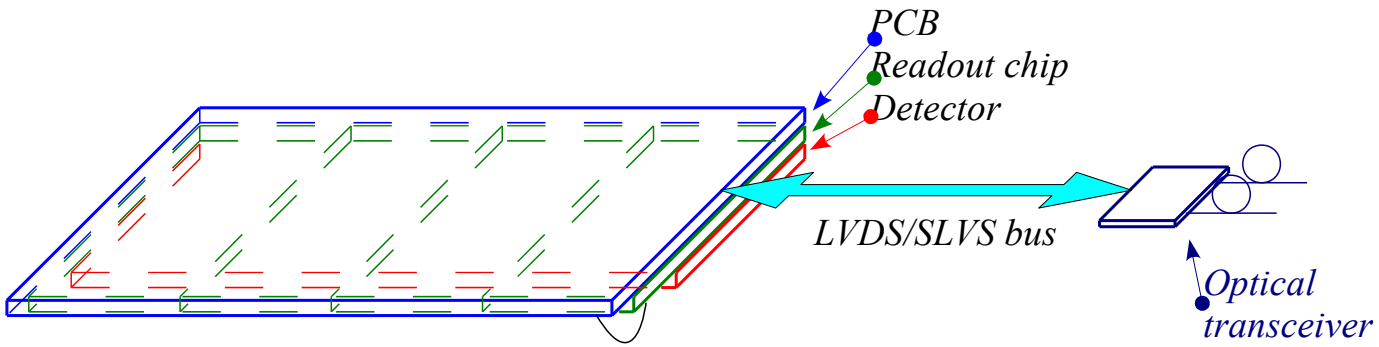


Option 1



Option 2

Electrical link

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E-link

- Under development for the GBT interface
- Up to 320 Mbit/s
- Direct connection to the GBT
- More cables, less design work

Custom design

- Target : 1 Gbit/s
- Common development : PANDA MVD and NA62 GTK
- More design work, less cables

Data rate *vs* event rate

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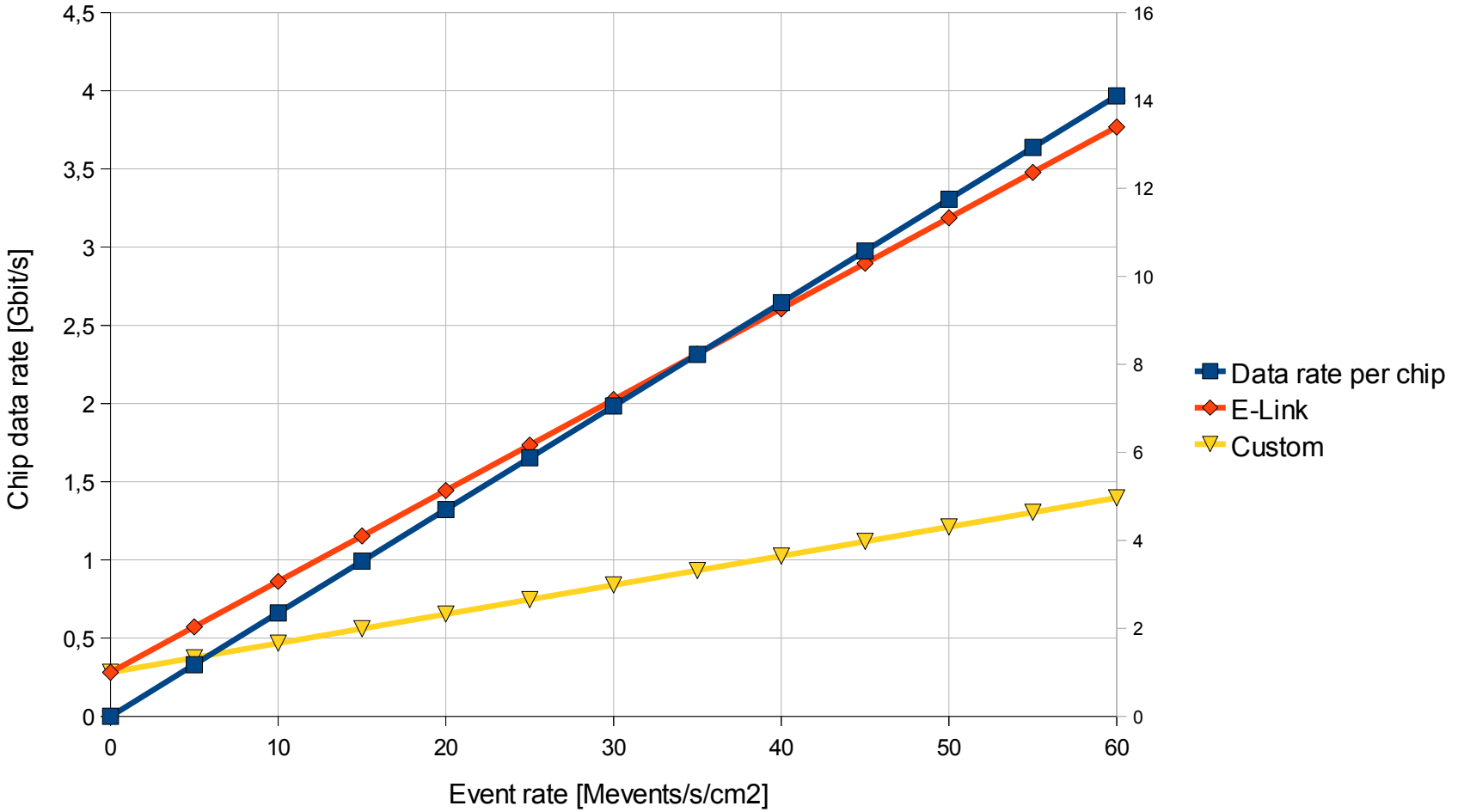

Power supply

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- Deep submicron technologies requires lower voltages (0.35 μm → 3.3 V, 0.25 μm → 2.5 V, 0.13 μm → 1.2 V)
- Power saving (~same current, lower voltage) *but...*
  - ➔ power drop on lines and voltage regulator become critical !
- *500 mW/1.2 V = 420 mA × 3 Ω = 1.26 V → 51% efficiency loss for cabling only*
- Two solutions are under study in the sLHC community :
  - ➔ serial powering
  - ➔ DC-DC converters

Serial powering

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- ATLAS (not official) choice
- N modules are connected in series with a $N \times V_{DD}$ voltage
- Shunt regulator to ensure voltage drop (keep current constant)
- AC connection to the detector and to the DAQ
- Three configurations :
  - W : on chip shunt regulator and shunt transistor
  - M : on chip shunt transistor, external shunt regulator
  - SPi ext : external shunt regulator and shunt transistor

DC-DC converter

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- CMS official 1st choice
- Direct voltage conversion via PWM
- Commonly used in consumer electronics
- High efficiency
- Issues for HEP experiments :
  - noise
  - inductors in magnetic field

MVD power scheme

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- Just started looking at the issue
- No manpower for a custom solution
- Very first feeling : DC-DC looks better
- PANDA and sLHC timeschedule are similar

  → *we can wait and see who will be the winner...*

MVD pixel requirements

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Basic considerations :

- in a triggerless environment SPDs generate a lot of data (currently 50 bits/hit : address+time reference+ToT)
  - → to fit space and material requirements, we need electrical to optical conversion as close as possible to the detector
- electronics has to be radiation hard
  - → no COTS components can be used
  - → looking for solution in the HEP community, expecially at development for LHC-sLHC

Clock issue

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- ToPiX is (almost) completely synchronous
  - most performances are defined by the clock (time resolution, dead time, transmission bandwidth, ToT gain)
  - we do need to freeze the clock frequency (at least ±10%)
- LHC electronics is based on a 40 MHz clock
  - in principle many ASICs can work at different frequencies but it is not guarantee (ref. QPLL)
  - for pixel it would be safer to for a $2^N \times 40$ MHz clock
  - any other PANDA detectors plan to use LHC electronics ?

GBT project

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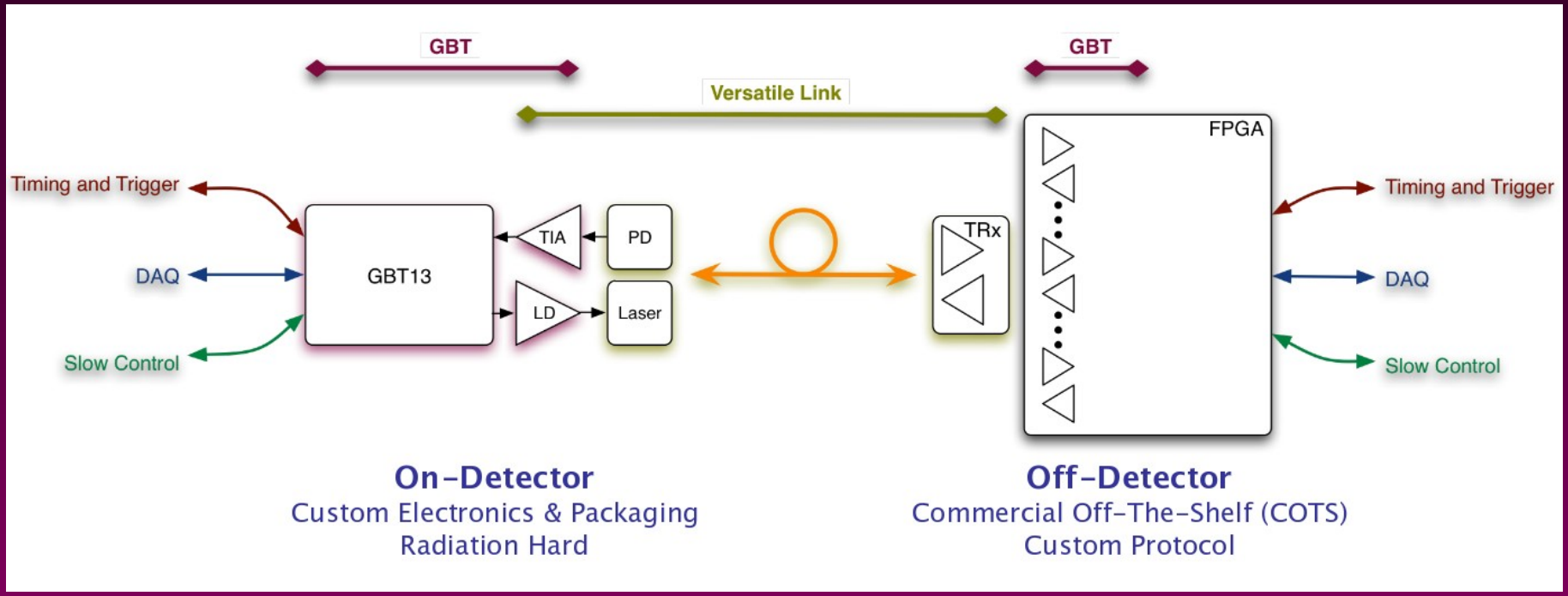

GBT chipset

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Radiation tolerant chipset :

- GBTIA : Transimpedance optical receiver
- GBLD : Laser driver
- GBTx : Data and Timing Transceiver
- GBT-SCA : Slow control ASIC

Target Applications :

- Data readout
- TTC
- Slow control and monitoring links

Supports :

- Bidirectional data transmission
- Bandwidth :
  - → Line rate : 4.8 Gb/s
  - → Effective : 3.36 Gb/s

Radiation Tolerance :

- Total dose
- Single Event Upset

GBLD

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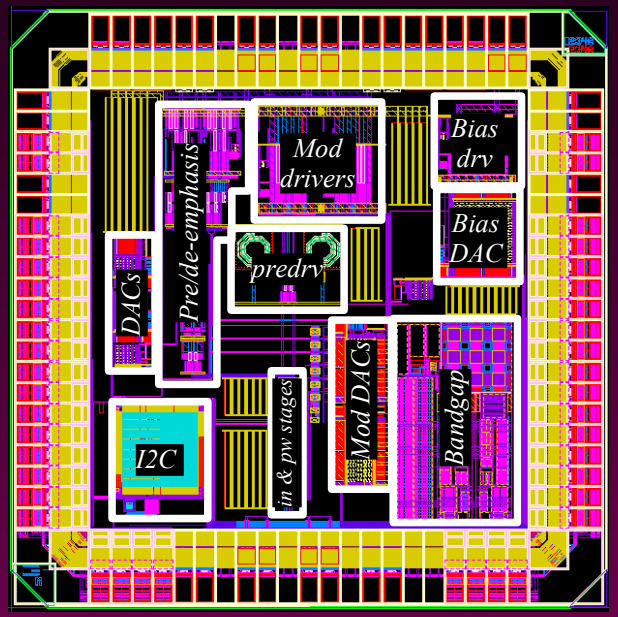
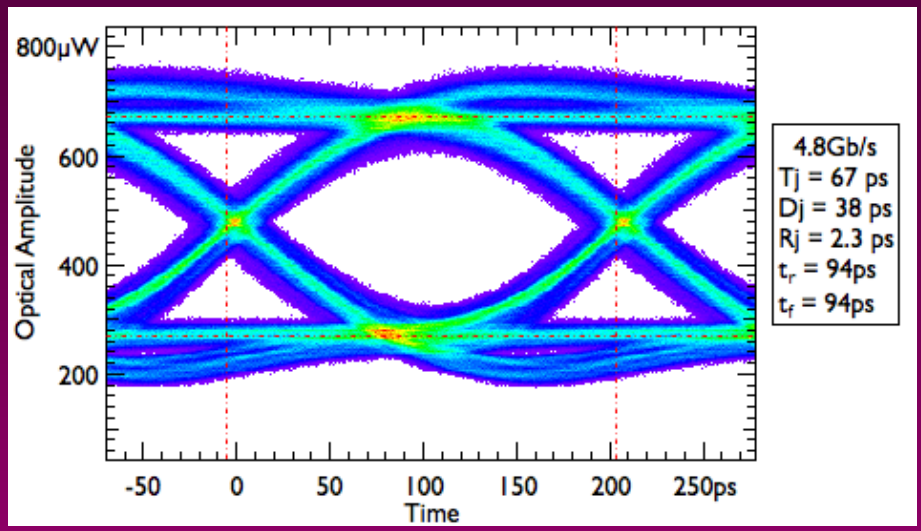


- GBLD : 5 Gb/s laser driver
- Modulation current : 2÷24 mA
- Bias current : 2÷43 mA
- Pre-emphasis/de-emphasis current : 0÷12 mA
- I2C digital control

Torino contribution to the GBT project



Conclusions

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- Some “hiccups” in the technology for ToPiX
- Design of the ToPiX v3 started
  - *still under the sword of Damocles of the clock frequency...*
- Ongoing studies on the full architecture :
  - electrical data transmission
  - optical conversion and DAQ interface
  - power supply
- clock issue