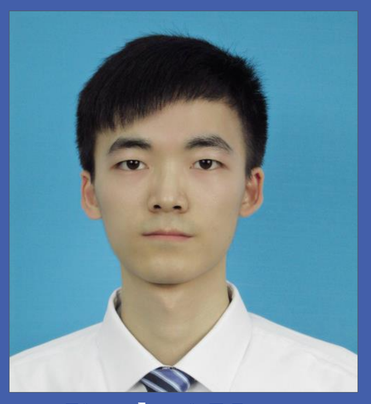
Readout method based on PCIe over optical fiber for CBM-TOF super module quality evaluation

Jianhui Yuan[1,2], Ping Cao[1,2*], Xiru Huang[1,3], Chao Li[1,3], Qi An[1,2]

[1]State Key Laboratory of Particle Detection and Electronics, University of Science and Technology of China, Hefei, 230026, China
[2]School of Nuclear Science and Technology, University of Science and Technology of China, Hefei, 230026, China
[3]Department of Modern Physics, University of Science and Technology of China, Hefei, 230026, China



Jianhui Yuan

1. Introduction

The Compressed Baryonic Matter experiment (CBM) is one of the core projects of the future accelerator facility FAIR in Darmstadt. It aims at investigating the QCD phase diagram at high net baryon densities and moderate temperatures using high-energy nucleus collisions. Time of Flight (TOF) system, one of the detectors of the CBM experiment, is designed to identify hadrons. The CBM-TOF is composed of super modules containing high performance Multi-gap Resistive Plate Chambers (MRPCs). During the mass production, the quality evaluation of super modules encounters the challenge of reading data from a super module at a speed of about 6 Gbps. Traditional VME or PXI technique is limited by the bandwidth of the crate backplane.

A readout method based on PCIe over optical fiber is proposed for CBM-TOF super module quality evaluation. A PCIe based readout architecture is explained in section 2. The design of PCIe switch module (PSM) is described in section 3.

2. System Architecture

Signals from MRPCs will be converted into digital signals，and be output to front electronics. The structure of the front electronics used in CBM-TOF super module quality evaluation is shown in figure 1.It is composed by these modules:

- a time over threshold feeding baseboard (TFB)
- 10 Time-to-Digital Converter (TDC) cards
- a TDC readout motherboard (TRM)

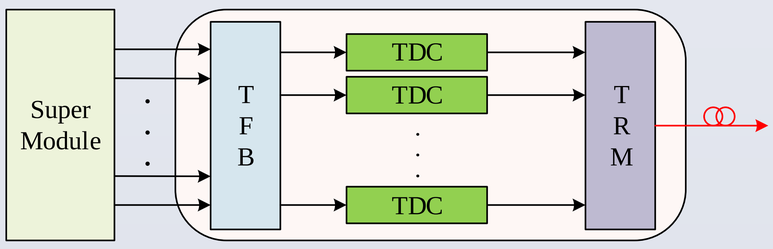


Figure 1. The structure of FEE in quality evaluation

The TFB connects TDC cards with the super module via gold fingers. The TDC cards is responsible for converting time information into digital data. TRM is the readout module for these 10 TDC cards. It receives and merges the data from 10 TDC cards into one data stream. A PCIe interface is implemented in the FPGA on each TRM. The TRM uses this PCIe interface to transmit data over optical fiber to the backend electronics.

In this design, The PCIe switch module (PSM) receives the data from TRM with small form-factor pluggable plus (SFP+) transceivers. The PSM is designed as a PCIe add-in card, so it is convenient to plug a PSM into a motherboard of data acquisition server. The PSM routes data from different TRMs, each of which corresponds to a super module, to the DAQ system though gold fingers.

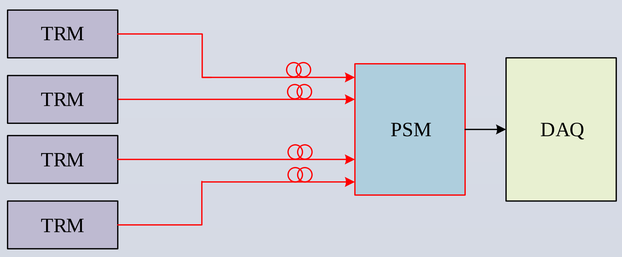


Figure 2. PCIe over optical fiber

This structure of PCIe over optical fiber, as shown in figure 2, provides a high transmission bandwidth. Traditional cables limit the distance between front-end electronics and back-end electronics because that long distance transmission causes high-speed signal attenuation. The deployment of optical links in this method allows long distance transmission and crates an electronic isolation between front-end electronics and back-end electronics.

3. PCIe Switch Module Design

The PSM is responsible for routing data from TRMs to the DAQ system. A PCIe system interconnect switch chip is used for PCIe packet switching. IDT's 89HPES24NT6AG2 is chose as this switch chip.

IDT's 89HPES24NT6AG2 is characterized as the following:

- 24-lane, 6-port PCIe switch with flexible port configuration
- Delivers up to 24 GBps (192 Gbps) of switching capacity
- Integrated SerDes supports 5.0 GT/s Gen2 and 2.5 GT/s Gen1 operation
- Supports dynamic reconfiguration of switch partitions
- Integrated Direct Memory Access (DMA) Controllers

These features allows a high speed PCIe packet switching operation. That makes it easy to gather data from TRMs and to send these data to DAQ. As shown in figure 3, the PSM receives data from TRMs through optical fiber with SFP+ transceivers. To minimize the signal degradation effects such as crosstalk and inter-symbol interference, PCIe repeaters are used in lanes between SFP+ transceivers and the PCIe system interconnect switch chip. The PSM is designed as a PCIe add-in card, so PCIe packets could be transferred to the motherboard of the DAQ system via gold fingers. Extra PCIe lanes are provided with SFP+ for possible optical links from PSM to the DAQ system. Configuration file that the PCIe system interconnect switch chip need is provided by an EEPROM. The PCIe switch chip can also be configured by software runs in the DAQ system.

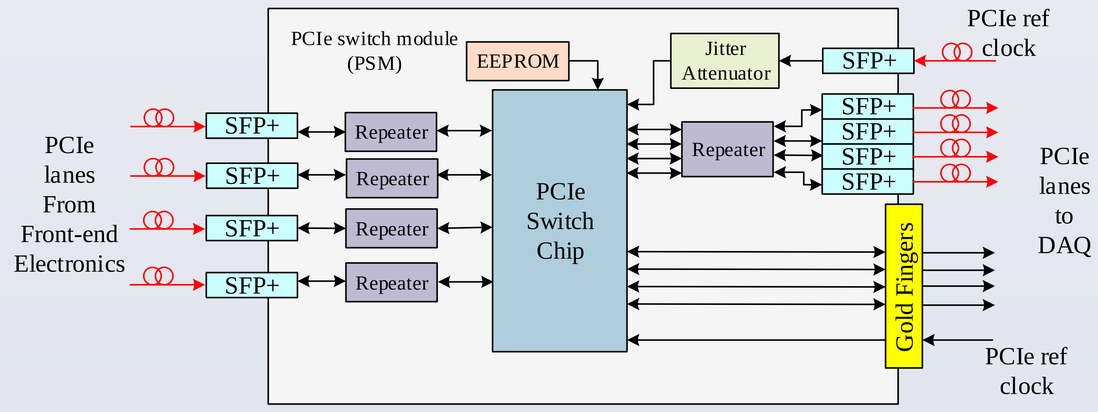


Figure 3. The block diagram of PSM

The PCIe switch chip need two reference clock signals from the same clock source, which will be provided to each port and an on chip PLL. The PLL within each port generates a 5.0 GHz clock used by the SerDes. However, if the root complex in the DAQ server uses Spread Spectrum Clocking (SSC), the corresponding port in PSM also has to use the SSC as reference clock. So, as designed in figure 4, the two upstream ports use the reference clock from root complex, while the others use the reference clock generated on PSM.

The PSM board is shown as figure 5.

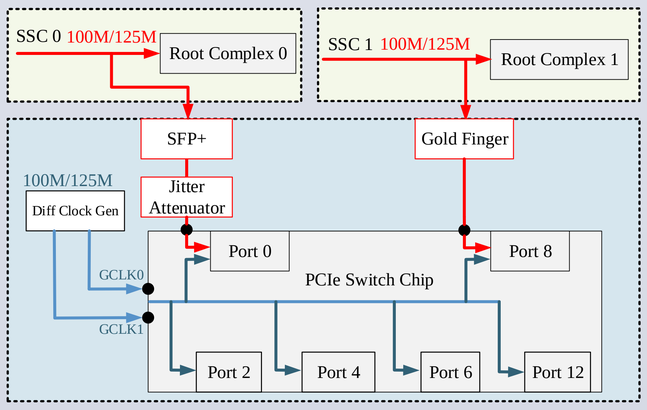


Figure 4. Block diagram of PCIe reference clock

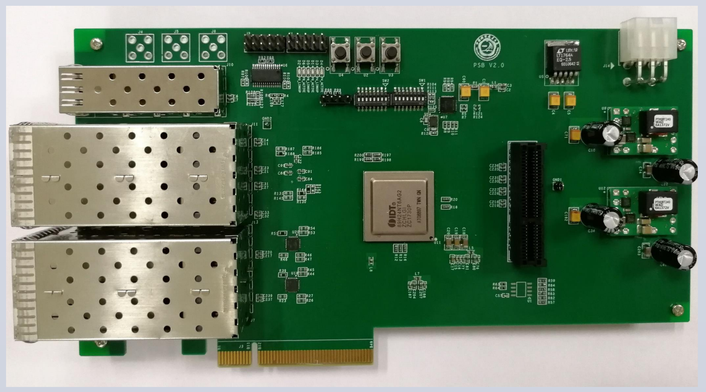


Figure 5. PCIe Switch Module

4. Acknowledgement

This work is supported by National Basic Research Program (973 Program) No. 2015CB85906.

*Corresponding author:cping@ustc.edu.cn