Test and development of the front-end electronics for the Silicon Tracking System of the CBM experiment

A. Rodriguez Rodriguez[1,2] & J. Lehnert[1] for CBM Collaboration

[1] GSI, Darmstadt, Germany, [2] Goethe University Frankfurt am Main, Germany

CBM at FAIR

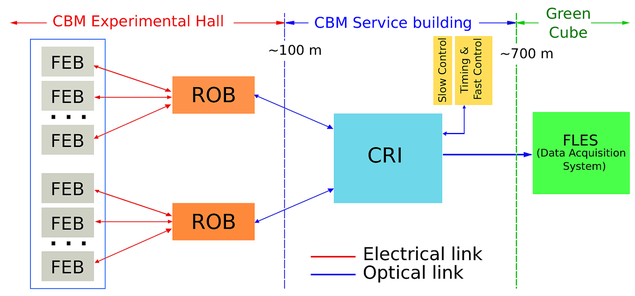
Compressed Baryonic Matter experiment

The Silicon Tracking System (STS) readout chain

CBM is a fixed-target experiment that will run at collision rates up to 10^7 collisions/s with no global trigger [1]. The STS is the main detector for charged particle tracking.

Challenges for the STS readout chain:

- High-granularity detector, with 1.8 million channels
- Free streaming readout of time-stamped data
- Low noise levels
- Radiation hard components
- Low power dissipation



Block diagram of the STS readout chain

Front-end Boards (FEB):

Part of a functional module, where 2 FEB with 8 custom designed ASICs each, are connected via microcables to a double-sided microstrip sensor.

- Every FEB contains 8 STS-XYTER ASICs for reading out 1024 channels
- Provides digitized hits

Readout Board (ROB) [2]**:**

- Data aggregation from several ASICs
- Optical readout interface
- Control and clock distribution
- Based on CERN GBTx and Versatile Link components
- Located inside STS box
  - → Limited space
  - → Radiation hardness

Control Readout Interface (CRI):

- CBM DAQ layer with common hardware platform
- FPGA based
- Timing and control interfaces
- Data preprocessing

First Level Event Selector (FLES):

- Time slice building & full event reconstruction
- Online event selection

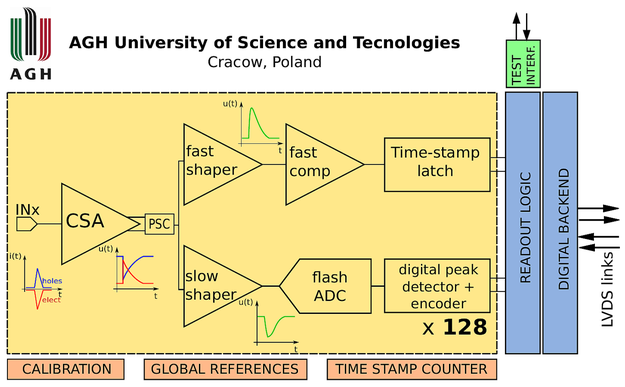
Front-end electronics: STS-XYTER ASIC

STS-XYTER

STS + **X**, **Y** coordinates + **T**ime and **E**nergy **R**esolution [3]

Fabricated in UMC 180 nm technology
Chip area: 10 mm x 6.72 mm

AGH University of Science and Tecnologies
Cracow, Poland



The STS-XYTER ASIC functional blocks

ASIC requirements:

- Expected total input capacitance up to 50 pF
- Channel pitch: 58 µm
- Self-triggered hit generation
- Both signal polarities
- Time measurement accuracy < 10 ns
- Low power < 10 mW/channel
- Hit rate/channel: 250 kHz average
- Radiation hard design: expected up to 20 kGy lifetime

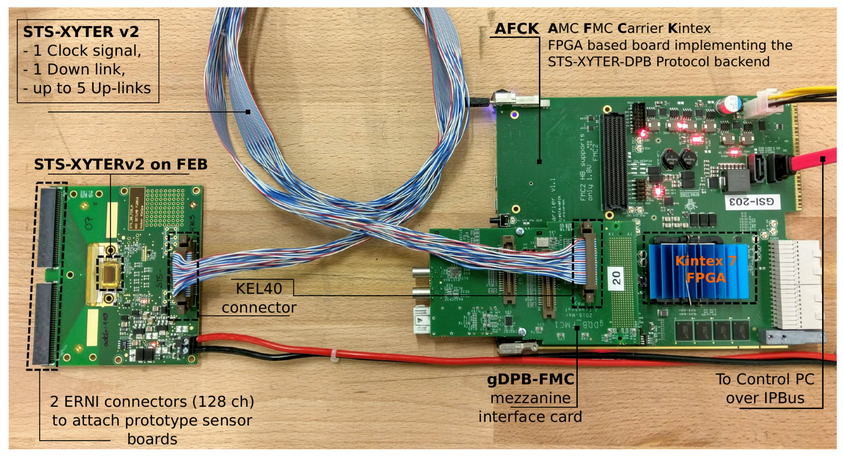
Features:

- 128 readout channels + 2 test channels
- Time resolution < 5 ns
- 5 bit flash ADC/channel
- 15 fC dynamic range
- Digital backend clocked at 160 MHz, compatible with the CERN GBTx data concentrator
- 5 serial LVDS uplinks for hit readout at 320 Mbps each (up to 50 Mhit/s/ASIC)

The STS-XYTER v2 test setup

Prototype FEB with single STS-XYTERv2 controlled via dedicated protocol backend in the AFCK Kintex7-FPGA board [4]. Flexible and modular platform for:

- ASIC and sensor testing and characterization
- Commissioning and test of prototype readout chains
- Software and firmware development



The main components of a STS-XYTER test setup

Test results

CALIBRATION:

Development and test of procedures to evaluate and calibrate in-channel ADCs and fast discriminators.

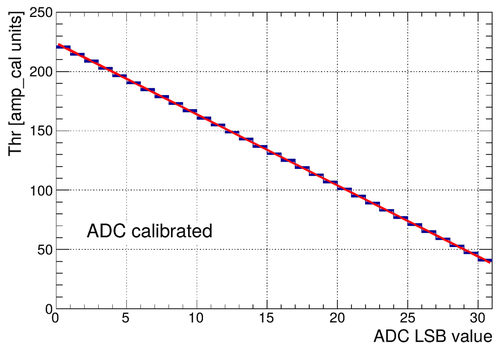
Used ASIC Features:

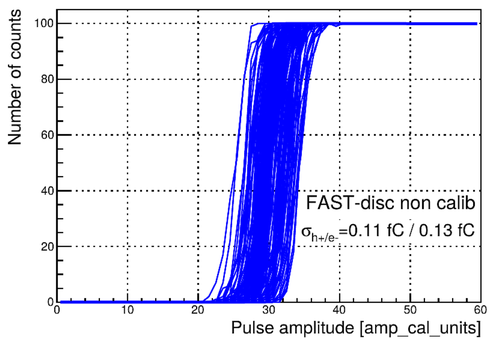
- Internal pulse generator (range up to 15 fC)
- Global DACs set ADCs range
- Every ADC has 31 discriminators with adjustable individual threshold (8 bits)
- FAST discriminator with adjustable individual threshold (6 bits)

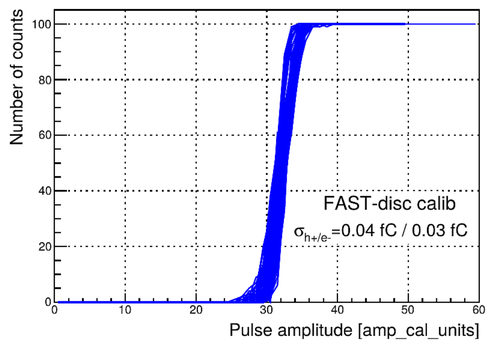
Table 1: Deviation across discriminators in all channels.

Polarity	Before [fC]	After [fC]
holes	0.08	0.02
electrons	0.09	0.02

1 amp_cal_unit = 0.056 fC

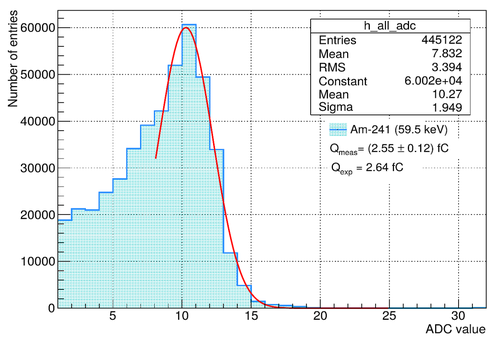




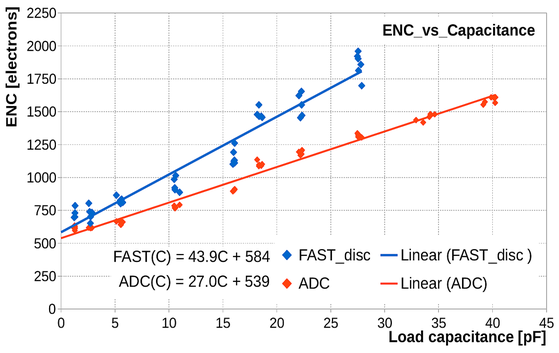


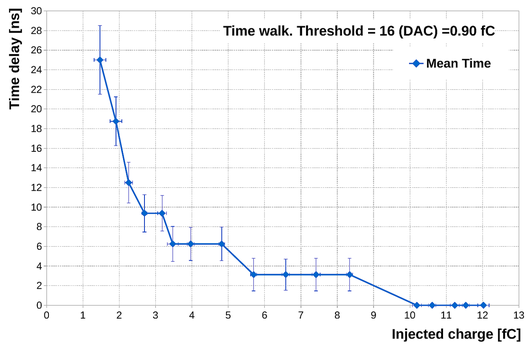
SIGNAL READOUT, TIME-WALK and NOISE ESTIMATION

Spectrum from ^{241}Am source, readout with a 4x6 cm^2 sensor and the STS-XYTERv2 ASIC.



Noise estimation as function of the load capacitance.





Measured FAST discriminator time walk as function of the signal amplitude.

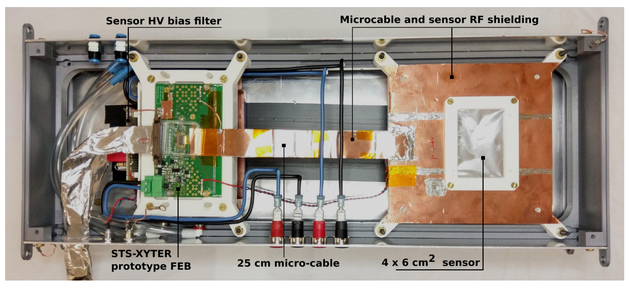
- External reference and test signals were generated using an Agilent 33500B Series waveform generator
- Reference signal amplitude set to ~10 fC with 1 kHz frequency

PERFORMANCE of SENSOR MODULE readout with the STS-XYTER ASIC during BEAM TIME

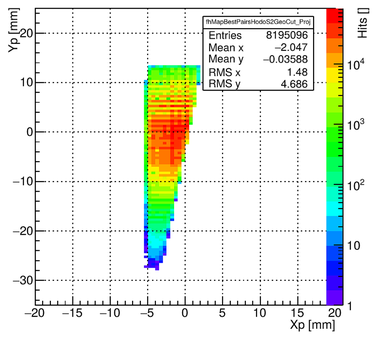
- Proton beam at COSY, Research Center Jülich.
- Momentum: 1.7 GeV/c
- Free streaming readout

Sensor Module for beam tests:

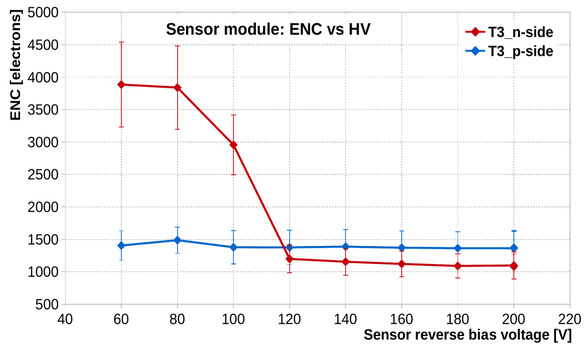
- 4.2 x 6.2 cm^2 double-sided Si sensor.
- 25 cm long microcable
- 2 STS-XYTERv2 on prototype FEBs
- 128 channels readout per sensor side
- Trapezoidal overlap area between sides: 192 mm^2
- Sensor and microcables shielding to reduce noise pick-up



Sensor module used in beam tests



Hit map measured with the module T3 after timing and geometrical constraints



System noise as function of the sensor bias voltage

Summary

- The functionality and performance of the STS-XYTER v2 ASIC have been intensively tested.
- Calibration procedures for the ADCs and fast (timing) discriminator have been developed.
- Signal readout and noise behaviour for a realistic detector module have been studied in laboratory setups and beam tests.

References

[1] Challenges in QCD matter physics —The scientific programme of the Compressed Baryonic Matter experiment at FAIR. *T. Ablyazimov et al.* Eur. Phys. J. A 53 (2017) 60
[2] GBT based readout in the CBM experiment. *J. Lehnert et al.* JINST 12 (2017) C02061
[3] Front-end readout electronics considerations for Silicon Tracking System and Muon Chamber. *K. Kasinski et al.* JINST 11 (2016) C02024
[4] A protocol for hit and control synchronous for the front-end electronics at the CBM experiment. *K. Kasinski et al.* NIM A 835 (2016) 66