

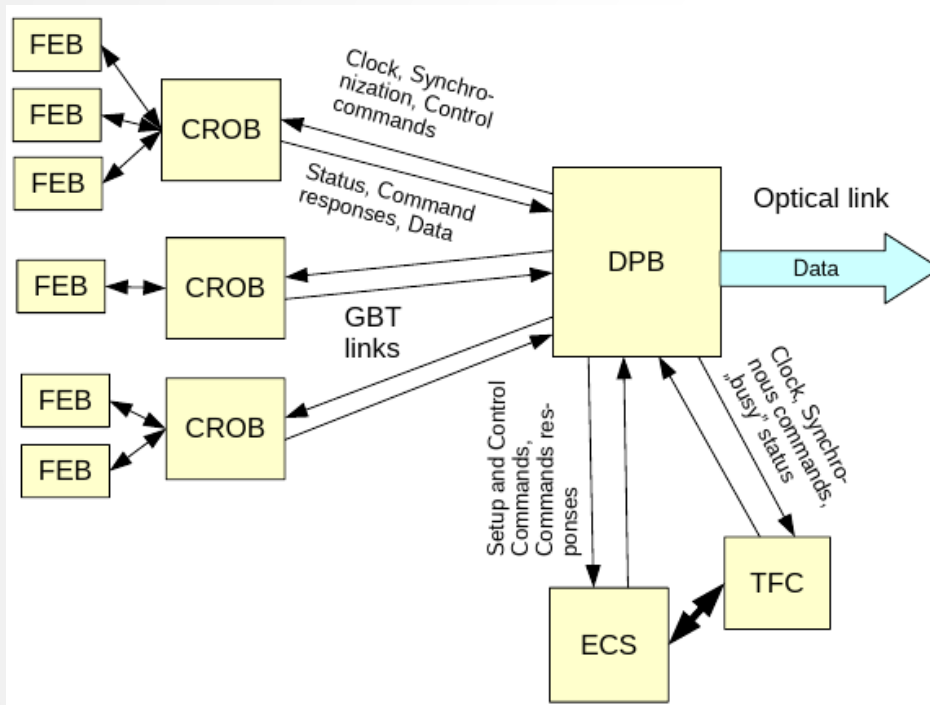
# Synchronisation of GBTx readout boards for CBM experiment

**Adrian Byszuk**

Wojciech Zabołotny, Marek Gumiński

Institute of Electronic Systems  
Warsaw University of Technology

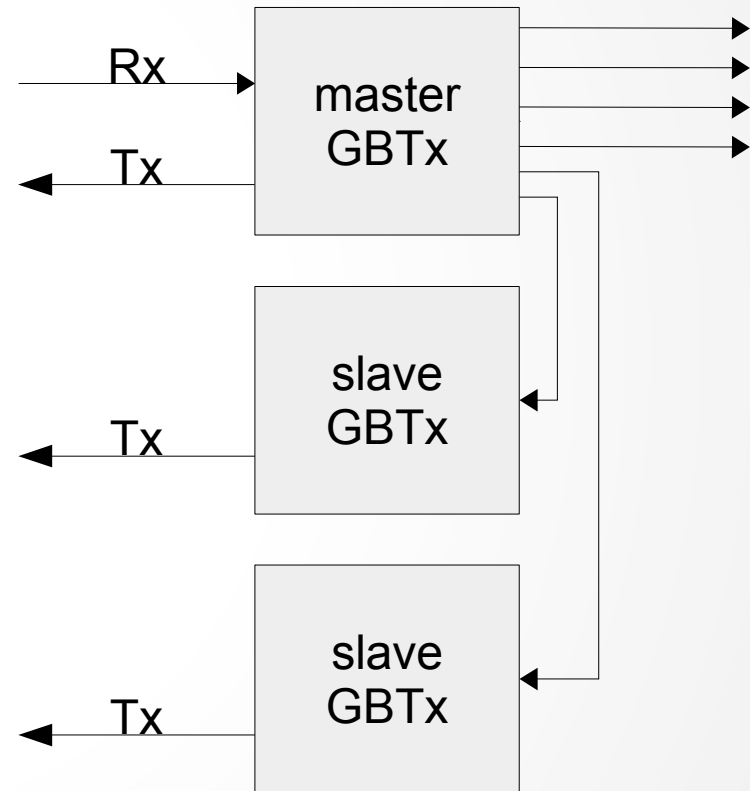
# DAQ readout chain in CBM



- FEBs must be synchronised with experiment clock forwarded by TFC subsystem
- TFC is **not** connected to frontend boards
- Clock is embedded in data stream of GBT links
- Clock recovery is done by GBTx chips on CROB boards
- Transmission clock of FPGA transceivers (DPB/CRI) must be synchronous to the TFC clock

# Clock recovery in CROB

- CROB has 3 GBTx chips: „master” (Rx/Tx) and 2 „slaves” (only Tx)
- master GBTx responsible for clock recovery
- recovered clock forwarded to slave GBTx and FEBs



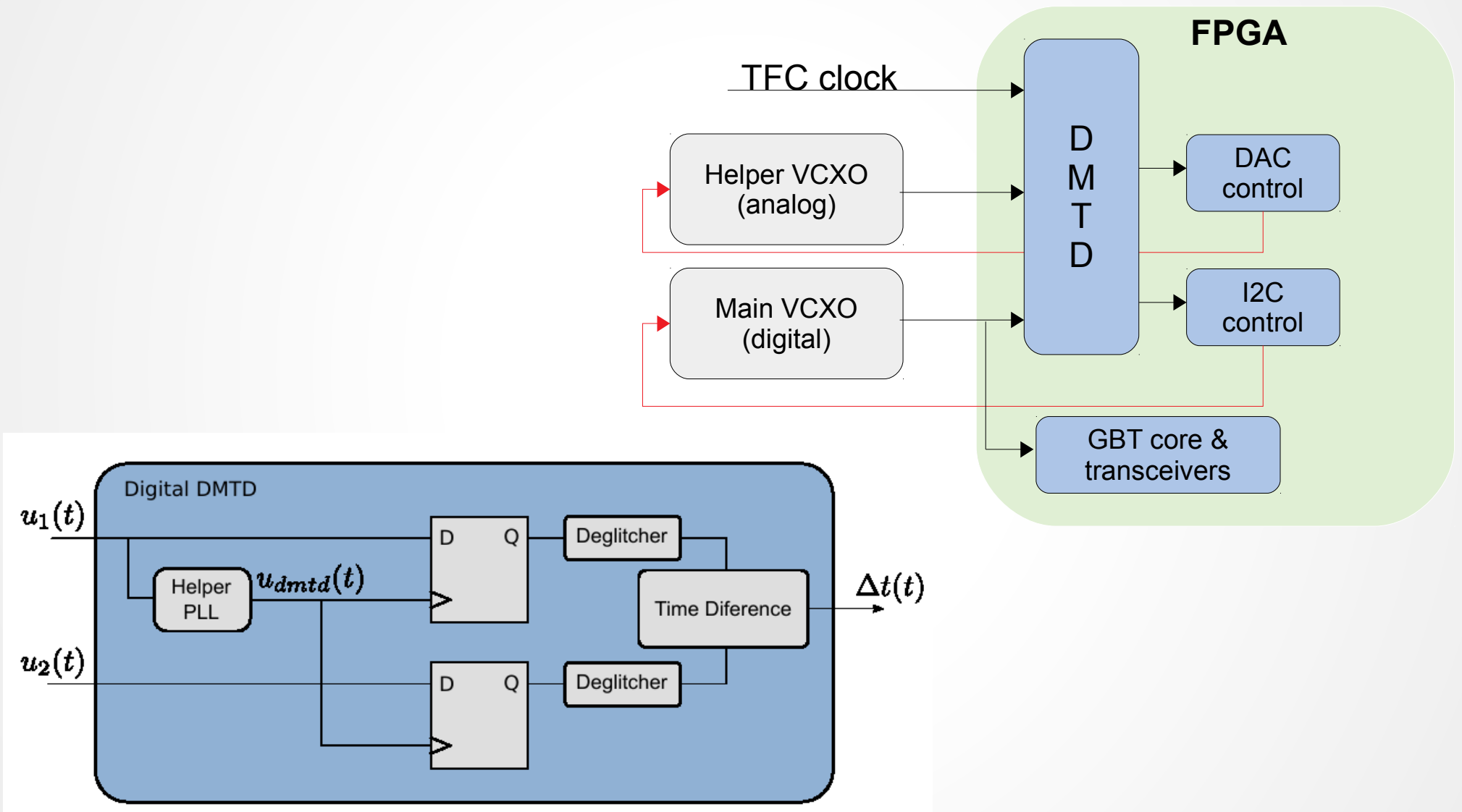
# FPGA MGT clock synchronisation

- MGT needs synchronous reference clock
- We can't use TFC clock directly
- There are 3 ways in which we can provide synchronous clock to gigabit transceivers:
  - Use external PLL chip
  - Design PLL in FPGA gateware to control external VCXO
  - Use internal features of MGT transceivers (available only in some FPGA families)

# FPGA PLL design with external VCXO

- Based on PLL design from WhiteRabbit project
- DMTD (Dual Mixer Time Difference) phase detector offers sub-ps performance
- Open source design
- Original design uses analog VCXO control
- Modifications available for digital VCXO

# DMTD usage in DPB



# Internal MGT clock control with PICXO

- Xilinx GTX/GTH/GTP transceivers have a special hardware block called „Phase Interpolator”
- PI is used to adjust phase of transmission clock
- Constant phase change effectively results in frequency shifting  $F_{OUT} = F_I + \frac{d\Phi_{CONTROL}(t)}{dt}$
- External MGT clock **does not** have to be synchronous
- Xilinx provides complete, free IP solution (encrypted, obfuscated)
- Advertised performance is very good, adds **2-3 ps** jitter

# Summary

- Clock synchronisation is critical for proper data acquisition in CBM experiment
- Clock recovery in CROB boards works reliably
- PICXO offers quite easy, low-cost and lightweight solution; but it's very hard to provide phase/latency determinism
- DDMTD-based PLL is the best solution for DPB
- Choice of final CRI board may require re-evaluation of these findings



Thank you for your attention!