WUT and AGH contribution to CBM experiment

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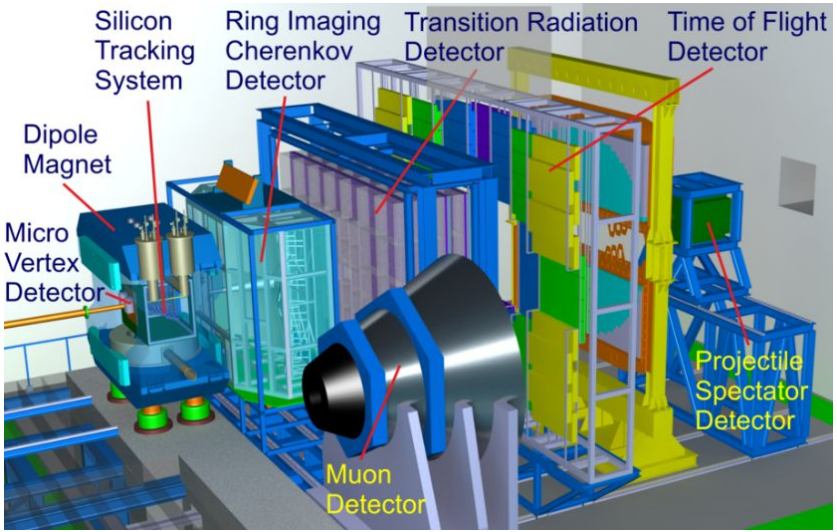
Introduction

Experiment

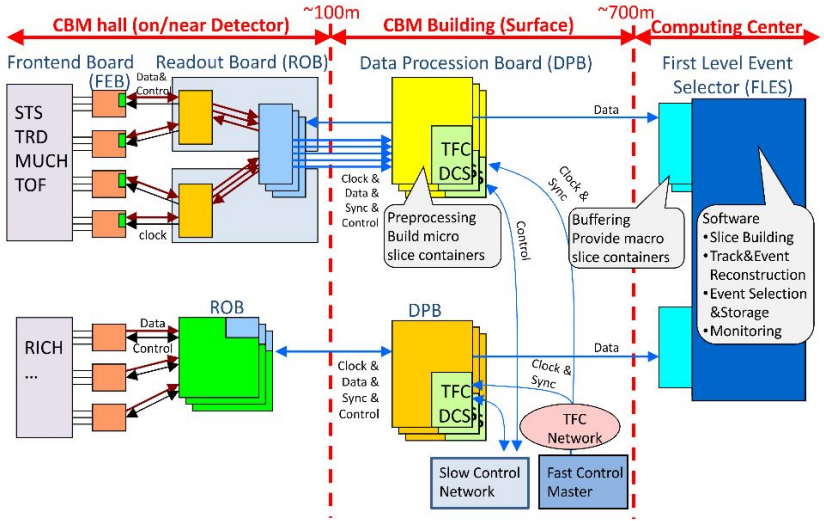
- research properties of extremely dense matter
- multiple specialised detectors
- no hardware trigger
- selection of interesting data based on complete decay reconstruction
- overlap of bunch decays
- data split into overlapping “time slices”



[1]

Readout chain

- multiple Front End modules
- data concentration in ROB (GBTx)
- data aggregation and processing in DPB
- event reconstruction and selection in FLES
- commons synchronisation propagated via DPB

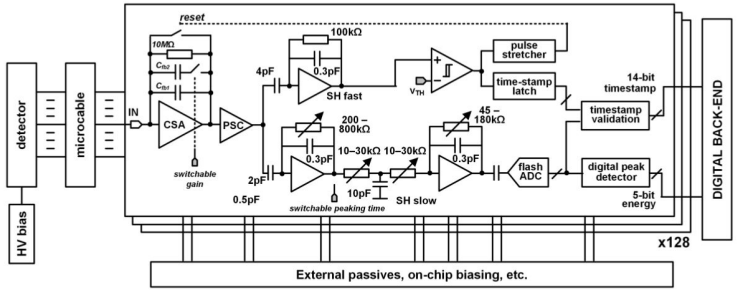


[2]

AGH and WUT contribution

STS-XYTER2 Front End modules

- design of FEE modules done by AGH
- 128 low noise analogue channels
- digital backend with 5 serial channels
- channel throughput of 320 Mb/s (~10 MHits/s)
- radiation tolerant: (TID= 3 MRad)



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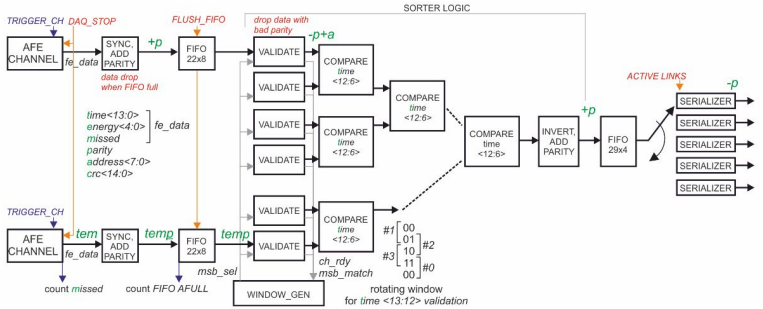
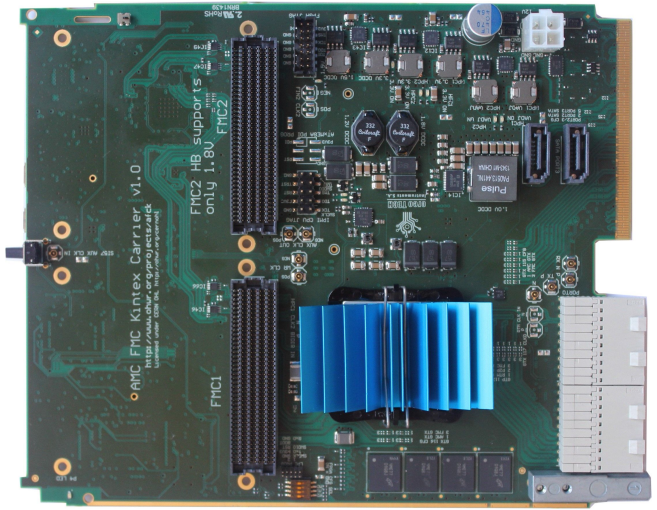


[4]

Data Processing Board prototype (AFCK)

- Open Hardware AMC Module
- Xilinx Kintex-7 325T FFG900 FPGA
- 16 10Gbps transceivers
- configurable low jitter clock crossbar
- support for White Rabbit synchronisation
- two FMC and SATA connectors



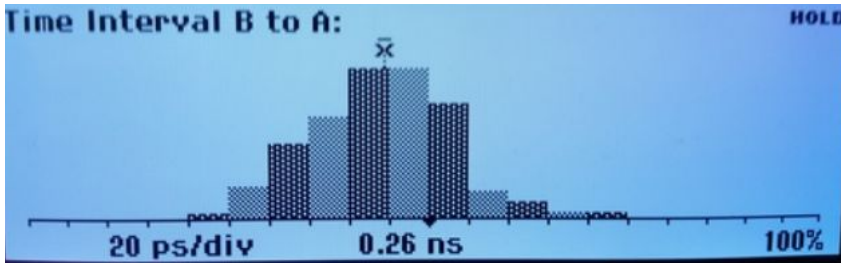
[5]

Slow control

- comparison of slow control candidates
- selection of IPbus protocol
  - based on Ethernet 1000 BaseX
  - transmission with acknowledgement
- implementation of IPbus core on AFCK
- implementation of IPbus infrastructure components

Synchronisation

- porting of White Rabbit node to AFCK
- synchronisation verification
- current implementation of synchronisation system is based on WR, but was developed at KIT



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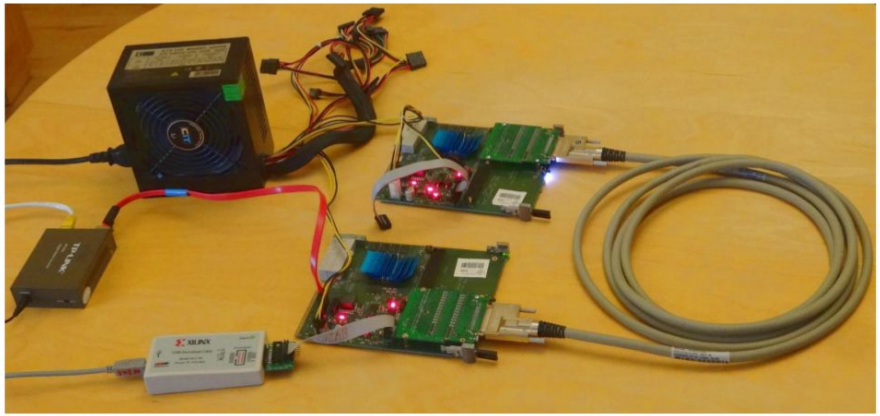
STS-XYTER communication

- protocol specification
- STS-XYTER emulator on AFCK
- protocol tester on AFCK
- communication with real STS-XYTER2
- python library enabling communication over IPBus



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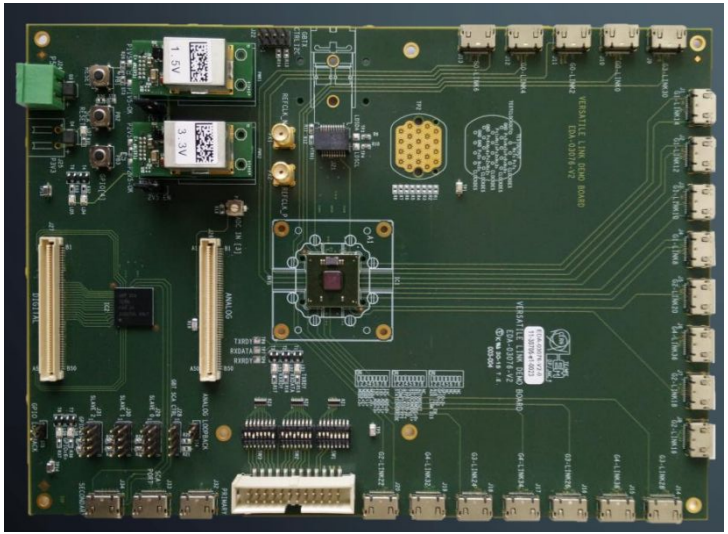
GBTx

- communication with GBTx
- modification of DPB interface core
- GBTx configuration for CBM experiment
- communication with DPB over GBTx



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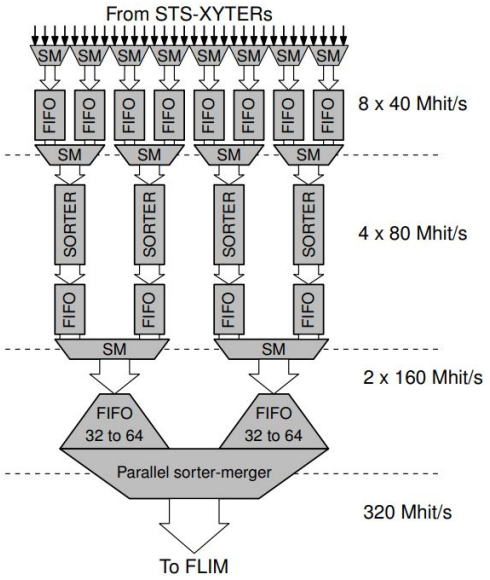
Data aggregation and sorting

- time sorting the input data
- aggregation of multiple channels
- generation of time slices
- throughput of 320 MHit/s



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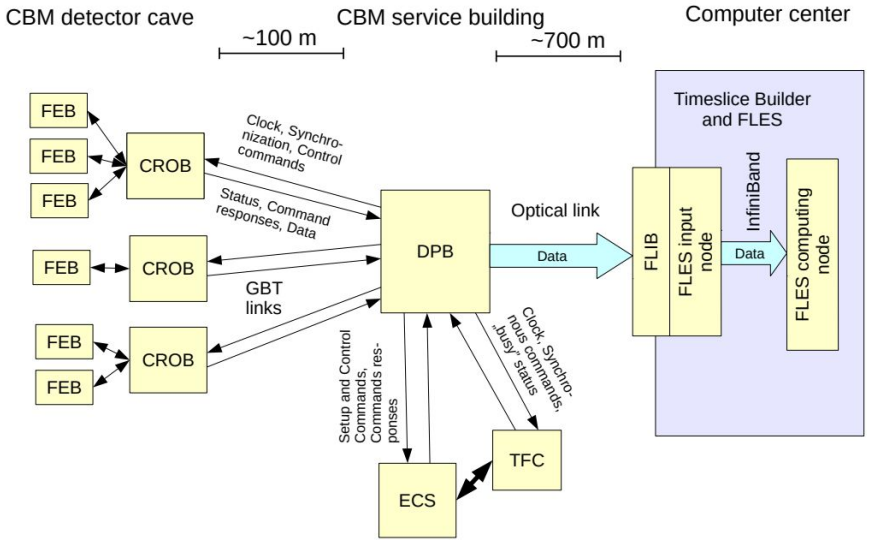
Common Readout Interface

- DPB and FLES replaced with a single module - CRI
  - PCIe interface
  - located CBM building
  - standard communication protocol with computer farm
- WUTs contribution in CRI hardware selection



Thank you for attention

Others

Image sources

1. J. Lehnert *et al* 2017 *JINST* **12** C02061
2. J. Lehnert *et al* 2017 *JINST* **12** C02061
3. K. Kasinski et al 2016 JINST **11** C02024
4. K. Kasinski *et al* 2016 *JINST* **11** C11018
5. https://www.ohwr.org/projects/afck/wiki
6. W.M. Zabołotny *et al* 2017 *JINST* **12** C02060
7. CBM Progress Report 2017
8. APPLICATION ENGINEER, VERSATILE LINK DEMONSTRATOR BOARD, FTEC 2015 QUARTERLY REPORT PH3464, RAÚL MARTÍN LESMA
9. M. Gumiński, W. Zabołotny, G. H. Kasprowicz, K. Poźniak, and R. Romaniuk, “Time and clock synchronization with AFCK for CBM,” in Proceedings of SPIE, Photonics Applications in Astronomy, Communications, Industry, and High-Energy Physics Experiments, 2015, vol. 9662, p. 96622V–1.