Noise Performance Analysis for the Silicon Tracking System Detector and Front-End Electronics

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Agenda

- Brief intro: Silicon Tracking System in the CBM experiment.
- Motivation.
- Sources of noise in a detection system.
- Impact of shaping amplifiers and preamplifier on noise.
- Noise reduction options.
- MiniASIC architecture proposals.
- Summary.

CBM experiment, GSI, Darmstadt, Germany

AGH

CBM

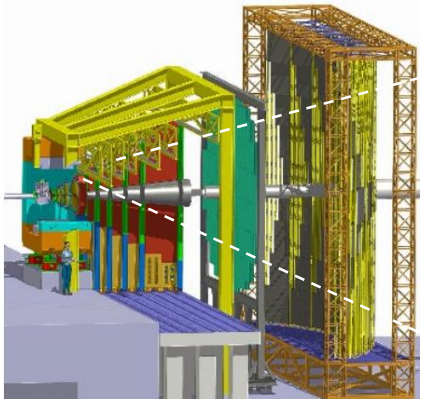
FAIR Facility for Antiproton and Ion Research in Europe GmbH

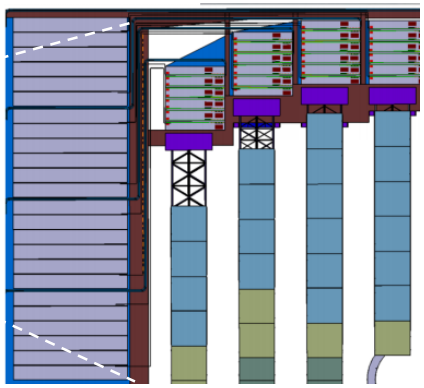
Aim: creation of the highest baryon densities in nucleus-nucleus collisions for the exploration of the properties of the super-dense nuclear matter. Exploration of the QCD phase diagram in the region of very high baryon densities

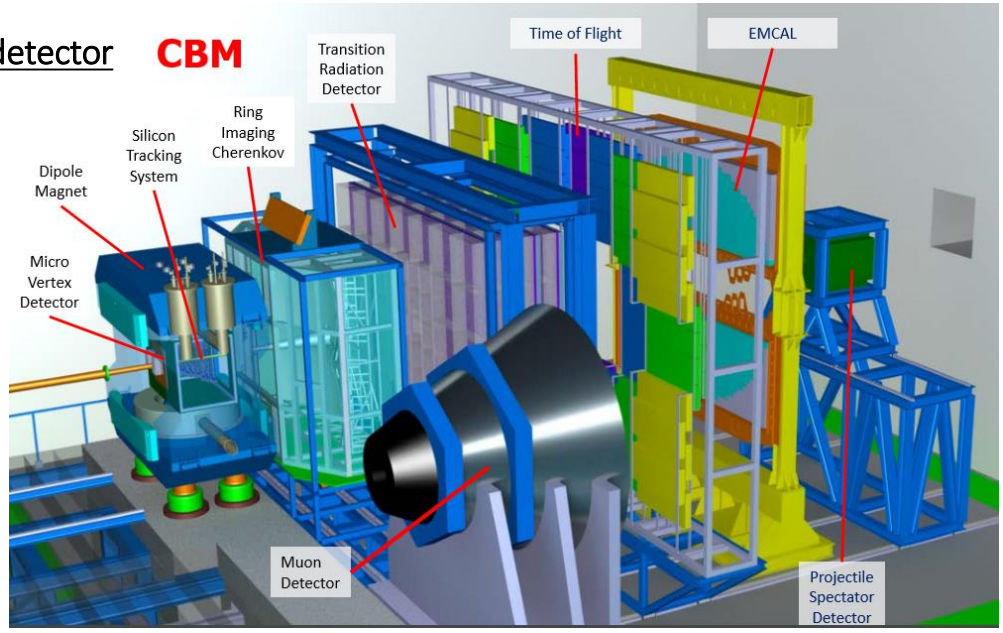
STS metrics:
>1 790 000 channels
>14 000 ASICs
1752 FEBs
600 ROBs
78 DPBs

STS (*Silicon Tracking System*) detector

Particles' track and momentum determination
Interaction rate 10 MHz
Silicon strip detectors

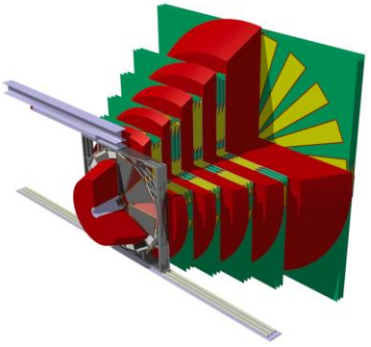






MUCH (*Muon Chamber*) detector

Gaseous detector (GEM)



Read-out electronics at the perimeter of the detection stations (FEB : 8 chips/board) + data concentrator (based on GBTx)

multi-line micro-cables-> sensors' read-out

double–sided, micro-strip sensors,1024 CH/side, 7.5◦ stereo angle, **58 µm** strip pitch

J. Heuser, et al., *GSI Report 2013-4 Technical Design Report for the CBM Silicon Tracking System (STS)*, GSI, Darmstadt, 2013.

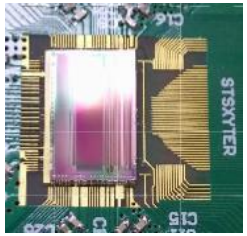
STS system overview

Read-out electronics

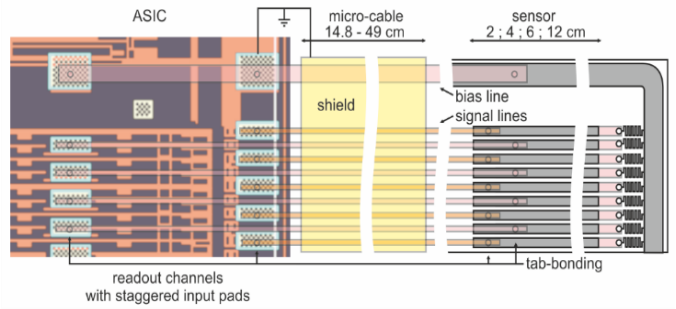
Total ENC: < 1000 e⁻ rms in system
Power: <10 mW / channel
CSA gain: 10 mV/fC
SH_slow gain: 35 mV/fC
SH_fast gain: 75 mV/fC
Peaking time (slow path): 90 ns
Peaking time (fast path): 40 ns

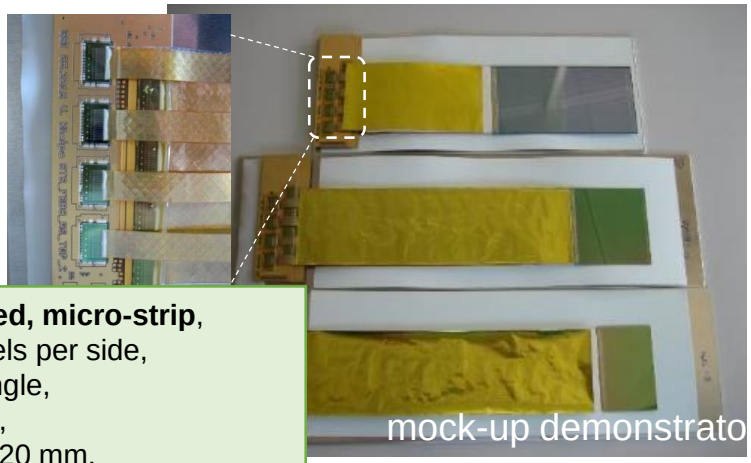
The STS/MUCH-XYTER2 (SMX2):

- developed at AGH University Cracow
- 10 mm × 6.8 mm, 288 pads
- 128 readout channels + 2 test channels
- Power: 1.1 – 1.3 W per chip
- 5-bit continuous-time ADC + 14-bit Timestamp
- Range of operation: 0-15 fC (STS)
- 250 kHit/s/channel (fast reset enabled)
- 9.41-47 Mhit/s/chip

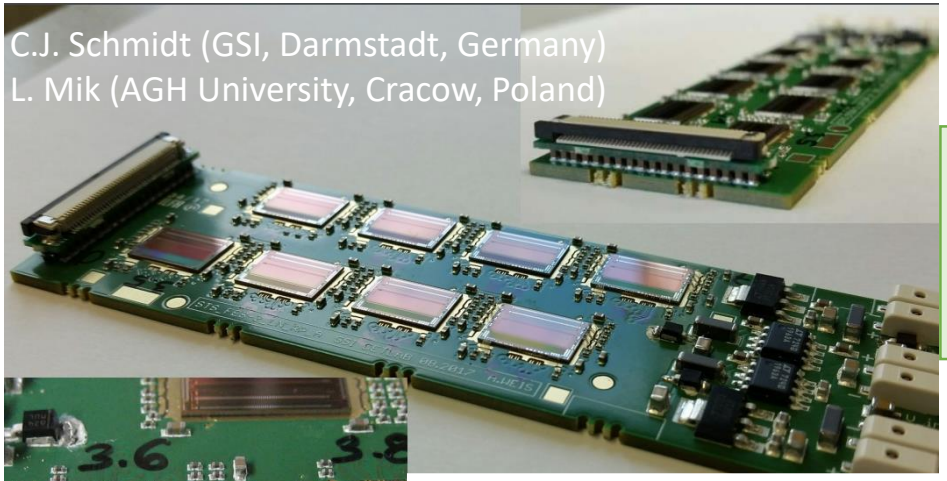


Sensor and micro-cable



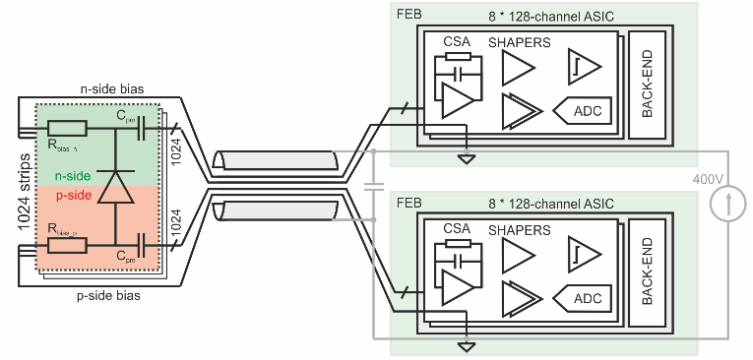


double–sided, micro-strip,
1024 channels per side,
7.5 stereo angle,
58 μm pitch,
lengths 20-120 mm,
300μm thickness,



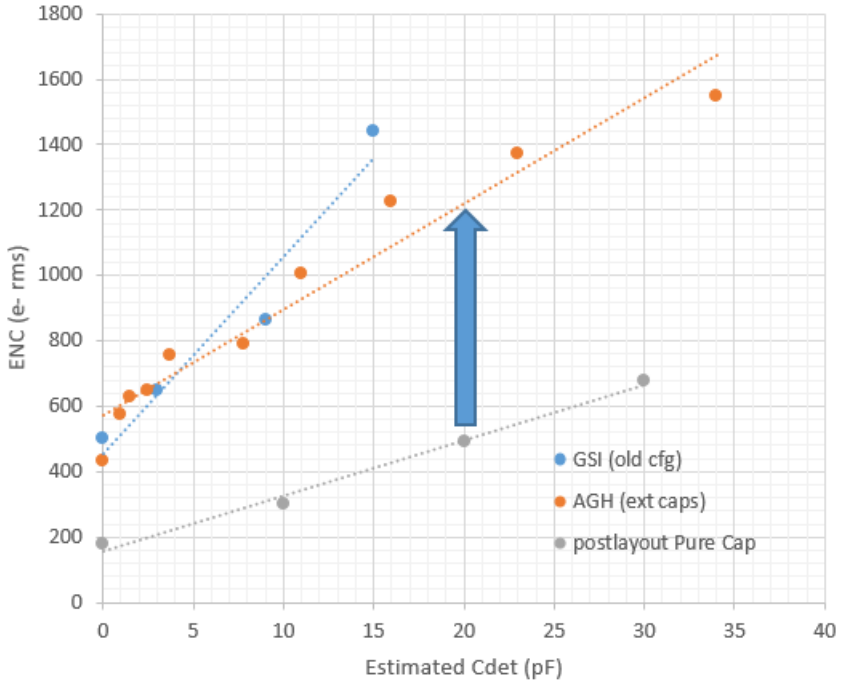
FEB (Front-end Board):

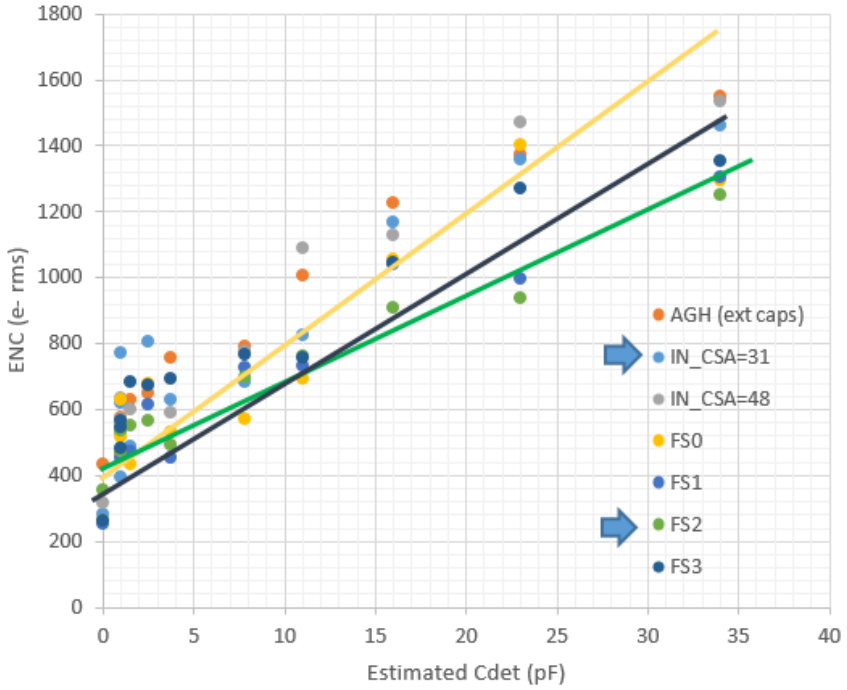
8 ASICs - read-out of a single side of 1024 strip sensor
Rad-hard LDOs (VECC India)
AC-coupling of SLVS e-links

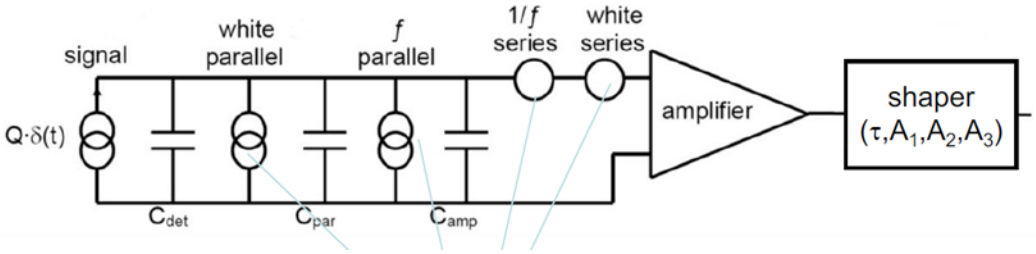


Motivation

ENC vs Cdet

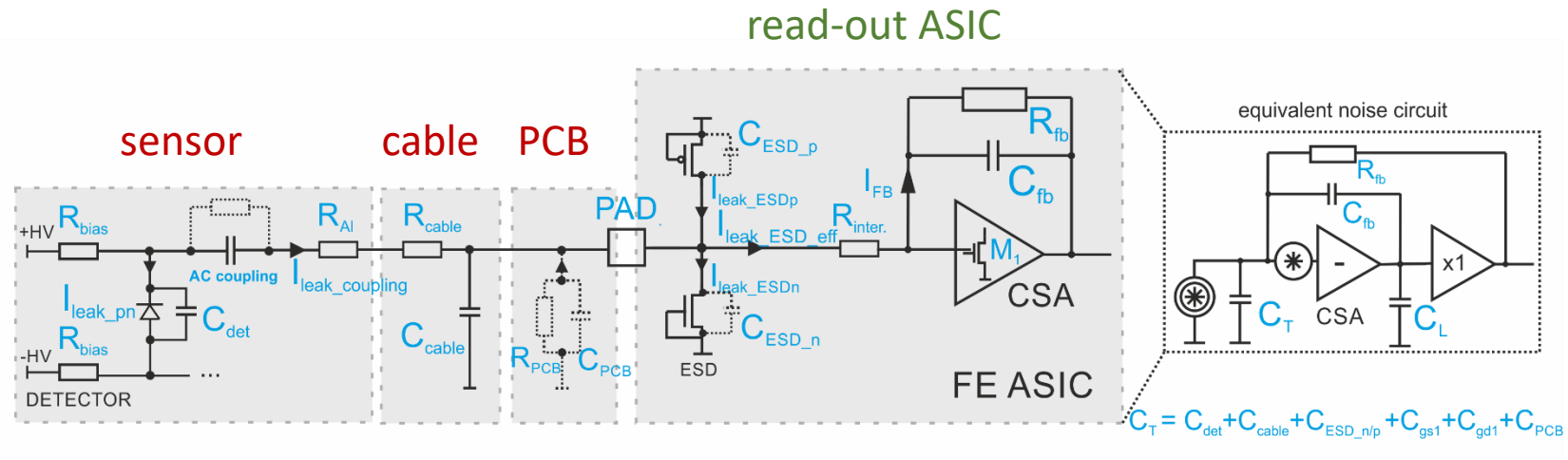






- many noise sources in the system;
- can be divided between intrinsic (contributed by the input amplifier itself) and extrinsic (originating in the sensor and biasing network).

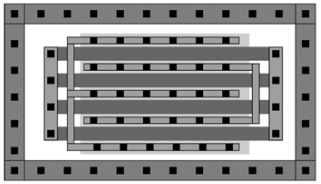
Noise sources in the detection system



1. parallel current noise:
   - detector leakage current shot noise (I_L),
   - detector bias shunt resistance R_{bias},
   - leakage current flowing through transistors in the Electrostatic Discharge (ESD) protection circuit,
   - current thermal noise from feedback resistance.
2. series white noise:
   - input transistor thermal noise ($M1_{th}$),
   - various series resistors' (sensor's metal strip, cable, interconnect on-chip) thermal noise.
3. series 1/f (or flicker) noise:
   - CSA input transistor flicker (1/f) noise (M1f).

Noise at CSA output - detailed considerations

- all devices forming the core amplifier and its feedback network contribute to the overall noise,
- usually only a few of them have a noticeable impact on the total ENC



Input transistor layout to reduce noise from the gate and the bulk resistance.

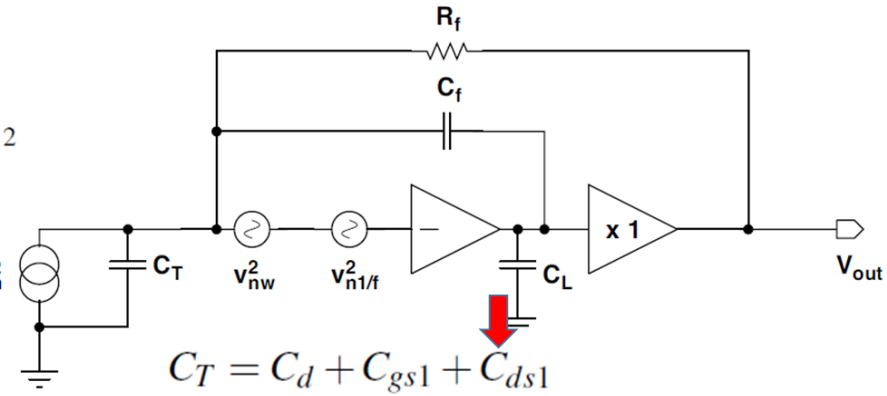
$$i_{n4}^2 = 4k_B T\,\alpha_{w4}\gamma_4 g_{m4}$$

$$i_{n,2}^2 = 4k_B T\,\alpha_{w2}\gamma_2 g_{m2,eq}$$

$$g_{m2,eq} = \frac{g_{m2}}{1+g_{m2}r_{01}} \approx \frac{1}{r_{01}} \ll g_{m1}$$

$$\frac{4k_B T}{R_{f,eq}} = 2qI_L \rightarrow R_{f,eq} = \frac{2k_B T}{qI_L} \approx \frac{50\text{ mV}}{I_L}$$

e.g. Il=1nA => Rf > 50 Mohm



$$v_{nw1,bulk}^2 = 4k_B T R_B \left(\frac{g_{mb1}}{g_{m1}}\right)^2$$

$$v_{nf1}^2 = \frac{K_f}{C_{ox}WL}\frac{1}{f}$$

$$v_{nw1}^2 = 4k_B T\,\alpha_{w1}\gamma_1 \frac{1}{g_{m1}}$$

$$C_T = C_d + C_{gs1} + C_{ds1}$$

A. Rivetti

”CMOS Front-end Electronics for Radiation Sensors”

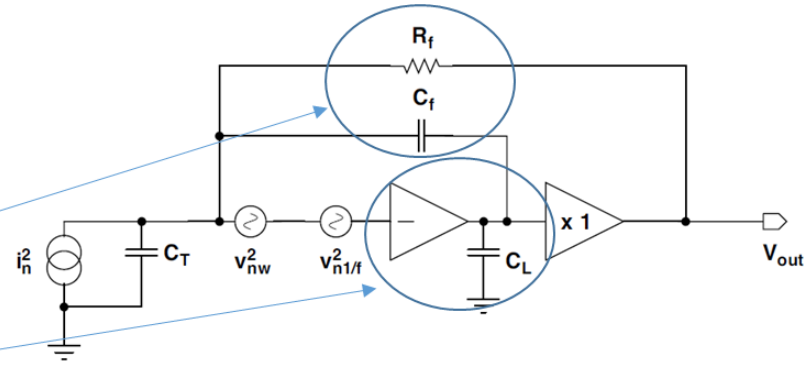
Noise at CSA output - detailed considerations

$$P_{av,out} = < y(t)^2 > = \int_{-\infty}^{\infty} S_{xx}(f)|H(f)|^2 df$$

Parallel, Current Noise

$$< v_{out}^2 >_{ni} = i_n^2 R_f^2 \int_0^{\infty} \left| \frac{1}{(1+s\tau_f)(1+s\tau_r)} \right|^2 df$$

$$\int_0^{\infty} \left| \frac{1}{(1+s\tau_f)(1+s\tau_r)} \right|^2 df = \frac{1}{4(\tau_f+\tau_r)} \approx \frac{1}{4\tau_f}$$



- τ_f – falling time, related to the CSA feedback capacitor discharge time constant
- τ_r - rising time, related to the CSA bandwidth (~40 ns for the CSA GBW ~9 GHz) -> the input of the CSA bandwidth has no strong impact on the ENC

$$< v_{out}^2 >_{ni} = \frac{i_n^2}{4}\frac{R_f}{C_f} \Rightarrow i_n^2 = 2qI_L \Rightarrow < v_{out}^2 >_{ni} = \frac{qI_L}{2}\frac{R_f}{C_f}$$

/($1/C_f^2$)

$$ENC_i^2 = \frac{i_n^2}{4}\frac{R_f C_f}{q^2} \Rightarrow i_n^2 = 2qI_L \Rightarrow ENC_i = \sqrt{\frac{I_L \tau_f}{2q}}$$

$$\Rightarrow i_n^2 = \frac{4k_B T}{R_f} \Rightarrow ENC_i = \frac{1}{q}\sqrt{k_B T C_f}$$

Preferably, the total noise is limited to the one produced by the input transistor. The noise introduced by other devices can be neglected.

Noise at CSA output - detailed considerations

Series, Voltage Noise => convert to current by $v_{nw}^2 s^2 C_T^2$

White series

$$< v_{out}^2 >_{nw} = v_{nw}^2 R_f^2 C_T^2 \int_0^\infty \left| \frac{j2\pi f}{(1+j2\pi f\tau_f)(1+j2\pi f\tau_r)} \right|^2 df$$

$$\int_0^\infty \left| \frac{j2\pi f}{(1+j2\pi f\tau_f)(1+j2\pi f\tau_r)} \right|^2 df = \frac{1}{4\tau_f\tau_r(\tau_f+\tau_r)} \approx \frac{1}{4\tau_f^2\tau_r}$$

$$< v_{out}^2 >_{nw} = v_{nw}^2 C_T^2 R_f^2 \frac{1}{4R_f^2 C_f^2 \frac{C_T C_L}{g_{m1} C_f}}$$

$$v_{nw1,bulk}^2 = 4k_B T R_B \left(\frac{g_{mb1}}{g_{m1}} \right)^2$$

$$v_{nw1}^2 = 4k_B T \alpha_{w1} \gamma_1 \frac{1}{g_{m1}}$$

detector

$$< v_{out}^2 >_{nw} = : \gamma k_B T \frac{C_T}{C_f C_L} \Rightarrow ENC_w = \frac{1}{q} \sqrt{\gamma k_B T \frac{C_T C_f}{C_L}}$$

CSA gain

CSA bandwidth

1/f series noise

$$v_{nf1}^2 = \frac{K_f}{C_{ox} W L} \frac{1}{f}$$

$$< v_{out}^2 >_{nf} = \frac{K_f}{C_{ox} W_1 L_1} C_T^2 R_f^2 \int_0^\infty \frac{1}{f} \left| \frac{j2\pi f}{(1+j2\pi f\tau_f)(1+j2\pi f\tau_r)} \right|^2 df$$

$$\int_0^\infty \frac{1}{f} \left| \frac{j2\pi f}{(1+j2\pi f\tau_f)(1+j2\pi f\tau_r)} \right|^2 df = \frac{\ln\left(\frac{\tau_r}{\tau_f}\right)}{\tau_r^2 - \tau_f^2} \approx \frac{1}{\tau_f^2} \ln\left(\frac{\tau_f}{\tau_r}\right)$$

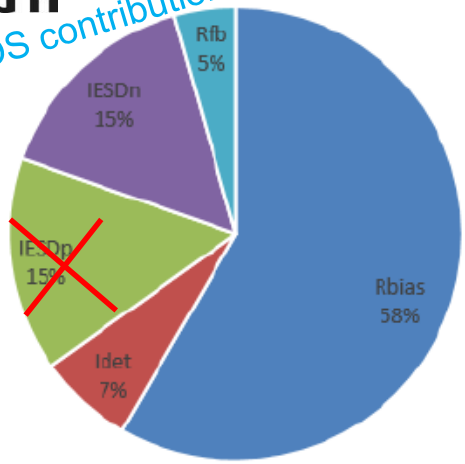
$$< v_{out}^2 >_{nf} = \frac{K_f}{C_{ox} W_1 L_1} \frac{C_T^2}{C_f^2} \ln\left(R_f C_f \frac{g_{m1} C_f}{C_T C_L} \right)$$

$$ENC_f = \frac{C_T}{q} \sqrt{\frac{K_f}{C_{ox} W_1 L_1}} \sqrt{\ln\left(R_f C_f \frac{g_{m1} C_f}{C_T C_L} \right)}$$

- CSA output noise related to input in ENC is strongly dependent on the CSA transfer function
- The noise spectral density at CSA output is dependent on the total input capacitance (including detector capacitance), feedback capacitance and CSA load capacitance.

Noise contributors

PMOS contribution is 10* lower



Source	Typ. value	Used for calc.
R_{bias}	500 $k\Omega$ - 1.5 $M\Omega$	1.5 $M\Omega$
I_{det}	1 - 8 nA/cm	4 nA
I_{ESDn}	1 - 10 nA	9 nA
I_{ESDp}	1 - 10 nA	9 nA
R_{fb}	5 $M\Omega$ - 30 $M\Omega$	20 $M\Omega$
R_{Al}	10.5 Ω/cm	42 Ω
R_{cable}	0.635 Ω/cm	12.7 Ω
$R_{inter.}$	10 Ω - 25 Ω	15 Ω
$M_{1,th}$	Tech. dep.	$\alpha = 0.5$, $\gamma = 1$, g_m=0.044 A/V

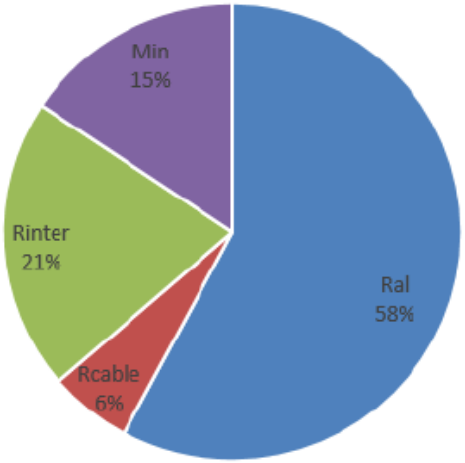


Figure 1: Components of the current noise.

Figure 2: Components of the voltage noise.

$$i_n^2 = \frac{4k_BT}{R_{bias}} + \frac{4k_BT}{R_{FB}} + 2qI_{det} + 2qI_{ESDn} + 2qI_{ESDp}$$

$$v_{nw}^2 = 4k_BTR_{Al} + {}^4/_3\, k_BTR_{cable} + 4k_BTR_{inter} + 4k_BT\alpha_w\gamma\, {}^1/_{g_m}$$

Input transistor flicker noise

$$v_{nf}^2 = \frac{k_f}{C_{ox}WLf}$$

Total noise at shaper's output:

$$\boldsymbol{ENC^2 = ENC_i{}^2 + ENC_w{}^2 + ENC_{1/f}{}^2 \rightarrow ENC^2 = \tau_p \cdot A_i \cdot i_n{}^2 + \frac{1}{\tau_p} \cdot v_n{}^2 \cdot A_w \cdot C_T{}^2 + A_{1/f} \cdot v_{nf}{}^2 \cdot C_T{}^2}$$

where Ct is the total capacitance connected to CSA input: $C_t = C_g + C_{fb} + C_{calib} + \boldsymbol{C_{DET}}$,
A_w A_i and $A_{1/f}$ are weighting coefficients for thermal, current and flicker noise respecitvely (depending on the filter type and order) and $\boldsymbol{\tau_p}$ is the peaking time.

ENC calculations – shaping amplifier's output

	A_w	$A_{1/f}$	A_i
CR-RC	0.92	3.69	0.92
CR-RC^2	0.85	3.41	0.64
CR-RC^3	0.93	3.32	0.52
CR-RC^4	1.02	3.27	0.45
CR^2-RC	1.03	4.70	1.00
CR^2-RC^2	1.16	4.89	0.72
Complex conjugate poles, 3rd order	0.85	3.39	0.61
Complex conjugate poles, 5th order	0.96	3.27	0.45

The total noise at shapre's output containing simplified expressions for each type of noise:

$$ENC^2 = A_w \frac{1}{\tau_p} \frac{4kT\gamma}{g_m} C_T^2 + A_f K_f C_T^2 + A_i \tau_p \left[2q\left(I_{det} + I_{fb}\right) + \frac{4kT}{R_{bias}} + \frac{4kT}{R_{fb}}\right]$$

where g_m and γ are parameters of the CSA input transistor:

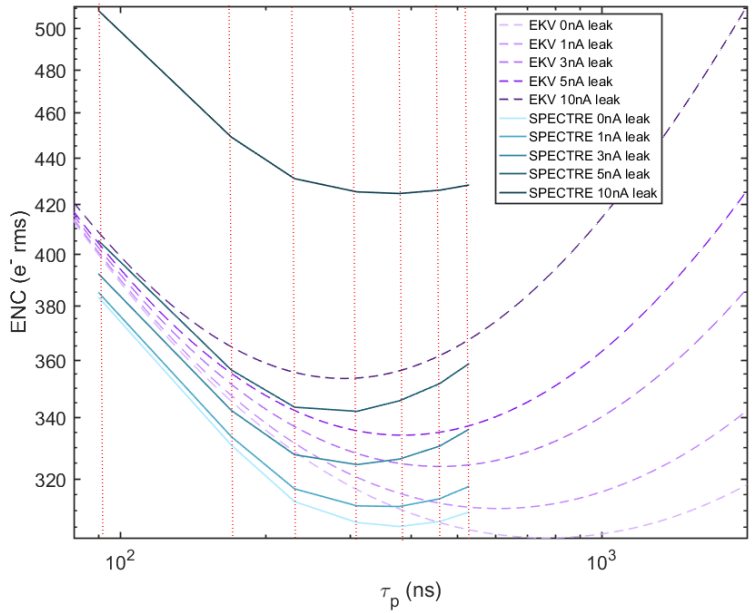
$$g_m = \frac{I_{DS}}{n\varphi_T} f(i_f),\ f(i_f) = \frac{1}{\sqrt{i_f + 0.5\sqrt{i_f} + 1}},\ \gamma = \frac{1}{2} + \frac{1}{6}\frac{i_f}{i_f + 1}$$

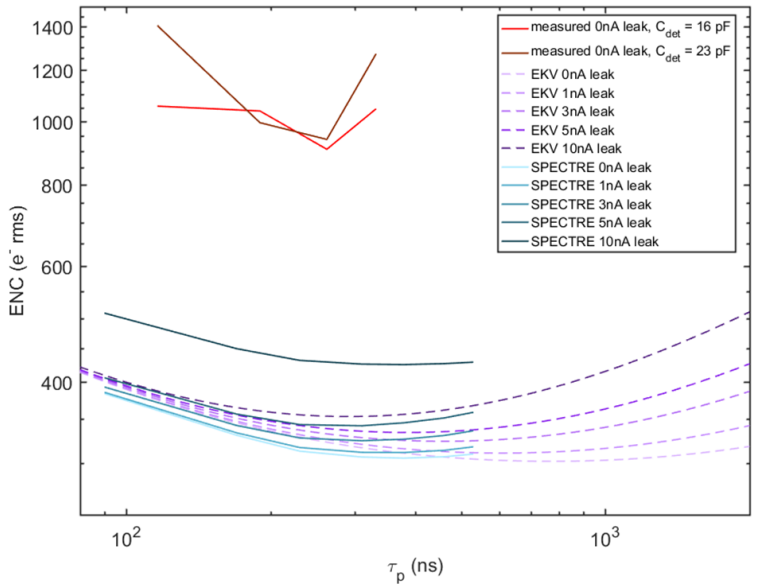
Decisions (ASIC):
- Minimize R_{inter} (~50%)
- Remove ESD

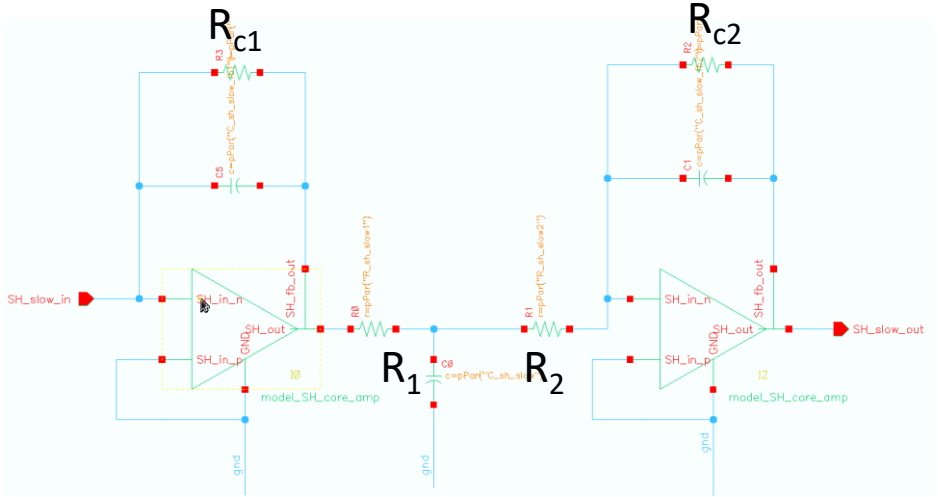
Decisions (Sensor):
- Minimize Al strip resistance
- Maximize R_{bias} (>5Mohm)

ASIC: Weighting coefficients of filters and peaking time can be used for multi-dimensional ENC minimization based on given conditions.

Results – EKV model and simulations







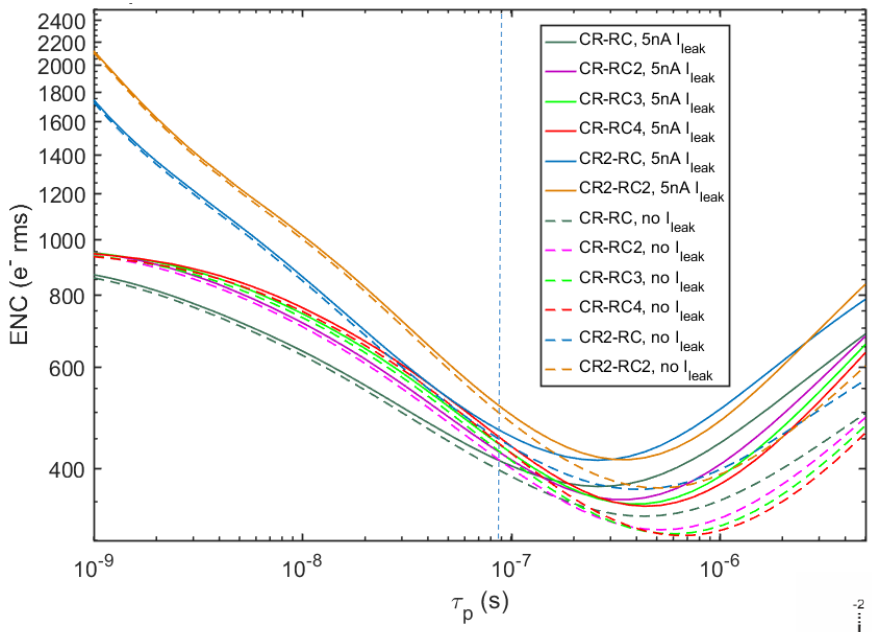
Model of the slow shaper implemented in SMX2 chip.

CR-RC^2 peaking times

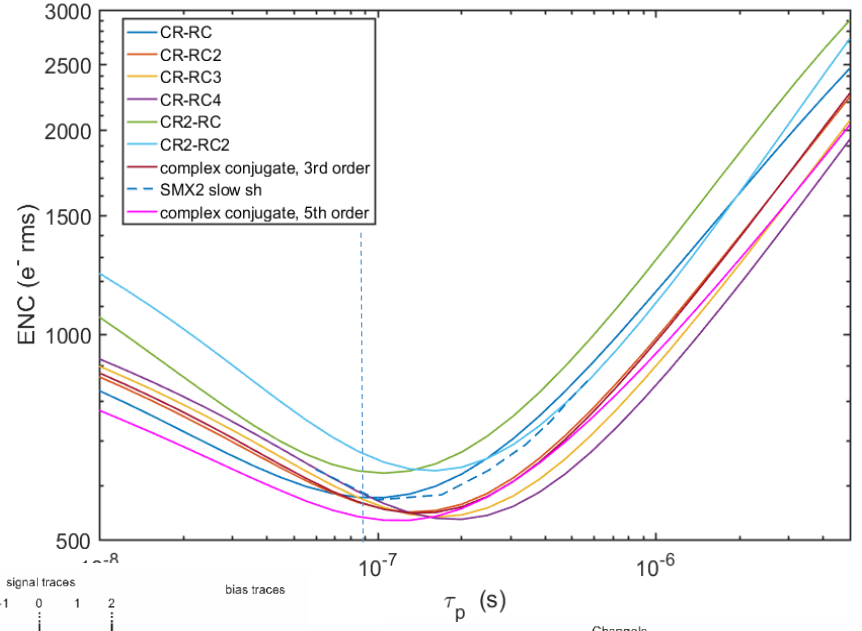
R_{c1}, R_{c2}, R_1, R_2	t_p for electrons (ns)	t_p for holes (ns)
200k, 45k, 10k, 10k	90	90
400k, 90k, 20k, 20k	170	170
600k, 135k, 30k, 30k	230	230
800k, 180k, 40k, 40k	310	310
1M, 225k, 50k, 50k	380	390
1.2M, 270k, 60k, 60k	460	460
1.4M, 315k, 70k, 70k	530	530

Simulations results – various shapers architectures

- R_{fb} noisy,
- ESD attached,
- pure capacitance (20 pF),
- detector leakage equal to 0 and 5 nA.

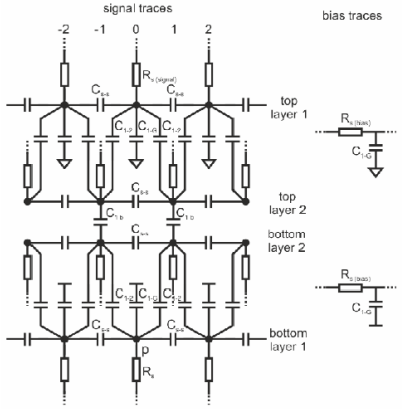


- R_{fb} noisy,
- ESD attached,
- detector model + shunt bias resistances+ interconnect series resistances,
- detector leakage 5 nA.

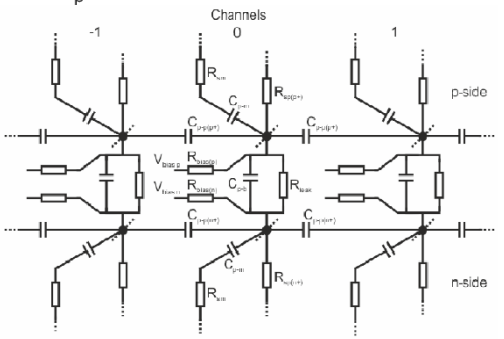


Simulation models of a) the cable and b) the double-sided sensor used for simulations; cable length = 49 cm and sensor lenght = 4 cm.

a)



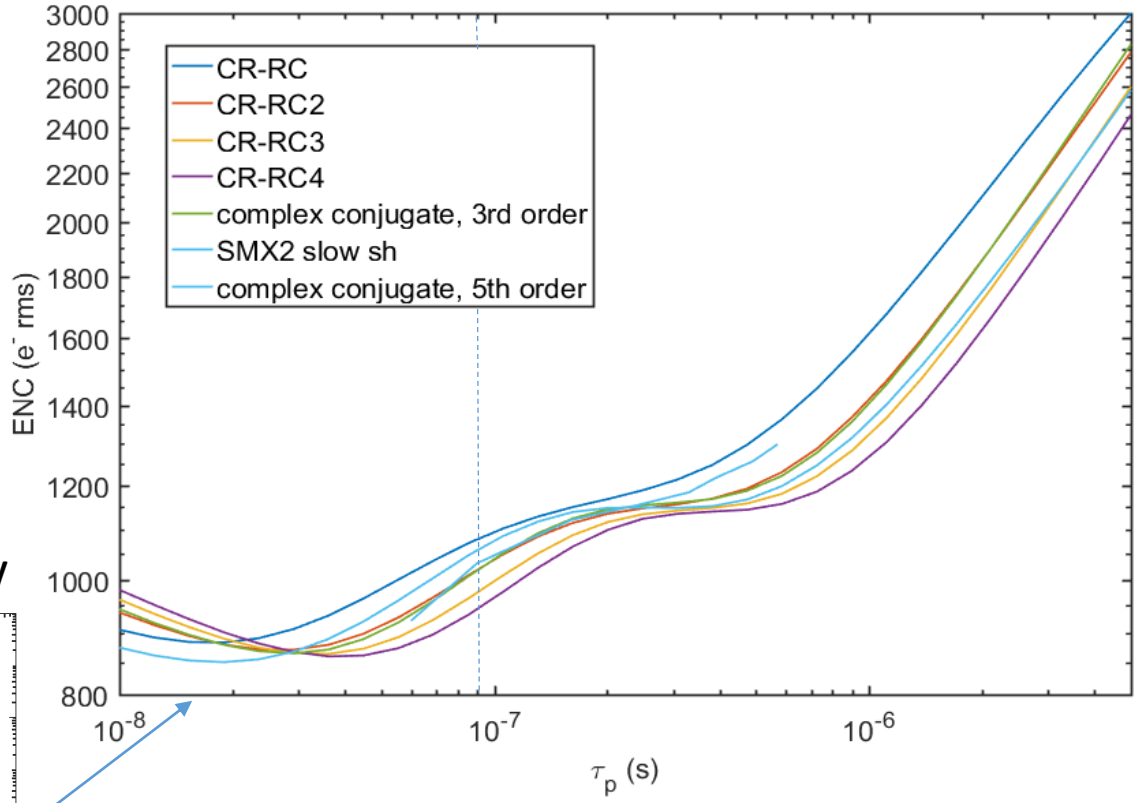
b)



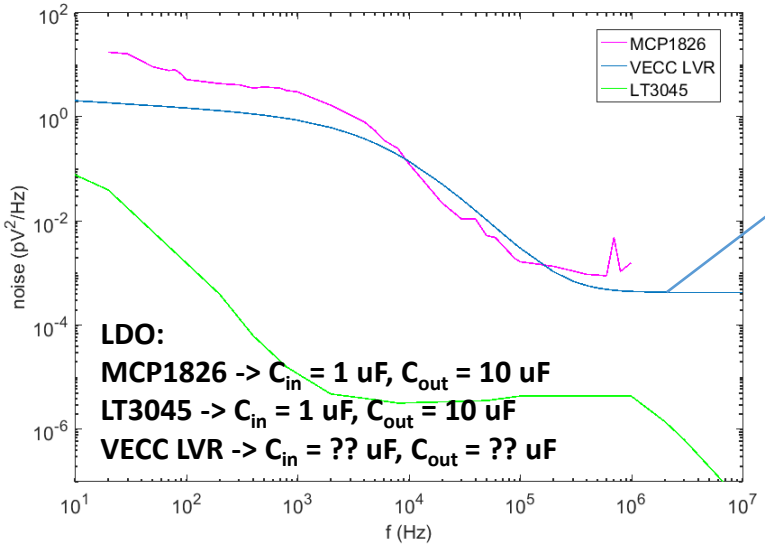
Simulations results with LDO – various shapers

- LDO noise model (VECC LVR),
- R_{fb} noisy,
- ESD attached,
- detector model (detector length 4 cm, cable length 49 cm),
- interconnect series resistances,
- detector leakage 5 nA.

ENC (e^- rms) vs. peaking time

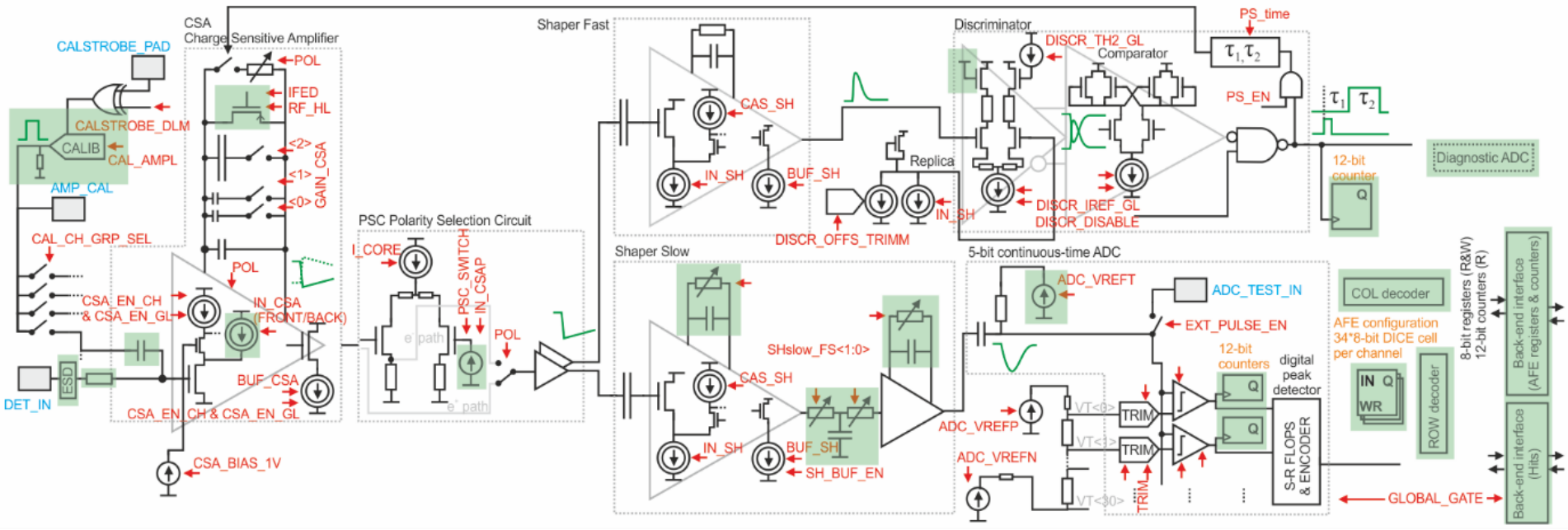


Output Noise Voltage Density vs. Frequency



According to simulation results power supply lines inside the chip filter the supply noise to only a small excent, which is not noticeable in the output noise level.

Noise sources – SMX2 chip example



Noise-related changes:

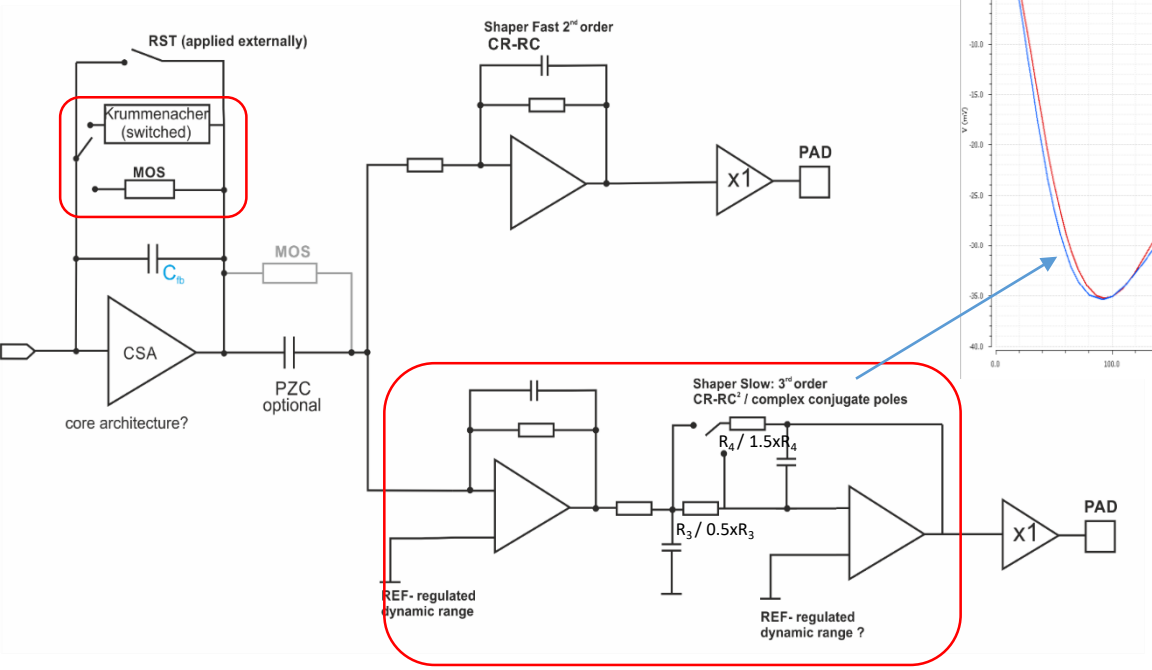
- Add 3pF decoupling capacitor at PSC reference in each channel
- Fix even/odd problem by adding decoupling pad
- Make sure biasing resistance of sensors is enlarged > 5 Mohm
- Minimize series resistance of pad-to-CSA connection (10, 25 Ohm)
- Remove ESD protection and extend power lines

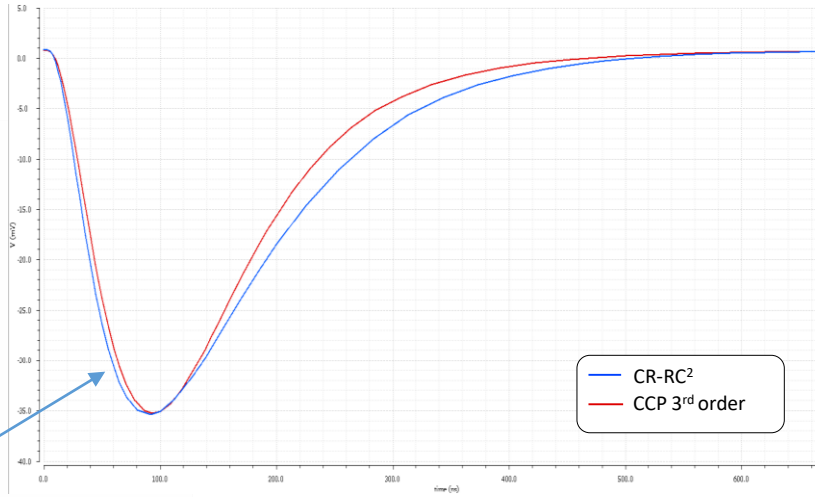
New channel architecture

(UMC180, mini@sic, run:july 2018)

1.5x1.5 mm
6-8 channels
4 single-ended, 4 differential
digital interface for configuration

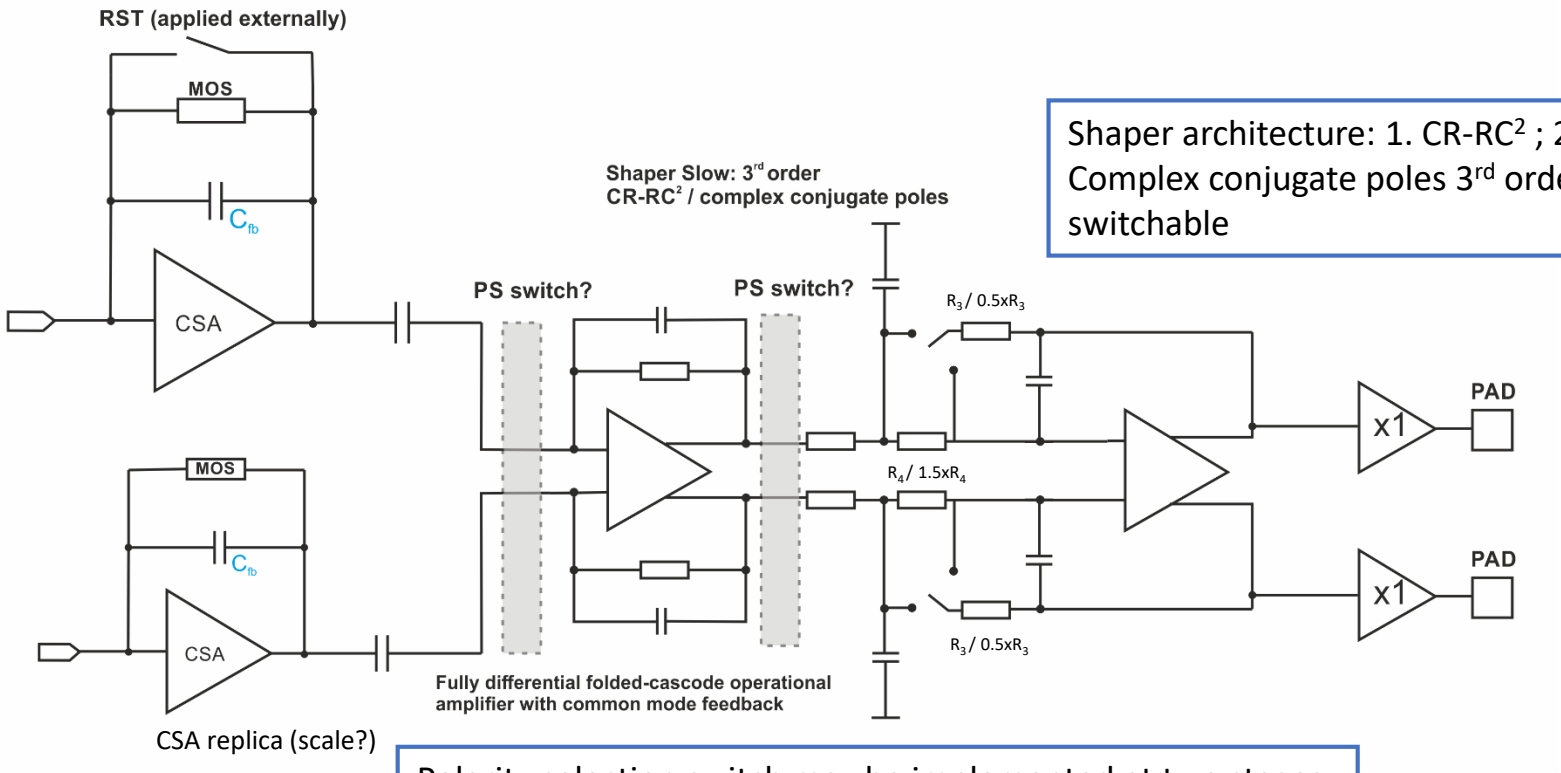
Key features:
- Eliminate PSC (inverting stage): equalize noise for both polarities
- Switchable shaper architectures:
  - Complex conjugate poles (3rd order)
  - Improved CR-RC^2 architecture
- Pseudo-differential architecture to reject power supply noise and digital interference (next slide)





Slow shaping amplifier:
- gain: ~36 mV/fC
- peaking time: ~90 ns

Channels' architecture – (pseudo-)differential



Shaper architecture: 1. CR-RC^2 ; 2. Complex conjugate poles 3rd order, switchable

Polarity selection switch may be implemented at two stages: 1. before the shaping amplifier; 2. after first stage of the shaping amplifie

Optionally: adding a digital register generating noise to check system immunity to substrate noise induced by digital part switching activity.

Eliminate power supply noise (LDOs contribution quite high!)

Conclusions

- There are multiple contributors to the total noise of a detection system.
- The total preamplifier input related noise (ENC) depends also on the total input capacitance, peaking time and weighting coefficients (shaping amplifier transfer function).
- Proper selection of the shaping amplifier architecture and peaking time value can decrease the total output noise by a few tens of electrons.
- The more severe effect on the total noise can be attributed to the power supply noise.
- CMRR of the pseudo-differential shaping stage can prove useful in rejecting power supply & digital –related noise sources at the cost of power|noise penalty.

Thank you for your attention.

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