Noise Performance Analysis for the Silicon Tracking System Detector and Front-End Electronics

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Brief intro: Silicon Tracking System in the CBM experiment.

Motivation.

Sources of noise in a detection system.

Impact of shaping amplifiers and preamplifier on noise.

Noise reduction options.

MiniASIC architecture proposals.

Summary.
CBM experiment, GSI, Darmstadt, Germany

**Aim:** creation of the highest baryon densities in nucleus-nucleus collisions for the exploration of the properties of the super-dense nuclear matter. Exploration of the QCD phase diagram in the region of very high baryon densities.

**STS metrics:**
- >1 790 000 channels
- >14 000 ASICs
- 1752 FEBs
- 600 ROBs
- 78 DPBs

**STS (Silicon Tracking System) detector**
Particles’ track and momentum determination
Interaction rate 10 MHz
Silicon strip detectors

**Read-out electronics** at the perimeter of the detection stations (FEB : 8 chips/board) + data concentrator (based on GBTx)
multi-line micro-cables-> sensors’ read-out
double-sided, micro-strip sensors, 1024 CH/side, 7.5° stereo angle, 58 μm strip pitch

**MUCH (Muon Chamber) detector**
Gaseous detector (GEM)

The STS/MUCH-XYTER2 (SMX2):
- developed at AGH University Cracow
- 10 mm × 6.8 mm, 288 pads
- 128 readout channels + 2 test channels
- Power: 1.1 – 1.3 W per chip
- 5-bit continuous-time ADC + 14-bit Timestamp
- Range of operation: 0-15 fC (STS)
- 250 kHit/s/channel (fast reset enabled)
- 9.41-47 Mhit/s/chip

**Total ENC:** < 1000 e⁻ rms in system
- Power: <10 mW / channel
- CSA gain: 10 mV/fC
- SH_slow gain: 35 mV/fC
- SH_fast gain: 75 mV/fC
- Peaking time (slow path): 90 ns
- Peaking time (fast path): 40 ns

**FEB (Front-end Board):**
- 8 ASICs - read-out of a single side of 1024 strip sensor
- Rad-hard LDOs (VECC India)
- AC-coupling of SLVS e-links
Motivation

ENC vs Cdet

- many noise sources in the system;
- can be divided between intrinsic (contributed by the input amplifier itself) and extrinsic (originating in the sensor and biasing network).
Noise sources in the detection system

1. parallel current noise:
   - detector leakage current shot noise ($I_L$),
   - detector bias shunt resistance $R_{bias}$,
   - leakage current flowing through transistors in the Electrostatic Discharge (ESD) protection circuit,
   - current thermal noise from feedback resistance.

2. series white noise:
   - input transistor thermal noise ($M_{1th}$),
   - various series resistors’ (sensor’s metal strip, cable, interconnect on-chip) thermal noise.

3. series 1/f (or flicker) noise:
   - CSA input transistor flicker (1/f) noise ($M_{1f}$).
Noise at CSA output - detailed considerations

- all devices forming the core amplifier and its feedback network contribute to the overall noise,
- usually only a few of them have a noticeable impact on the total ENC

Input transistor layout to reduce noise from the gate and the bulk resistance.

A. Rivetti
“CMOS Front-end Electronics for Radiation Sensors”
Noise at CSA output - detailed considerations

\[ P_{av,\text{out}} = <y(t)^2> = \int_{-\infty}^{\infty} S_{xx}(f) |H(f)|^2 df \]

Parallel, Current Noise

\[ <v_{out}^2>_ni = \frac{i_n^2 R_f}{4 C_f} \]

\[ \int_{0}^{\infty} \frac{1}{(1+s\tau_f)(1+s\tau_r)} \left| \frac{1}{1+s\tau_f}(1+s\tau_r) \right|^2 df = \frac{1}{4(\tau_f + \tau_r)} \approx \frac{1}{4\tau_f} \]

\[ <v_{out}^2>_ni = \frac{i_n^2 R_f}{4 C_f} \rightarrow i_n = 2qI_L \]

\[ ENC_i^2 = \frac{i_n^2 R_f C_f}{4 q^2} \rightarrow ENC_i = \sqrt{\frac{I_L \tau_f}{2q}} \]

\[ ENC_i = \frac{1}{q} \sqrt{k_B T C_f} \]

- \( \tau_f \) – falling time, related to the CSA feedback capacitor discharge time constant
- \( \tau_r \) - rising time, related to the CSA bandwidth (~40 ns for the CSA GBW ~9 GHz) -> the input of the CSA bandwidth has no strong impact on the ENC

Preferably, the total noise is limited to the one produced by the input transistor. The noise introduced by other devices can be neglected.
Noise at CSA output - detailed considerations

Series, Voltage Noise => convert to current by

White series

\[
\left< v_{out}^2 \right>_{nw} = \frac{v_{nw}^2 R_f^2 C_T^2}{4 R_f^2 C_T^2 C_f g_{m1} C_f} \int_0^\infty \frac{j2\pi f}{(1+j2\pi f \tau_f)(1+j2\pi f \tau_r)} \frac{1}{df}
\]

\[
< v_{out}^2 >_{nw} = v_{nw}^2 C_T R_f \left( \frac{g_{mb1}}{g_{m1}} \right)^2
\]

\[
v_{nw1, bulk} = 4k_B T R_B \left( \frac{g_{mb1}}{g_{m1}} \right)^2
\]

\[
ENC_w = \frac{1}{q} \sqrt{\gamma k_B T \frac{C_T C_f}{C_f C_L}}
\]

1/f series noise

\[
\left< v_{out}^2 \right>_{nf} = \frac{K_f}{C_{ox} W_1 L_1} \left( \frac{R_f C_f g_{m1} C_f}{C_T C_L} \right) \ln \left( \frac{\tau_f}{\tau_r} \right)
\]

\[
ENC_f = \frac{1}{q} \sqrt{\frac{K_f}{C_{ox} W_1 L_1}} \sqrt{\ln \left( \frac{R_f C_f g_{m1} C_f}{C_T C_L} \right)}
\]

- CSA output noise related to input in ENC is strongly dependent on the CSA transfer function
- The noise spectral density at CSA output is dependent on the total input capacitance (including detector capacitance), feedback capacitance and CSA load capacitance.
**Noise contributors**

![Pie chart showing components of the current noise](image1.png)

- **$R_{bias}$** 50%  
- **IESDn** 15%  
- **Idet** 7%  
- **Rbias** 15%

**Figure 1:** Components of the current noise.

<table>
<thead>
<tr>
<th>Source</th>
<th>Typ. value</th>
<th>Used for calc.</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{bias}$</td>
<td>500 kΩ - 1.5 MΩ</td>
<td>1.5 MΩ</td>
</tr>
<tr>
<td>$I_{det}$</td>
<td>1 - 8 nA/cm</td>
<td>4 nA</td>
</tr>
<tr>
<td>$I_{ESDn}$</td>
<td>1 - 10 nA</td>
<td>9 nA</td>
</tr>
<tr>
<td>$I_{ESDP}$</td>
<td>1 - 10 nA</td>
<td>9 nA</td>
</tr>
<tr>
<td>$R_{fb}$</td>
<td>5 MΩ - 30 MΩ</td>
<td>20 MΩ</td>
</tr>
<tr>
<td>$R_{Al}$</td>
<td>10.5 Ω/cm</td>
<td>42 Ω</td>
</tr>
<tr>
<td>$R_{cable}$</td>
<td>0.635 Ω/cm</td>
<td>12.7 Ω</td>
</tr>
<tr>
<td>$R_{inter.}$</td>
<td>10 Ω - 25 Ω</td>
<td>15 Ω</td>
</tr>
<tr>
<td>$M_{1,th}$</td>
<td>Tech. dep.</td>
<td></td>
</tr>
</tbody>
</table>

**Total noise at shaper’s output:**

$$ ENC^2 = ENC_i^2 + ENC_w^2 + ENC_{1/f}^2 \quad \rightarrow \quad ENC^2 = \tau_p \cdot A_i \cdot i_n^2 + \frac{1}{\tau_p} \cdot v_n^2 \cdot A_w \cdot C_T^2 + A_{1/f} \cdot v_{nf}^2 \cdot C_T^2 $$

where $C_T$ is the total capacitance connected to CSA input: $C_T = C_g + C_{fb} + C_{calib} + C_{DET}$, $A_w$, $A_i$ and $A_{1/f}$ are weighting coefficients for thermal, current and flicker noise respectively (depending on the filter type and order) and $\tau_p$ is the peaking time.

![Pie chart showing components of the voltage noise](image2.png)

**Figure 2:** Components of the voltage noise.

$$ i_n^2 = \frac{4k_B T}{R_{bias}} + \frac{4k_B T}{R_{FB}} + 2ql_{det} + 2ql_{ESDn} + 2ql_{ESDP} $$

Input transistor flicker noise

$$ v_{nw}^2 = 4k_B T R_{Al} + \frac{4}{3} k_B T R_{cable} + 4k_B T R_{inter} + 4k_B T \alpha_w \gamma \frac{1}{g_m} $$

$$ v_{nf}^2 = \frac{k_f}{C_{ox} W L_f} $$

PMOS contribution is 10\* lower.
ENC calculations – shaping amplifier’s output

<table>
<thead>
<tr>
<th></th>
<th>$A_w$</th>
<th>$A_{1/f}$</th>
<th>$A_i$</th>
</tr>
</thead>
<tbody>
<tr>
<td>CR-RC</td>
<td>0.92</td>
<td>3.69</td>
<td>0.92</td>
</tr>
<tr>
<td>CR-RC$^2$</td>
<td>0.85</td>
<td>3.41</td>
<td>0.64</td>
</tr>
<tr>
<td>CR-RC$^3$</td>
<td>0.93</td>
<td>3.32</td>
<td>0.52</td>
</tr>
<tr>
<td>CR-RC$^4$</td>
<td>1.02</td>
<td>3.27</td>
<td>0.45</td>
</tr>
<tr>
<td>CR$^2$-RC</td>
<td>1.03</td>
<td>4.70</td>
<td>1.00</td>
</tr>
<tr>
<td>CR$^2$-RC$^2$</td>
<td>1.16</td>
<td>4.89</td>
<td>0.72</td>
</tr>
<tr>
<td>Complex conjugate poles, 3rd order</td>
<td>0.85</td>
<td>3.39</td>
<td>0.61</td>
</tr>
<tr>
<td>Complex conjugate poles, 5th order</td>
<td>0.96</td>
<td>3.27</td>
<td>0.45</td>
</tr>
</tbody>
</table>

The total noise at shaper’s output containing simplified expressions for each type of noise:

$$ ENC^2 = A_w \frac{1}{\tau_p} \frac{4kT \gamma}{g_m} C_T^2 + A_i K_f C_T^2 + A_i \tau_p [2q(I_{det} + I_{fb}) + \frac{4kT}{R_{bias}} + \frac{4kT}{R_{fb}}] $$

where $g_m$ and $\gamma$ are parameters of the CSA input transistor:

$$ g_m = \frac{I_{DS}}{n \phi_T} f(i_f), \quad f(i_f) = \frac{1}{\sqrt{i_f + 0.5} \sqrt{i_f + 1}}, \quad \gamma = \frac{1}{2} + \frac{1}{6} \frac{i_f}{i_f + 1} $$

**Decisions (ASIC):**
- Minimize $R_{\text{inter}}$ (~50%)
- Remove ESD

**Decisions (Sensor):**
- Minimize Al strip resistance
- Maximize $R_{\text{bias}}$ (>5Mohm)

**ASIC:** Weighting coefficients of filters and peaking time can be used for multi-dimensional ENC minimization based on given conditions.
Results – EKV model and simulations

Model of the slow shaper implemented in SMX2 chip.

CR-RC² peaking times

<table>
<thead>
<tr>
<th>$R_{c1}$, $R_{c2}$, $R_1$, $R_2$</th>
<th>$t_p$ for electrons (ns)</th>
<th>$t_p$ for holes (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>200k, 45k, 10k, 10k</td>
<td>90</td>
<td>90</td>
</tr>
<tr>
<td>400k, 90k, 20k, 20k</td>
<td>170</td>
<td>170</td>
</tr>
<tr>
<td>600k, 135k, 30k, 30k</td>
<td>230</td>
<td>230</td>
</tr>
<tr>
<td>800k, 180k, 40k, 40k</td>
<td>310</td>
<td>310</td>
</tr>
<tr>
<td>1M, 225k, 50k, 50k</td>
<td>380</td>
<td>390</td>
</tr>
<tr>
<td>1.2M, 270k, 60k, 60k</td>
<td>460</td>
<td>460</td>
</tr>
<tr>
<td>1.4M, 315k, 70k, 70k</td>
<td>530</td>
<td>530</td>
</tr>
</tbody>
</table>
Simulations results – various shapers architectures

- $R_{fb}$ noisy,
- ESD attached,
- pure capacitance (20 pF),
- detector leakage equal to 0 and 5 nA.

Simulation models of a) the cable and b) the double-sided sensor used for simulations; cable length = 49 cm and sensor length = 4 cm.
Simulations results with LDO – various shapers

- LDO noise model (VECC LVR),
- $R_{fb}$ noisy,
- ESD attached,
- detector model (detector length 4 cm, cable length 49 cm),
- interconnect series resistances,
- detector leakage 5 nA.

Output Noise Voltage Density vs. Frequency

According to simulation results power supply lines inside the chip filter the supply noise to only a small extent, which is not noticeable in the output noise level.
Noise-related changes:
- Add 3pF decoupling capacitor at PSC reference in each channel
- Fix even/odd problem by adding decoupling pad
- Make sure biasing resistance of sensors is enlarged > 5 Mohm
- Minimize series resistance of pad-to-CSA connection (10, 25 Ohm)
- Remove ESD protection and extend power lines
New channel architecture

(UMC180, mini@sic, run: july 2018)

Key features:
- Eliminate PSC (inverting stage): equalize noise for both polarities
- Switchable shaper architectures:
  - Complex conjugate poles (3\textsuperscript{rd} order)
  - Improved CR-RC\textsuperscript{2} architecture
- Pseudo-differential architecture to reject power supply noise and digital interference (next slide)

1.5x1.5 mm
6-8 channels
4 single-ended, 4 differential digital interface for configuration

Slow shaping amplifier:
- gain: \(~36\text{ mV/fC}\)
- peaking time: \(~90\text{ ns}\)
Channels’ architecture – (pseudo-)differential

Shaper architecture: 1. CR-RC\(^2\); 2. Complex conjugate poles 3\(^{rd}\) order, switchable

Polarity selection switch may be implemented at two stages: 1. before the shaping amplifier; 2. after first stage of the shaping amplifier

Optionally: adding a digital register generating noise to check system immunity to substrate noise induced by digital part switching activity.

Eliminate power supply noise (LDOs contribution quite high!)
Conclusions

- There are multiple contributors to the total noise of a detection system.
- The total preamplifier input related noise (ENC) depends also on the total input capacitance, peaking time and weighting coefficients (shaping amplifier transfer function).
- Proper selection of the shaping amplifier architecture and peaking time value can decrease the total output noise by a few tens of electrons.
- The more severe effect on the total noise can be attributed to the power supply noise.
- CMRR of the pseudo-differential shaping stage can prove useful in rejecting power supply & digital–related noise sources at the cost of power/noise penalty.
Thank you for your attention.

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