STS-XYTER, a 128 channel readout ASIC for silicon strips

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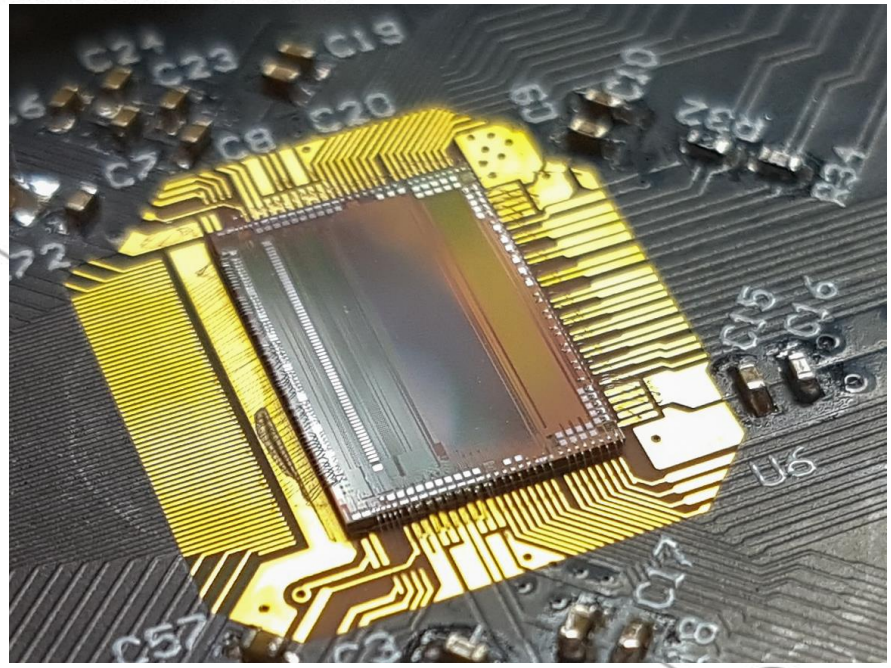
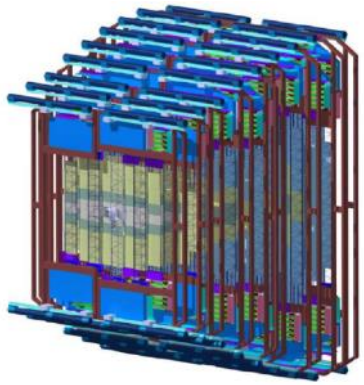
GSI Helmholtzzentrum für Schwerionenforschung, Darmstadt, Germany





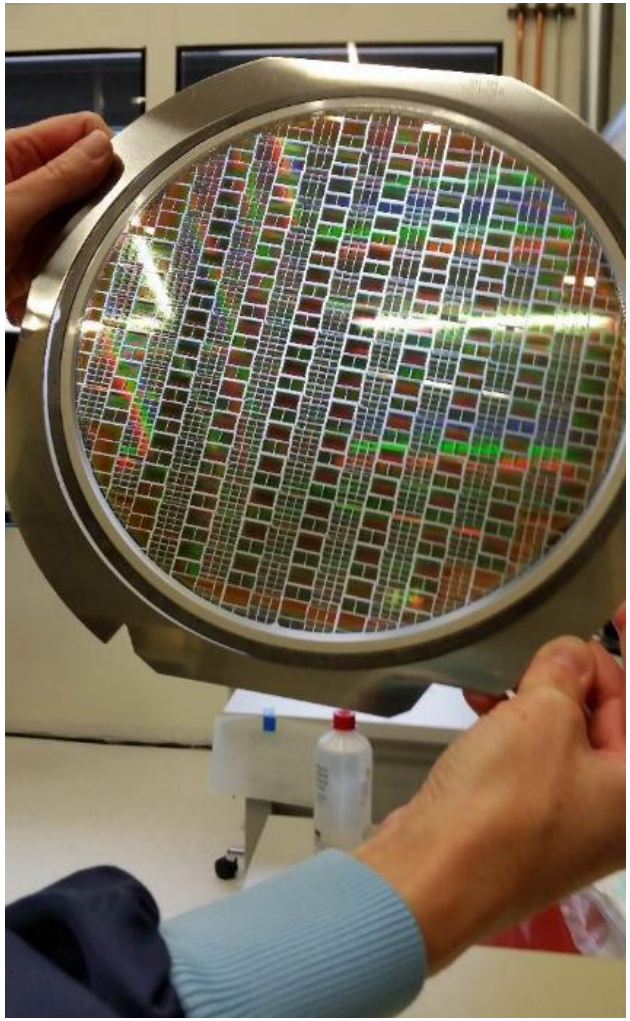
2018 FEE, Jouvence, Canada

Outline

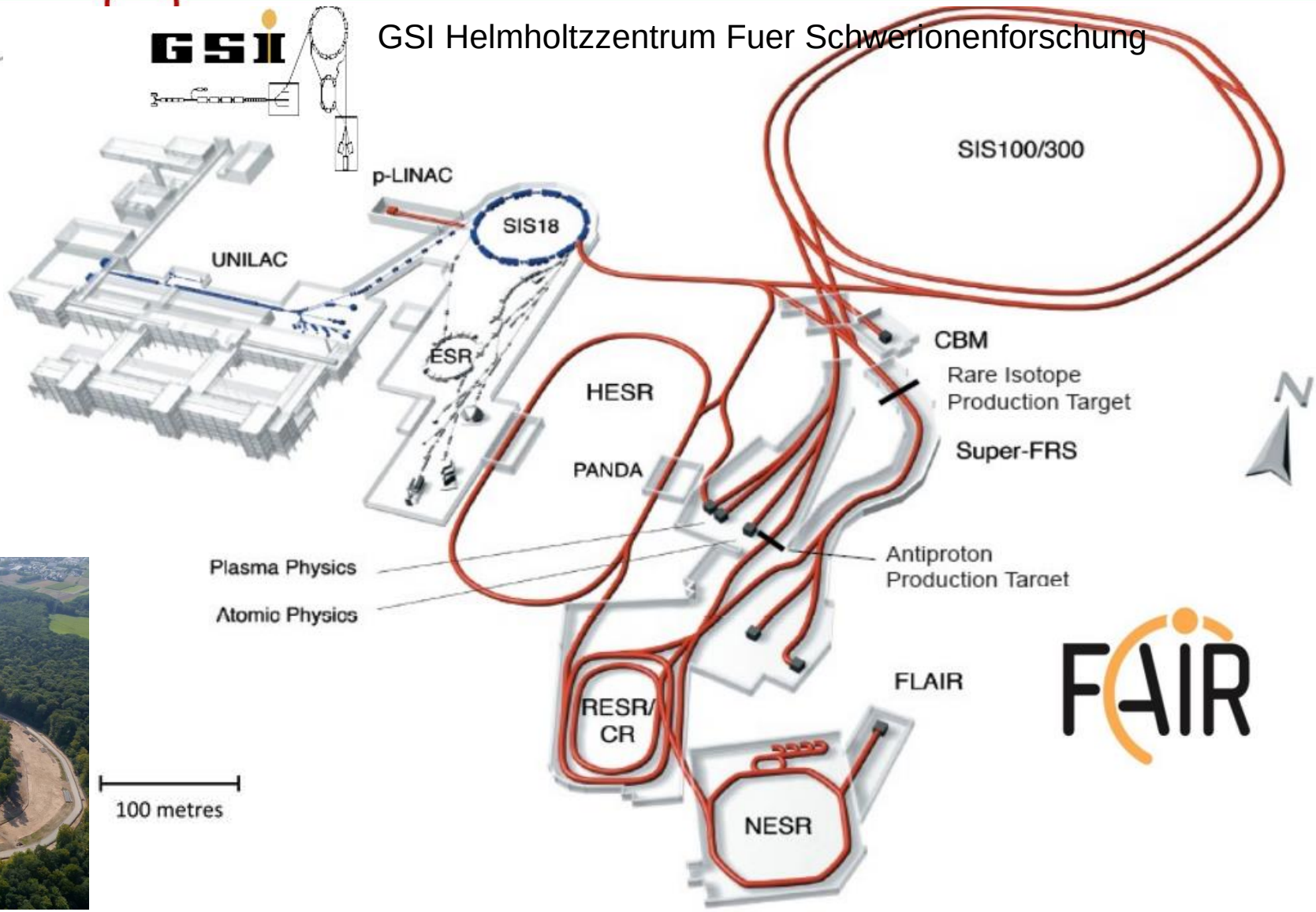
- CBM Experiment, STS & MUCH detectors
- DAQ system

- STS/MUCH-XYTER2 ASIC
  - Analog part
  - Digital read-out (Data flow, Protocol & Interface)

- Measurement results
- Lessons learned
- Summary



GSI Helmholtzzentrum Fuer Schwerionenforschung



under construction
in Darmstadt, Germany

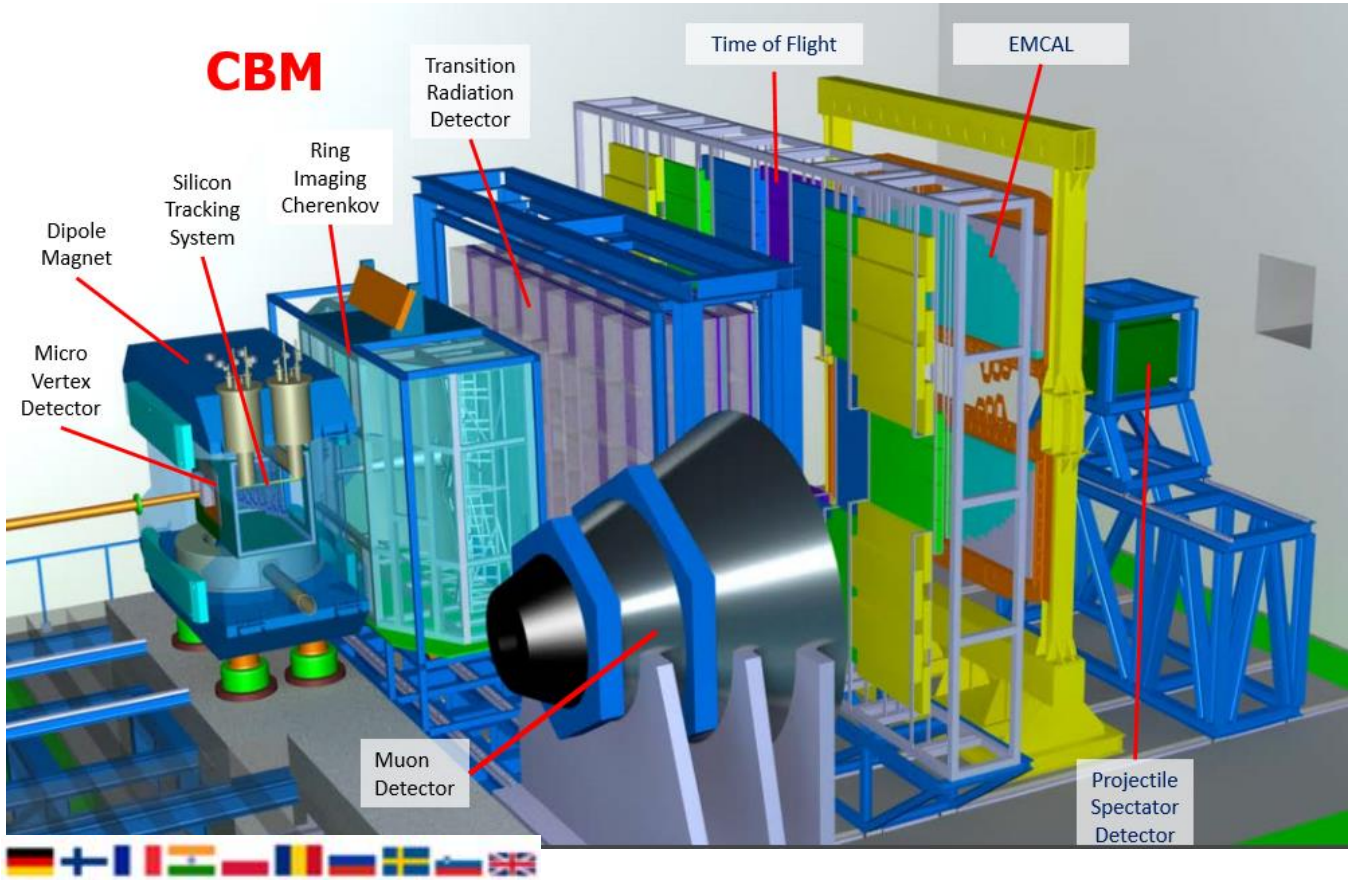
FAIR Facility for Antiproton and Ion Research

The Compressed Baryonic Matter experiment at GSI/FAIR

Aim: Creation of the highest baryon densities in nucleus-nucleus collisions, exploration of the properties of the super-dense nuclear matter.

- up to 10 MHz interactions
- **self-triggering** front-end chip

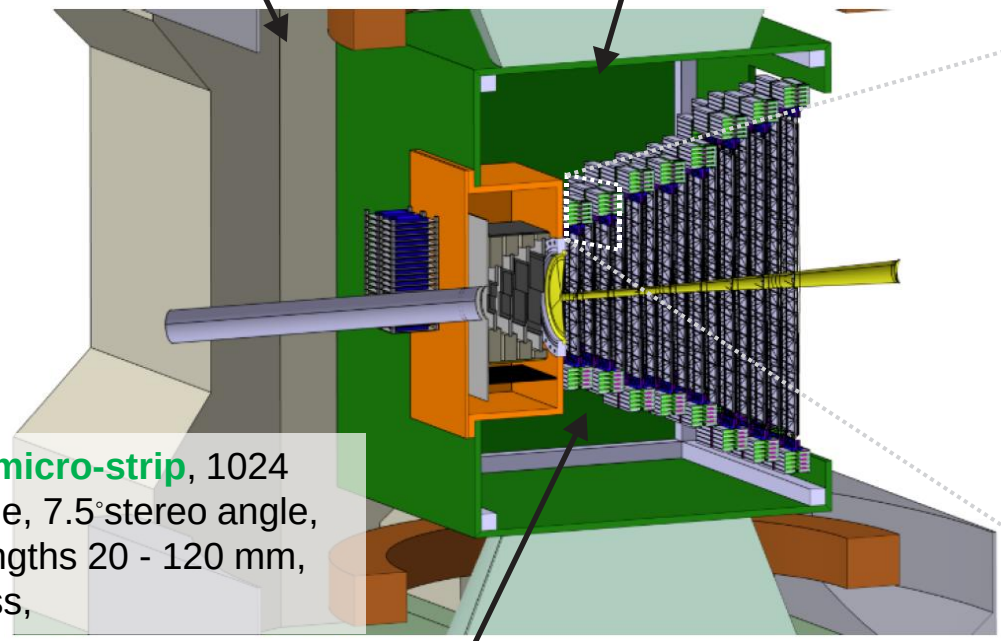
STS: (Silicon Tracking System)
Track reconstruction
and momentum determination
of charged particles in 1T field,
8 detector stations
(30cm – 100 cm from target)



STS metrics:
>1 790 000 channels
>14 000 ASICs
1752 FEBs
600 ROBs
78 DPB s

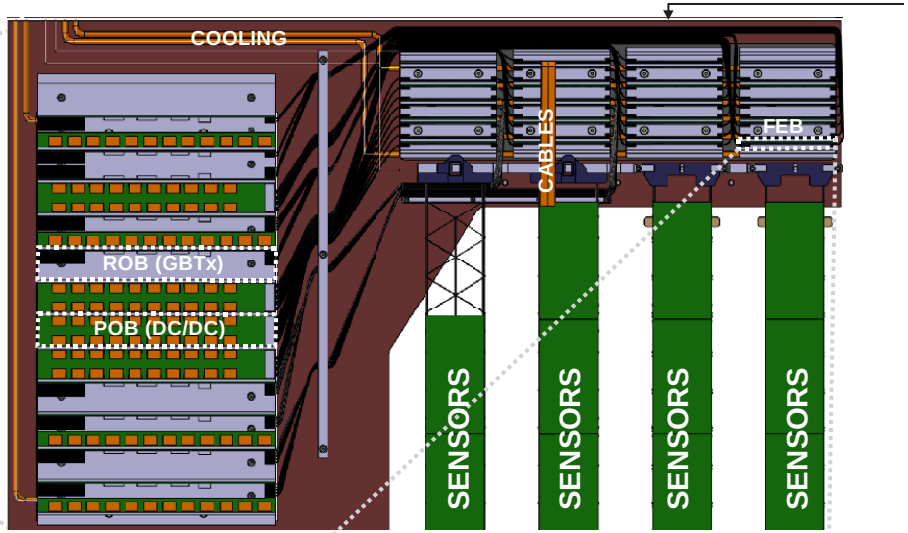
Goal: exploration of the QCD phase diagram in the region of very high baryon densities

STS system - overview

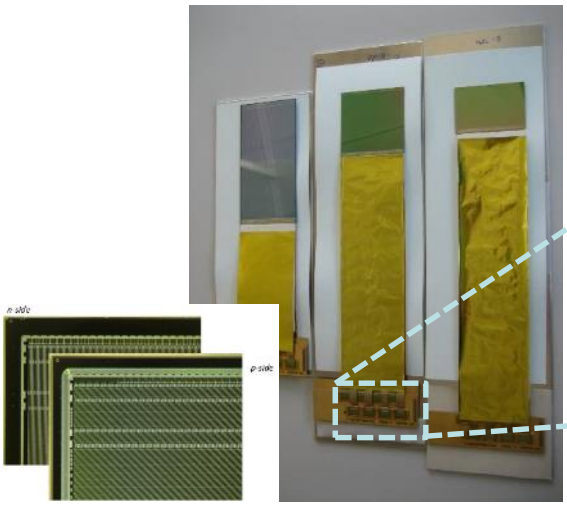


double–sided, micro-strip, 1024 channels per side, 7.5°stereo angle, **58 μm pitch**, lengths 20 - 120 mm, 300 μm thickness,

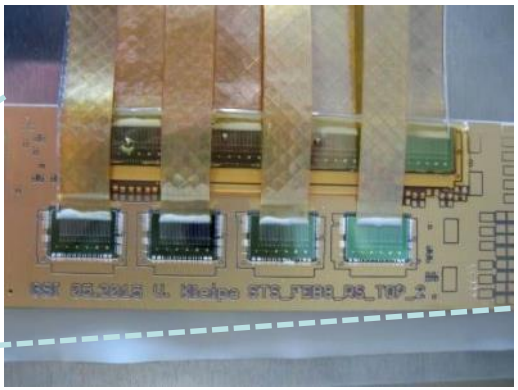
CORNER OF THE SINGLE STATION



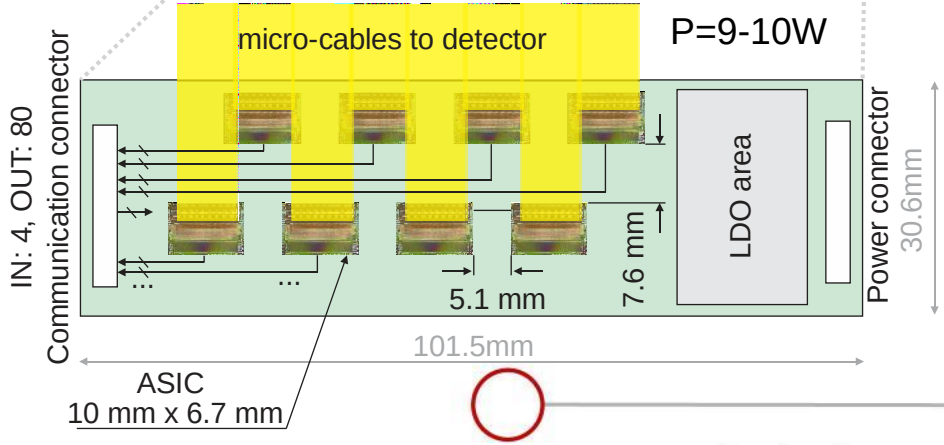
readout electronics located at the perimeter of the detector stations on FEB boards (8 chips/board).



mock-up demonstrator

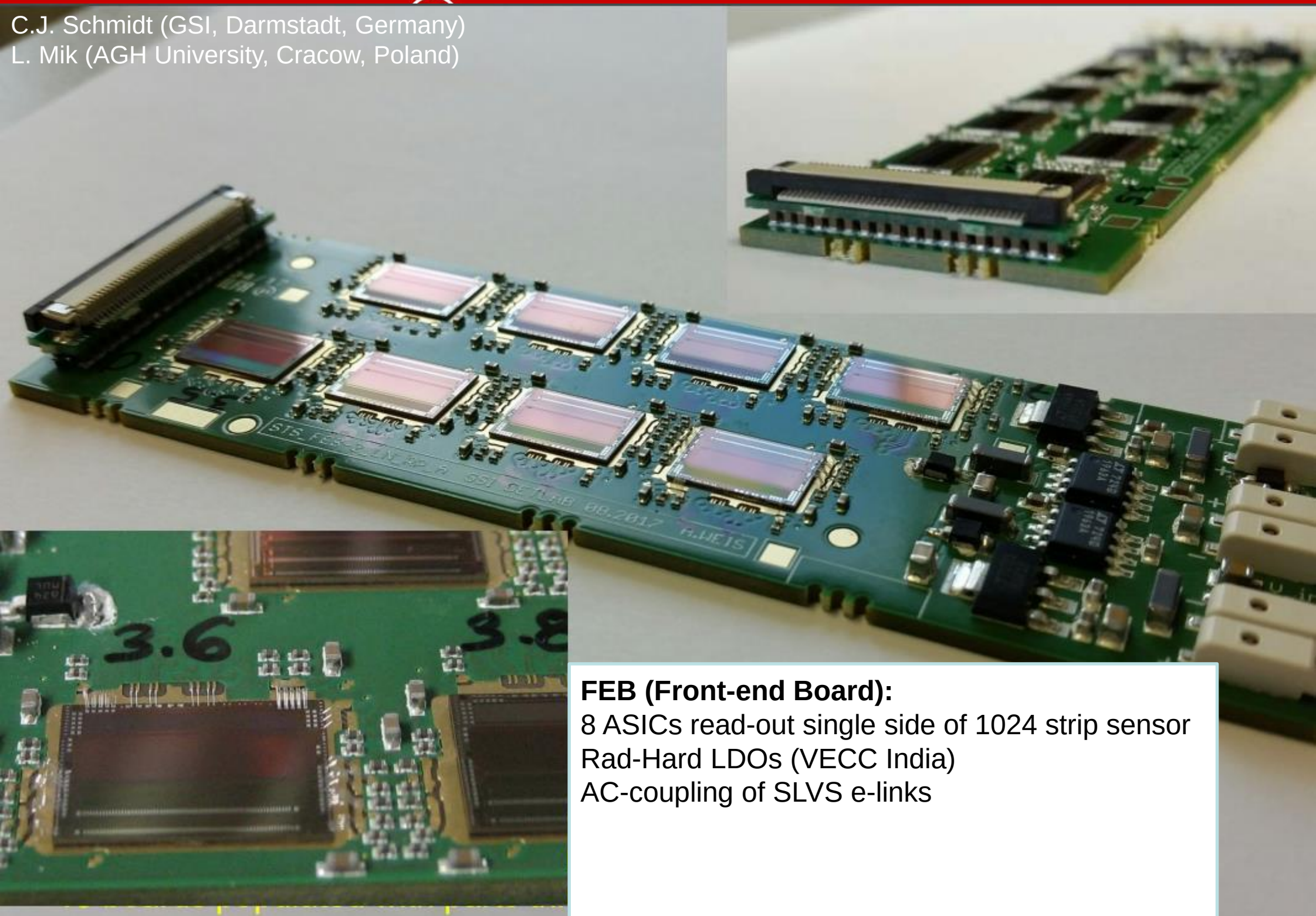


FRONT-END BOARD



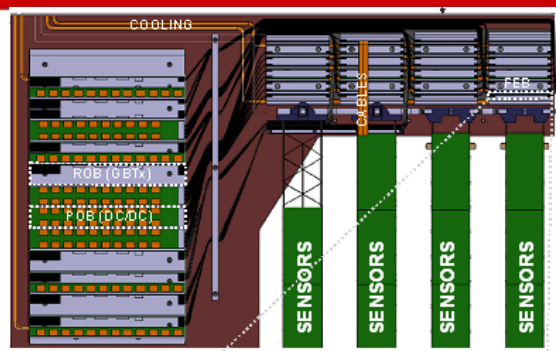
J. Heuser, et al., *GSI Report 2013-4 Technical Design Report for the CBM Silicon Tracking System (STS)*, GSI, Darmstadt, 2013.

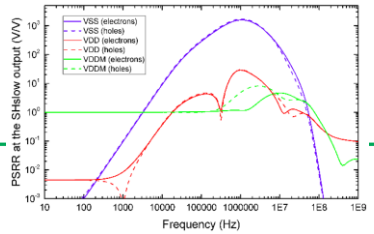
C.J. Schmidt (GSI, Darmstadt, Germany)
L. Mik (AGH University, Cracow, Poland)



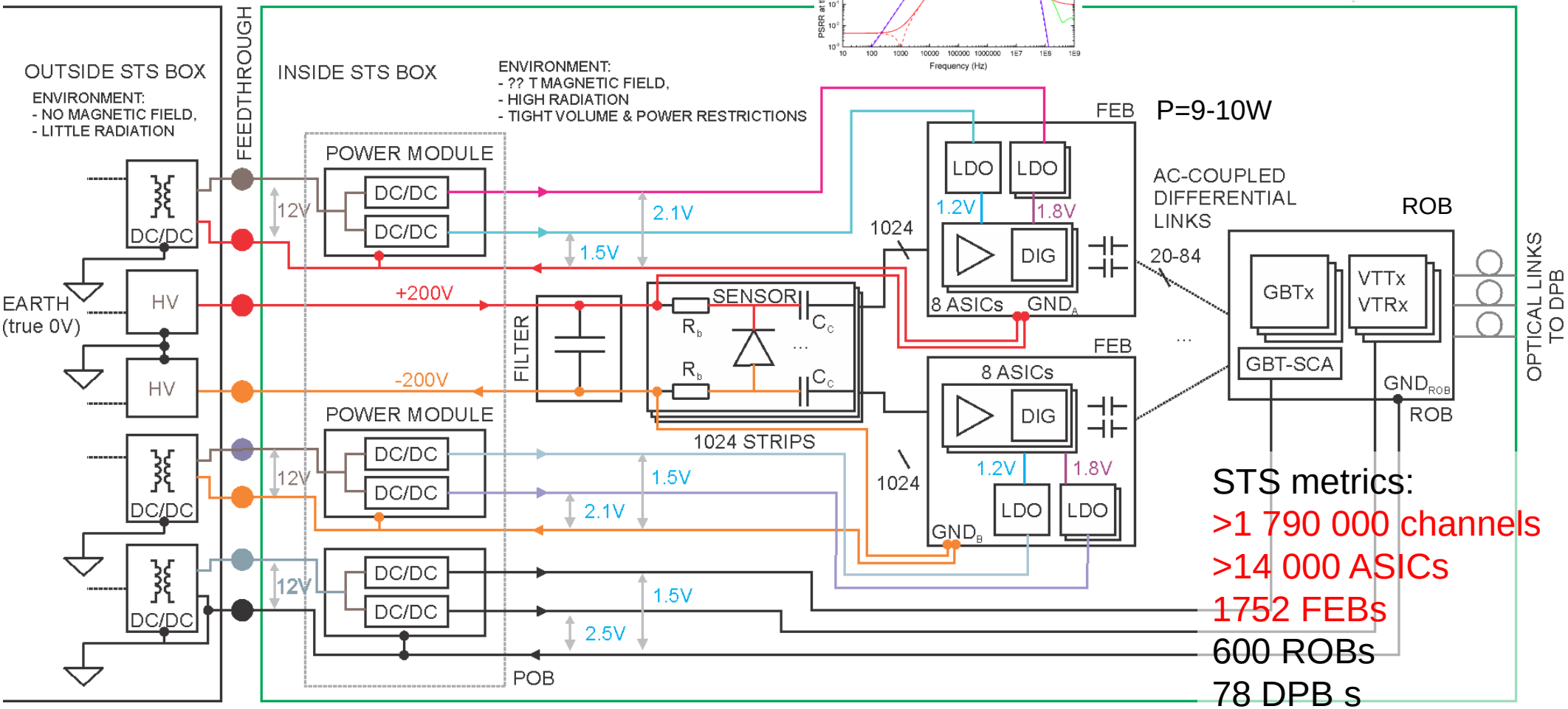
FEB (Front-end Board):
8 ASICs read-out single side of 1024 strip sensor
Rad-Hard LDOs (VECC India)
AC-coupling of SLVS e-links

STS Power & Readout





LOW-VOLTAGE and HIGH-VOLTAGE POWERING SCHEME (SINGLE SENSOR)



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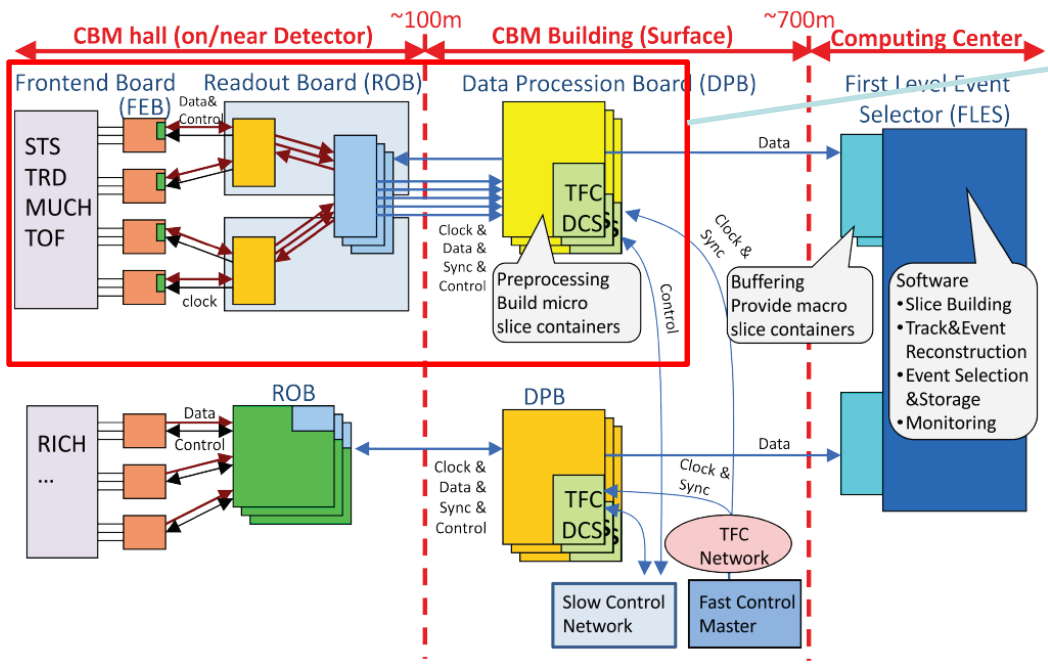
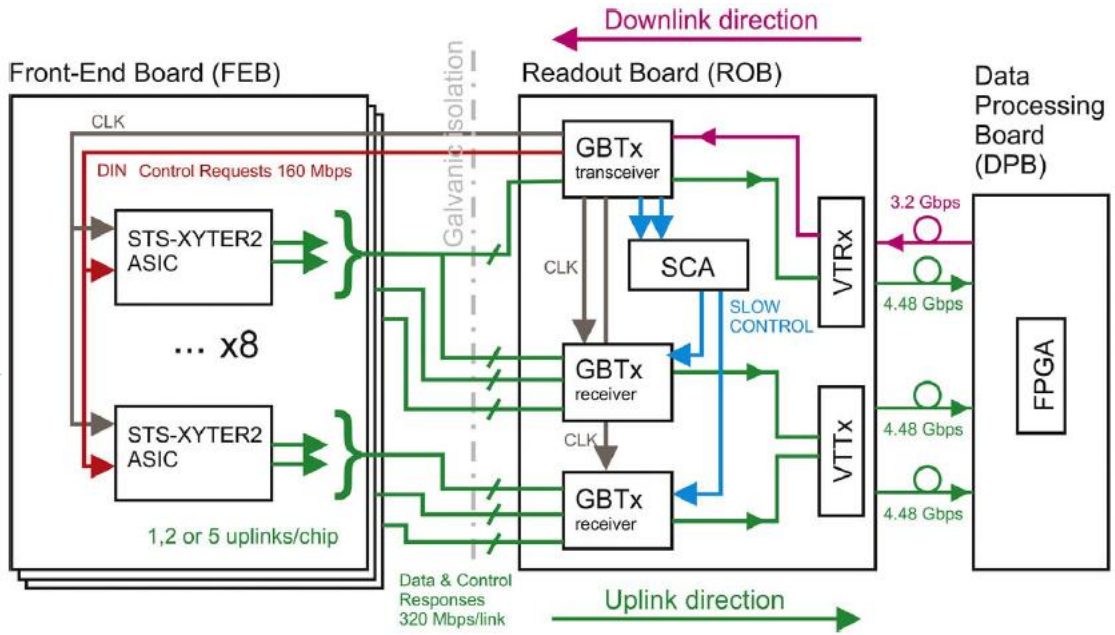
J. Lehnert ; W. F. J. Müller ; C. J. Schmidt;
The GBT-based readout concept for the silicon tracking system of the CBM experiment. Proc. SPIE 9662, 96622S.

DAQ system



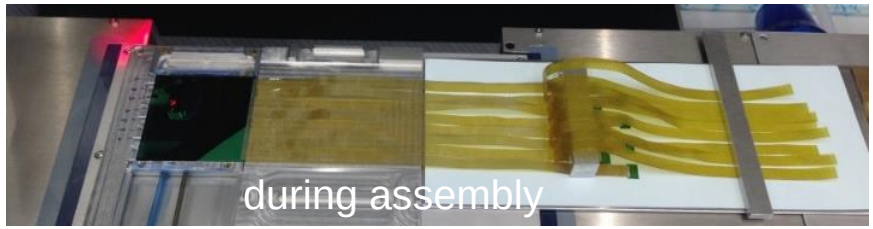


	STS	MUCH station 1,2	TOF	TRD
Technology	silicon strip	GEM	MRPC	TRD
Frontend ASIC	STS-XYTER2 128 channels AGH Cracow	MUCH-XYTER2 64 channels AGH Cracow	GET4 4 channels GSI	SPADIC 32 channels ZITI Univ. Heidelberg
Readout	1 to 5 E-Links (configurable) @320MHz		1 E-Link(compatible) @80 MHz	2 E-Links @320MHz
Configuration, Slow Control, Fast Control	DL: dedicated E-Link shared by ASICs UL: all E-Links, shared with data		DL: control UL: control in data stream	DL: shared E-Link UL: single E-Link shared with data
Clock	phase adjustable clock 160 MHz		external 160MHz clock (tbc)	phase adjustable clock@160 MHz
Channels	1.8 million	249k	100k	245k
No. E-Links DL UL	1.800 20.000	1.944 7.776	25.000 ASIC Links 25.000 ASIC Links	< 7.500 15.000
Versatile Links DL UL	600 1.800	216 648	<=625 <=625	240 1.152

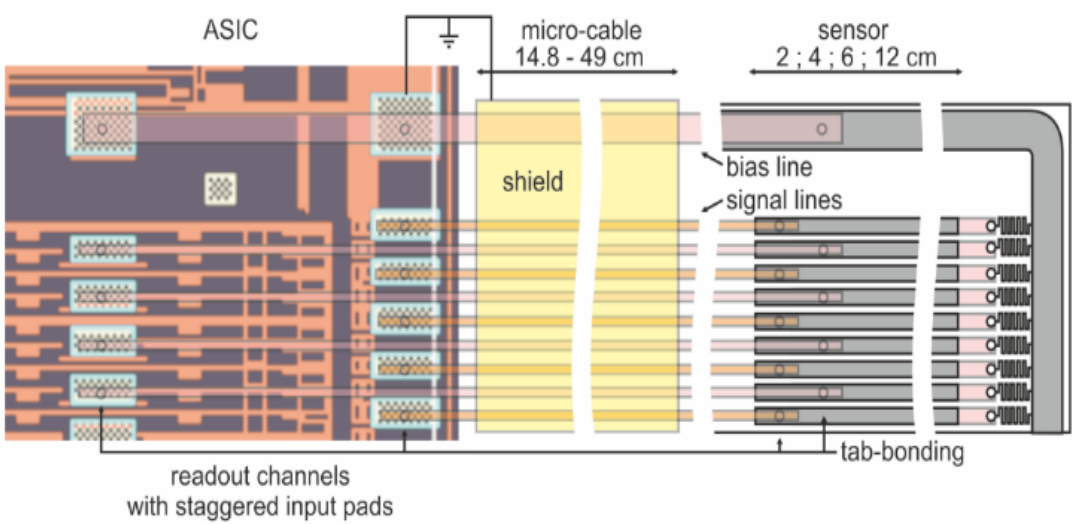
K. Kasinski, P. Koczon, S. Ayet, S. Loechner, C. J. Schmidt; *System-level Considerations of the Front-End Readout ASIC in the CBM Experiment from the Power Supply Perspective*. JINST 2017.

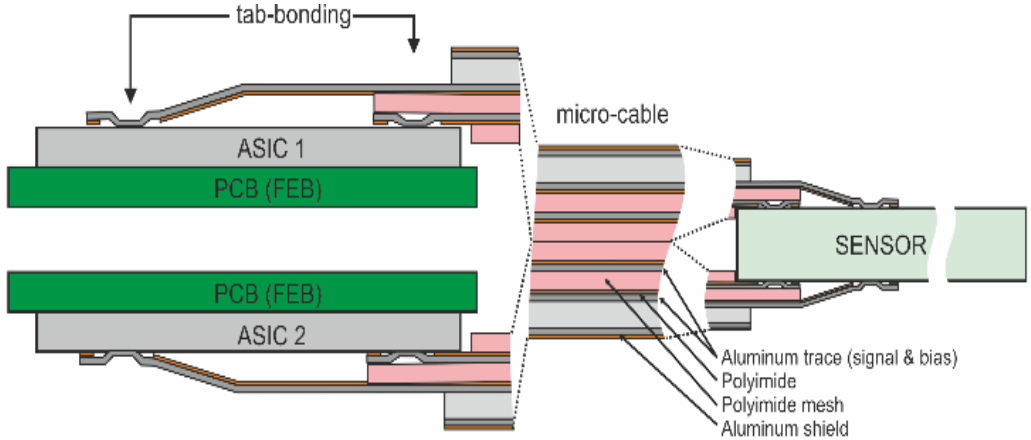
J. Lehnert, A.P. Byszuk, D. Emschermann, K. Kasinski, W.F.J. Müller, C.J. Schmidt, R. Szczygiel, W.M. Zabolotny, GBT based readout in the CBM experiment, JINST 12 (2017) C02061.

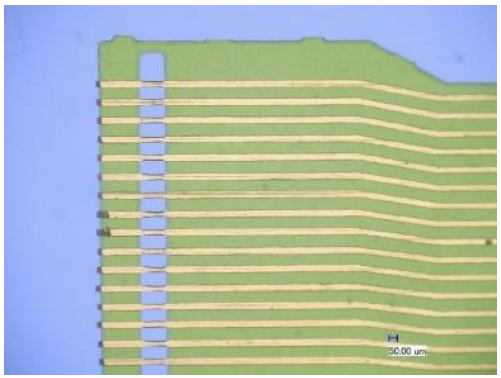
Detector – readout ASICs assemby

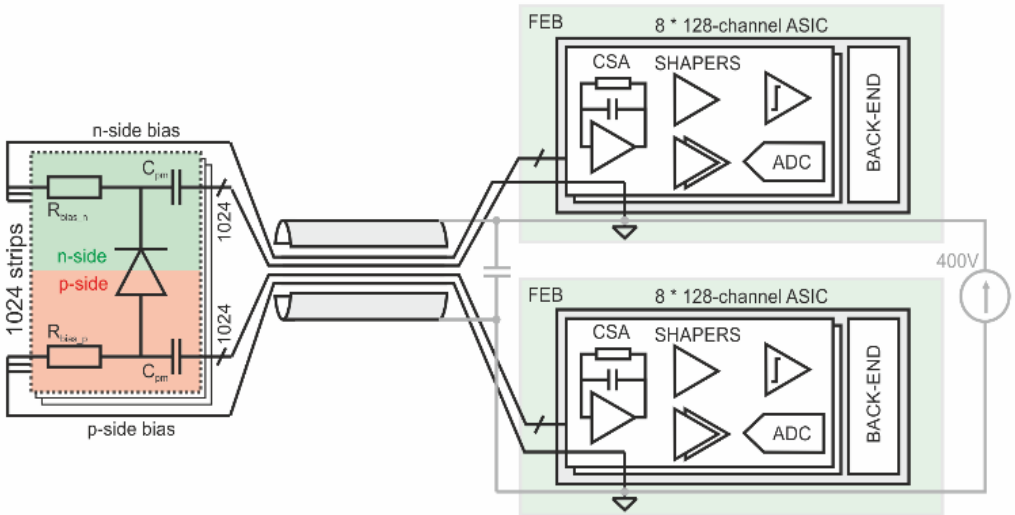


Micro-cable tab-bonded to the ASIC









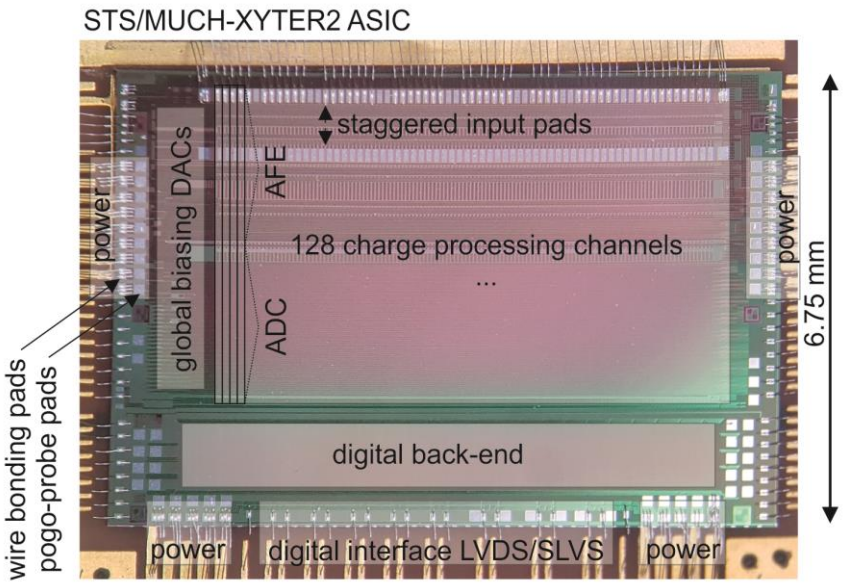
STS & MUCH requirements

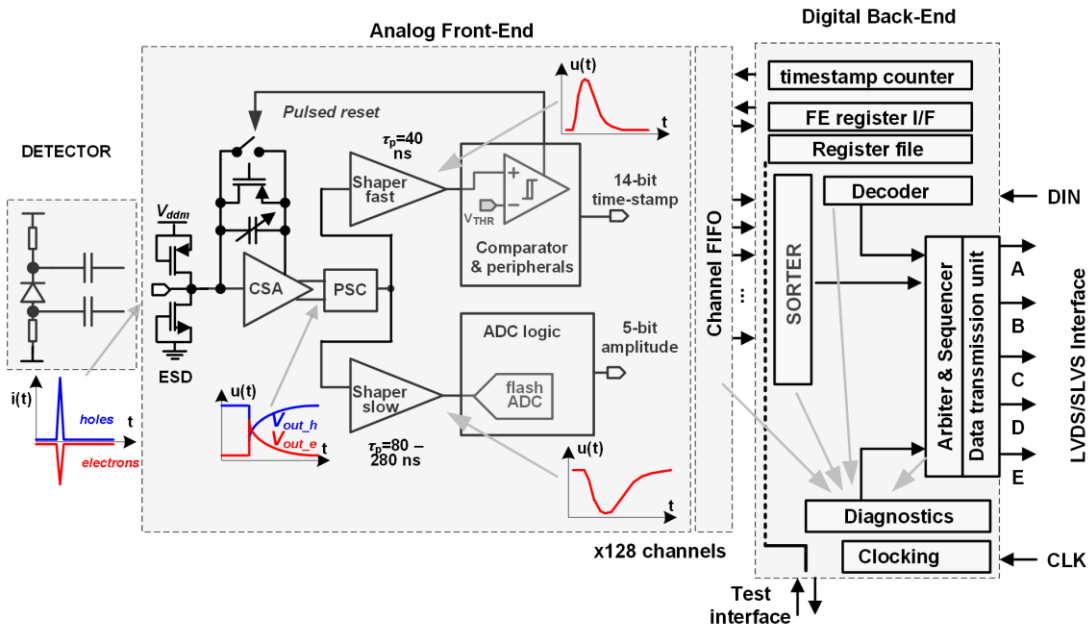
Detector system	STS	MUCH
Sensor type	Silicon microstrip, double-sided, AC-coupled, stereo-angle 7° on n-side, 280 - 320 μm thickness	Gas electron multiplier, 3-foil, trapezoidal GEM sensors
Sensor lengths	2 cm, 4 cm, 6 cm, 12 cm	
Microcable lengths	15 cm - 47 cm	
Expected total capacitance	4-50 pF	up to 50 pF
Hit rate	250 kHz average	up to 2 MHz (in central pads)
Channel pitch	58 μm	116 μm
Power consumption [mW/channel]	< 10	
Dynamic range	0-15 fC 4 fC typical	1-100 fC
Time measurement accuracy	< 10 ns	
Signal polarity	positive, negative	negative
Operating temperature	~ -10 °C	~ 60 °C
Irradiation expected	up to 2 Mrad | 20 kGy	

higher gain (x6) ESD not critical all channels (100% power)	lower gain (x1) ESD critical every 2nd channel (50% power)

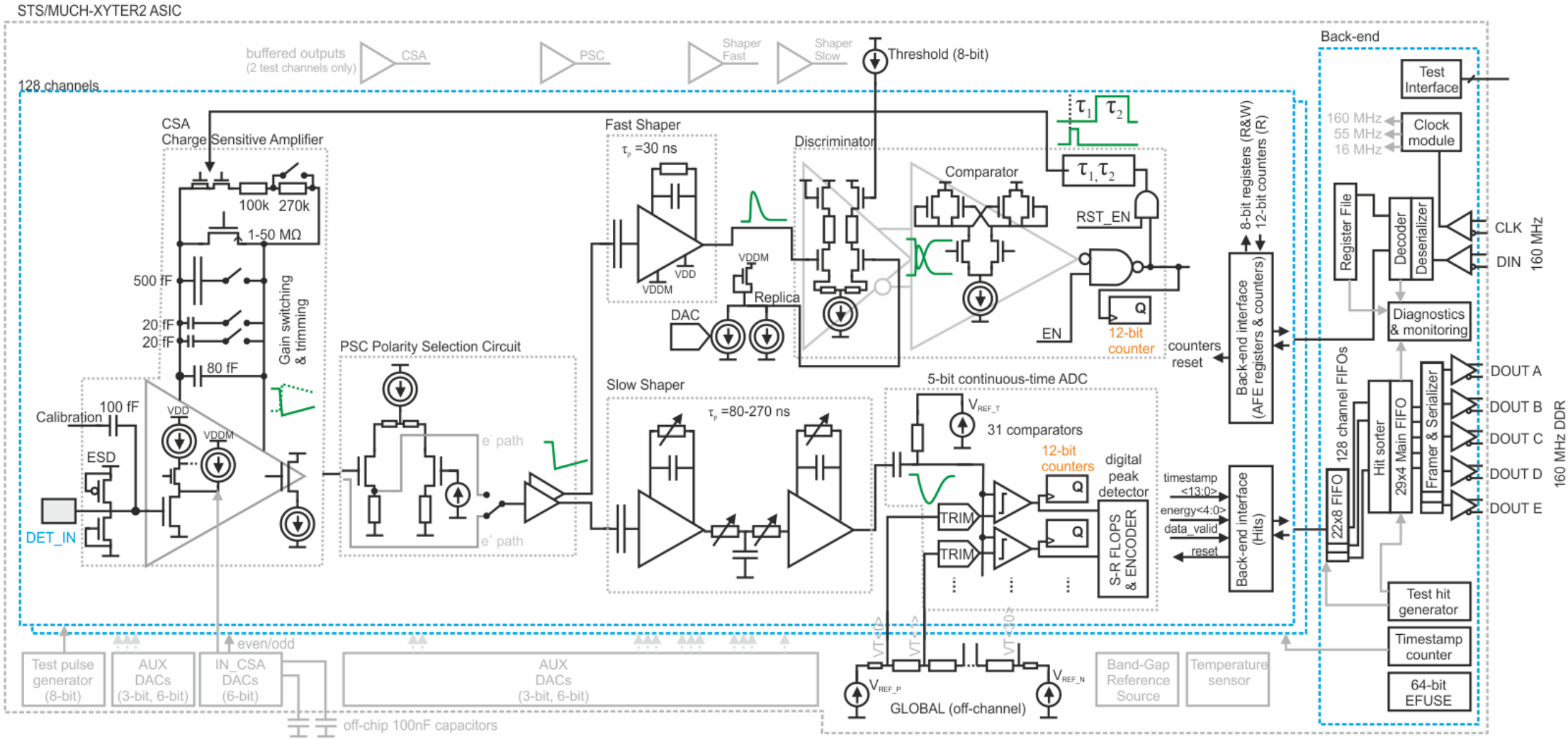
STS: Noise ~ 1000 e- rms

STS/MUCH-XYTER2 - overview





- 128 channels + 2 test channels
- charge sensitive amplifier (continuous+pulsed reset, switchable gains (STS/MUCH) + trim)
- 5-bit amplitude measurement (shaper slow + ADC)
- 14-bit timestamp measurement (shaper fast + leading edge discriminator)



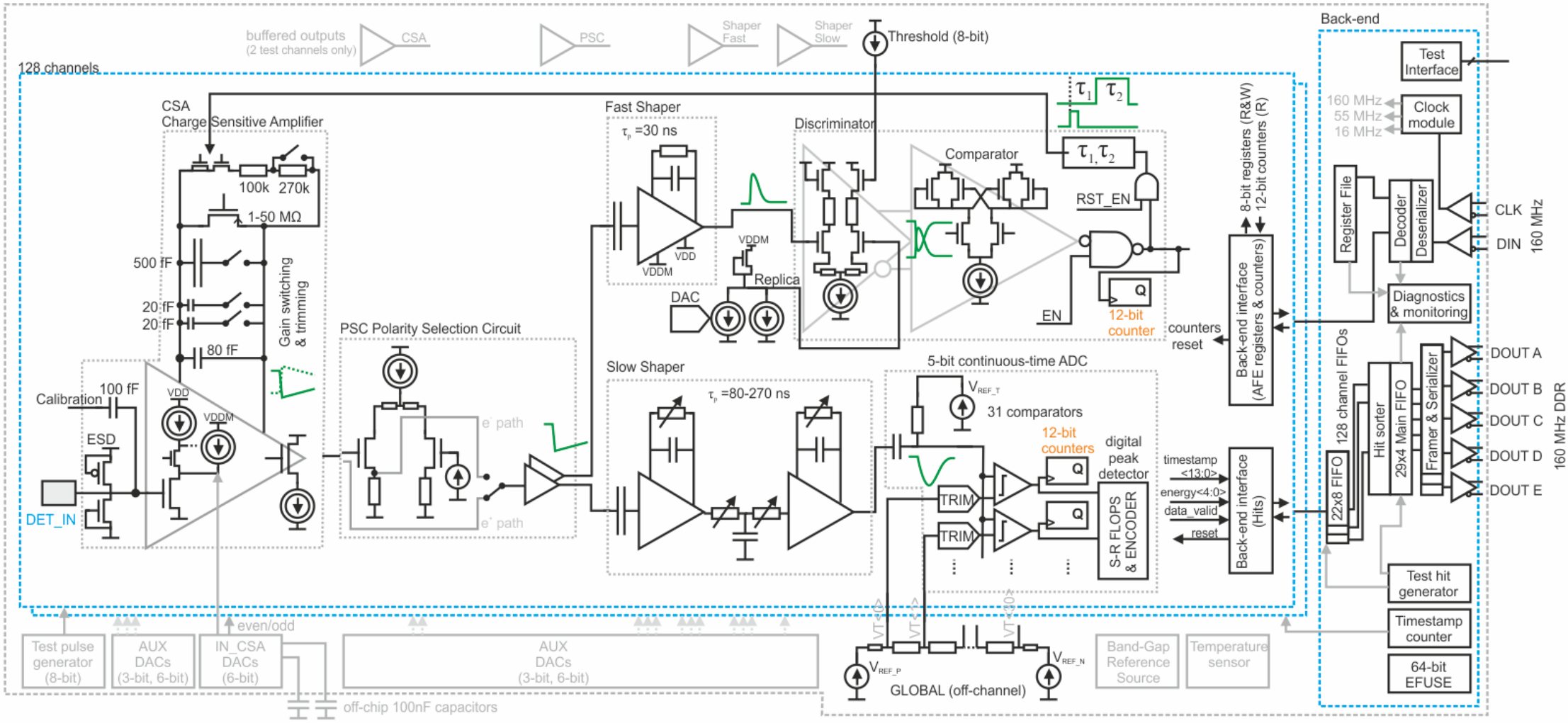
128 channels - time (3.125 ns) & amplitude digitization (5-bit)

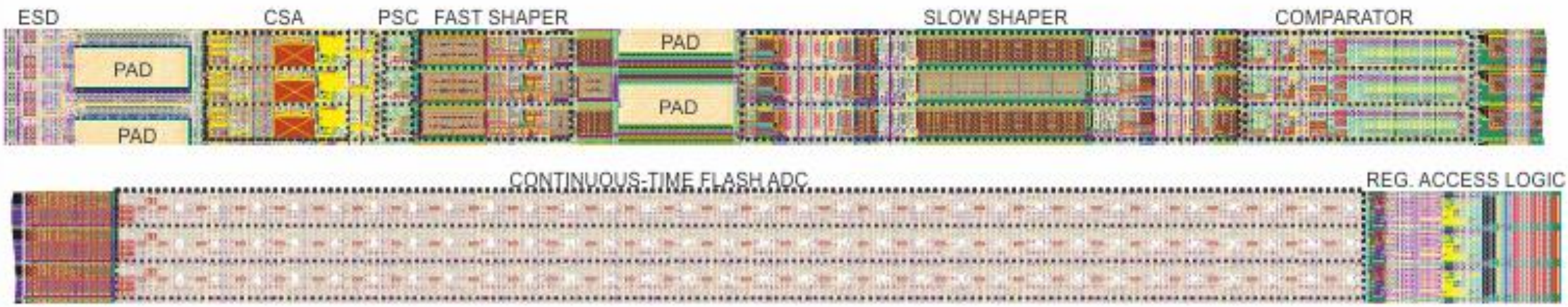
- 0-12 fC electrons & holes (STS)
- gain switching & trimming
- 250 khit/s rate (pulsed reset)
- 80-280 ns shaping time (slow path)
- time-walk corrected offline
- continuous-time ADC + peak det.
- P=8.5-10 mW/channel (incl. logic)

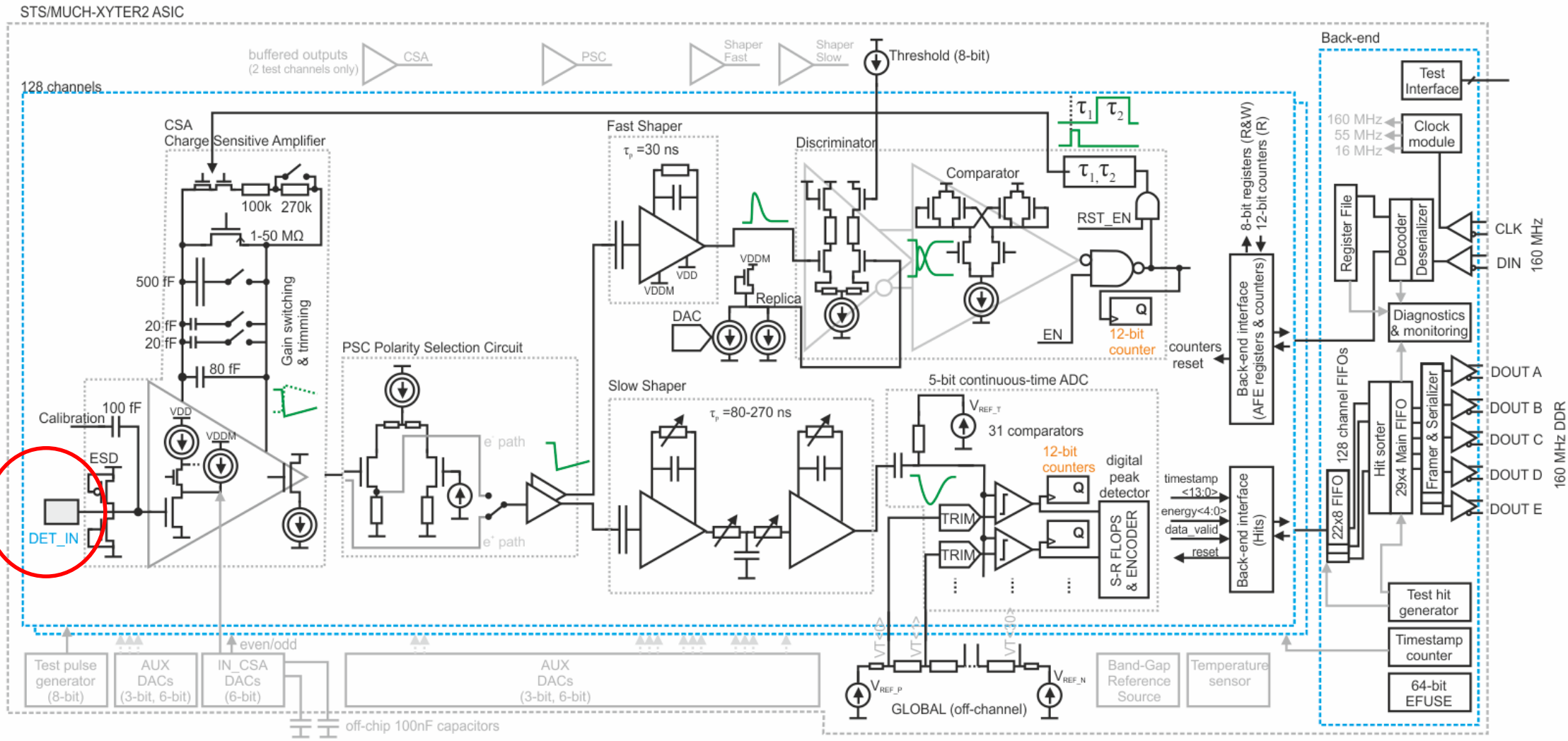
Back-end:

- control via synthesized reg & AFE DICE cells
- 9.41 – 47 Mhit/s/ASIC data BW
- dedicated protocol
- throttling, diagnostic features
- link loopback (multi-level)
- 64-bit e-fuse for traceability

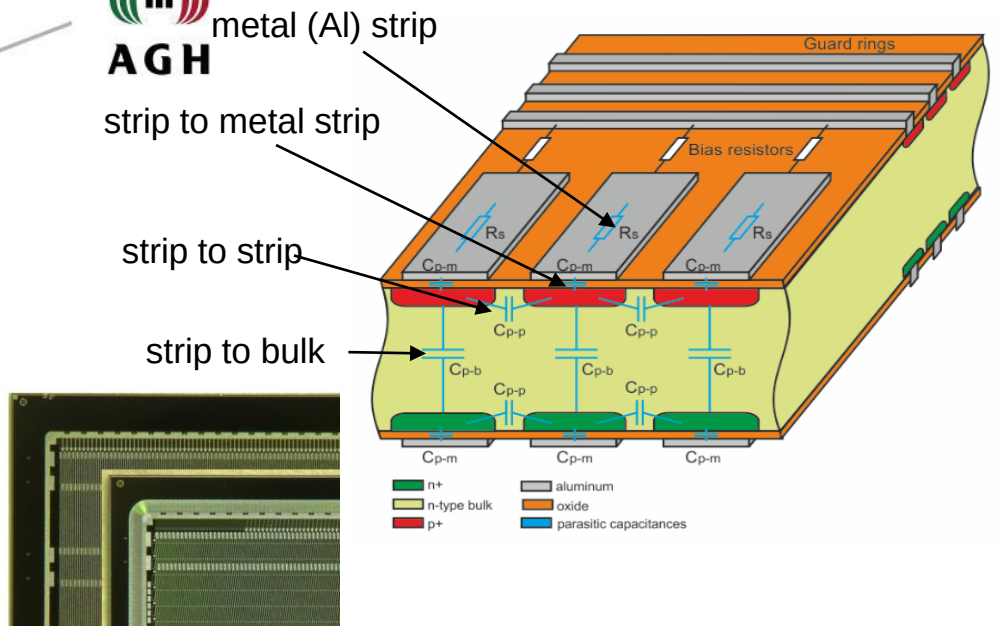
STS/MUCH-XYTER2 ASIC



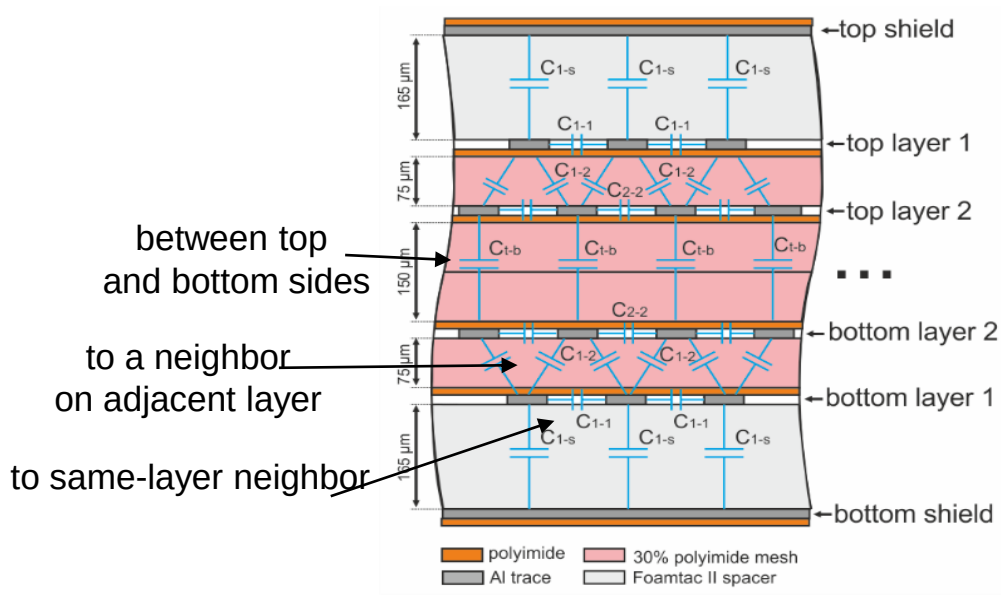



STS/MUCH-XYTER2 ASIC
128 channels
buffered outputs
(2 test channels only)
CSA
PSC
Shaper Fast
Shaper Slow
Threshold (8-bit)
Back-end
Test Interface
160 MHz
55 MHz
16 MHz
Clock module
CSA
Charge Sensitive Amplifier
100k
270k
1-50 MΩ
500 fF
20 fF
20 fF
80 fF
Gain switching & trimming
Calibration
100 fF
ESD
DET_IN
VDD
VDDM
PSC Polarity Selection Circuit
e⁻ path
e⁺ path
Fast Shaper
τp =30 ns
VDD
VDDM
Replica
DAC
Discriminator
Comparator
RST_EN
EN
12-bit counter
Q
counters reset
8-bit registers (R&W)
12-bit counters (R)
Back-end interface (AFE registers & counters)
Register File
Decoder
Deserializer
CLK
DIN
160 MHz
Diagnostics & monitoring
Slow Shaper
τp =80-270 ns
5-bit continuous-time ADC
VREF_T
31 comparators
12-bit counters
digital peak detector
TRIM
S-R FLOPS & ENCODER
timestamp <13:0>
energy<4:0>
data_valid
reset
Back-end interface (Hits)
128 channel FIFOs
22x8 FIFO
Hit sorter
29x4 Main FIFO
Framer & Serializer
DOUT A
DOUT B
DOUT C
DOUT D
DOUT E
160 MHz DDR
Test hit generator
Timestamp counter
64-bit EFUSE
Test pulse generator (8-bit)
AUX DACs (3-bit, 6-bit)
IN_CSA DACs (6-bit)
even/odd
AUX DACs (3-bit, 6-bit)
off-chip 100nF capacitors
VREF_P
VREF_N
GLOBAL (off-channel)
Band-Gap Reference Source
Temperature sensor

Sensor and cable models



Cross section and parasitic capacitances of double-sided detector



Cross section and parasitic capacitances of ultra-light micro-cable assembly

- array of strip-shaped, reverse-biased diodes on a common bulk;
- 1024 strips with 58 µm pitch;
- 7.5º stereo angle on each side;
- thickness - 300 *µ*m;
- lengths - 2, 4, 6 and 12 cm;
- AC coupled (the coupling capacitor formed with the metal strip deposited over a diffusion strip and an isolation layer);

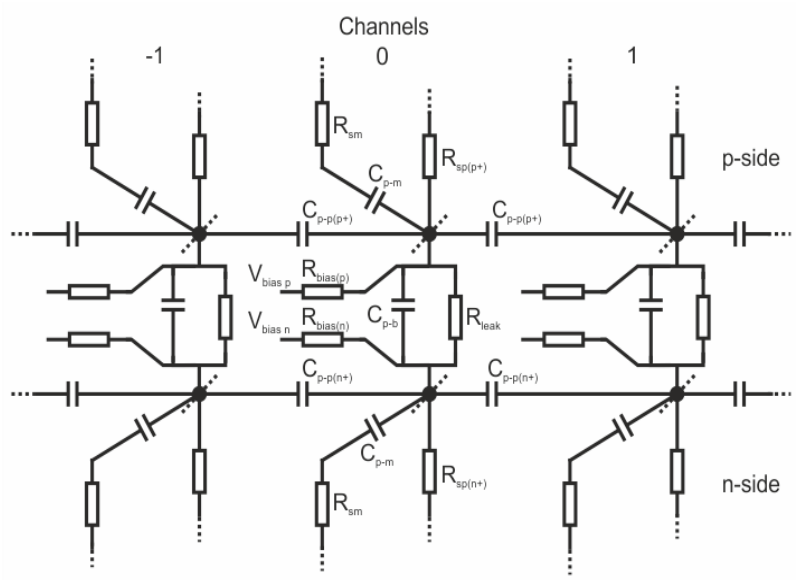
- multi-line micro-cables;
- 128 thin aluminum trace lines;
- 116 µm pitch, 15 µm thickness
- signals' transfer between the sensors and front-end (FE) electronics and for the sensors biasing;
- insulating meshed spacer made from polyimide foil between the layers of cables in a bundle
- shieliding of the stack with four micro-cable layers

Sensor and cable models

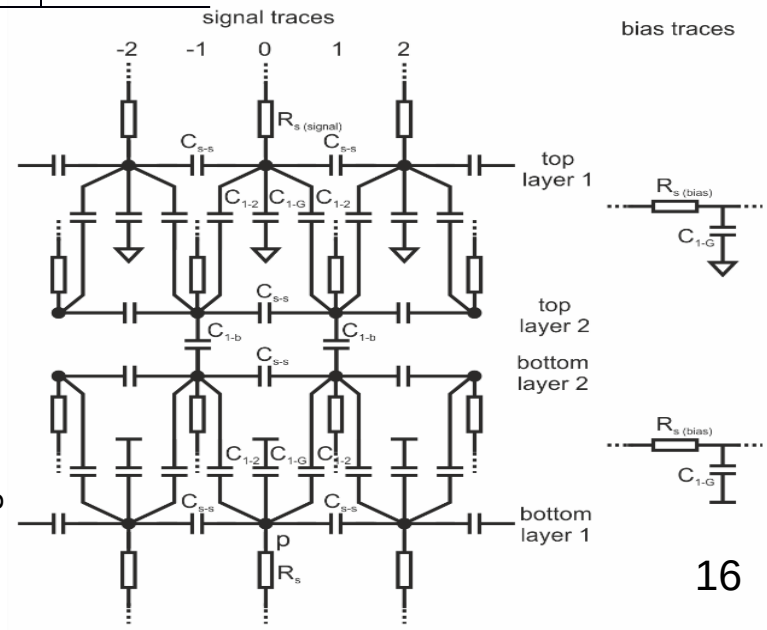
SENSOR			CABLE	
Sensor parameter	**Value**		**Cable parameter**	**Value**
	FAB1	**FAB2**		
strip to strip $C_{p\text{-}p}$ (p+)	0.36 pF/cm	0.43 pF/cm	trace material & dimensions	Al 35 µm × 14 µm
strip to strip $C_{p\text{-}p}$ (n+)	0.37 pF/cm	0.57 pF/cm	capacitance to same-layer neighbor $C_{2\text{-}2}$=$C_{1\text{-}1}$= $C_{S\text{-}S}$	
strip to metal strip $C_{p\text{-}m}$	10 pF/cm	18 pF/cm	capacitance to a neighbor on adjacent layer $C_{1\text{-}2}$	0.119 pF/cm
strip to bulk $C_{p\text{-}b}$	0.18 pF/cm	0.21 pF/cm	to ground plane $C_{2\text{-}G}$	0.139 pF/cm
metal (Al) strip R_{sm}	10.5 Ω/cm	10.5 Ω/cm	to ground plane $C_{1\text{-}G}$	0.38 pF/cm
strip $R_{sp\ (p+)}$	66 kΩ/cm	66 kΩ/cm	trace series resistance R_s (signal)	0.29 pF/cm
strip $R_{sp\ (n+)}$	44 kΩ/cm	44 kΩ/cm	trace series resistance R_s (bias)	0.635 Ω/cm
Bias resistance $R_{bias\ (p\text{-}side)}$	500 kΩ/strip	450 kΩ/strip		0.618 Ω/cm
Bias resistance $R_{bias\ (n\text{-}side)}$	500 kΩ/strip	1700 kΩ/strip		
Sensor thickness	285 µm	320 µm		
Total strip capacitance				
p-side	1.02 pF/cm	1.74 pF/cm	**Total cable capacitance**	0.382 pF/cm
n-side	1.02 pF/cm	1.52 pF/cm		

optimized for
best R & C combination
(incl. yield)
lowest C (selection of dielectric)

Double-sided sensor

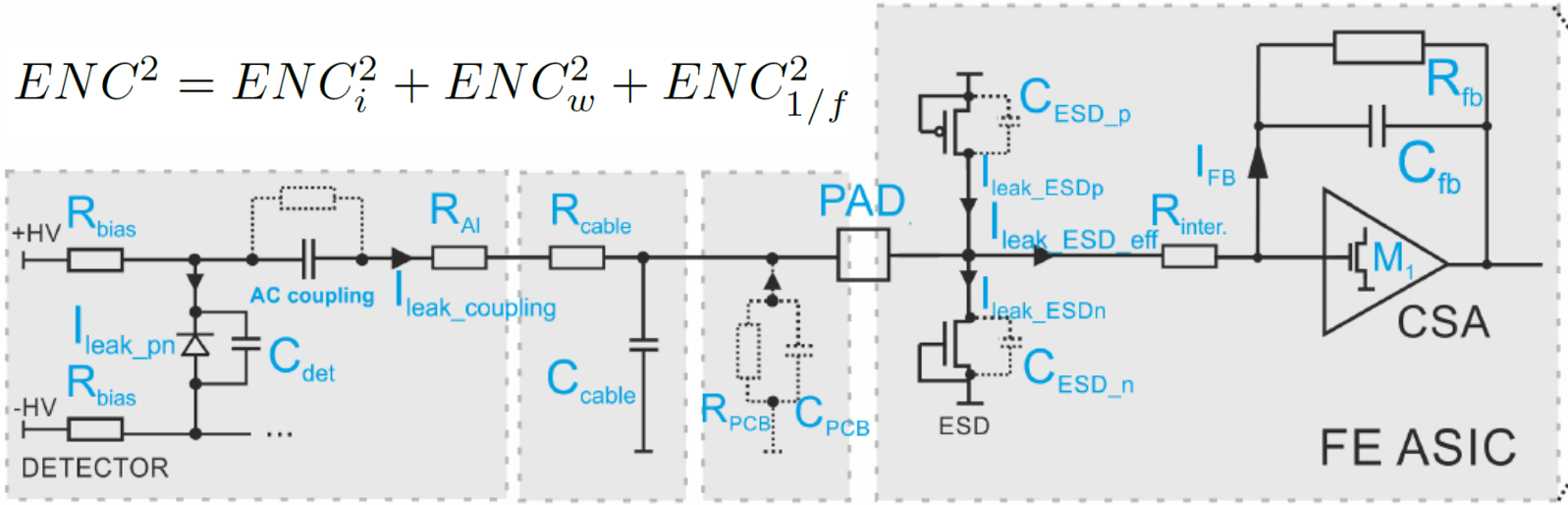


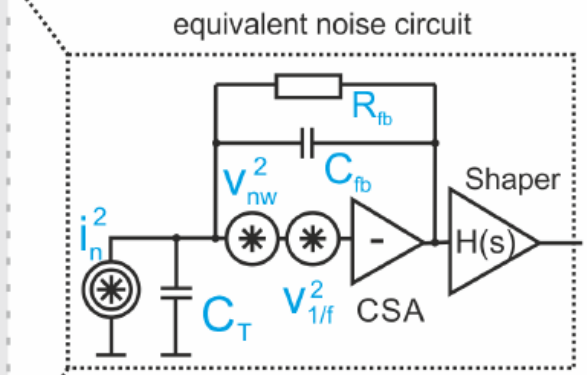
Ultra-light micro-cable



Noise contributors

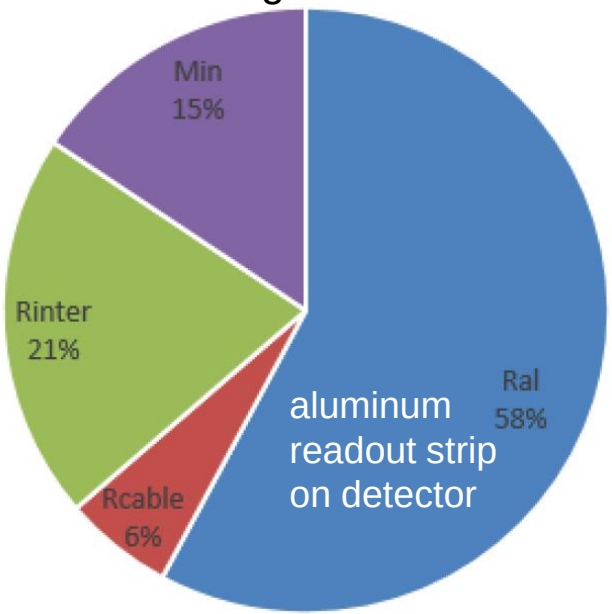
$$ENC^2 = ENC_i^2 + ENC_w^2 + ENC_{1/f}^2$$



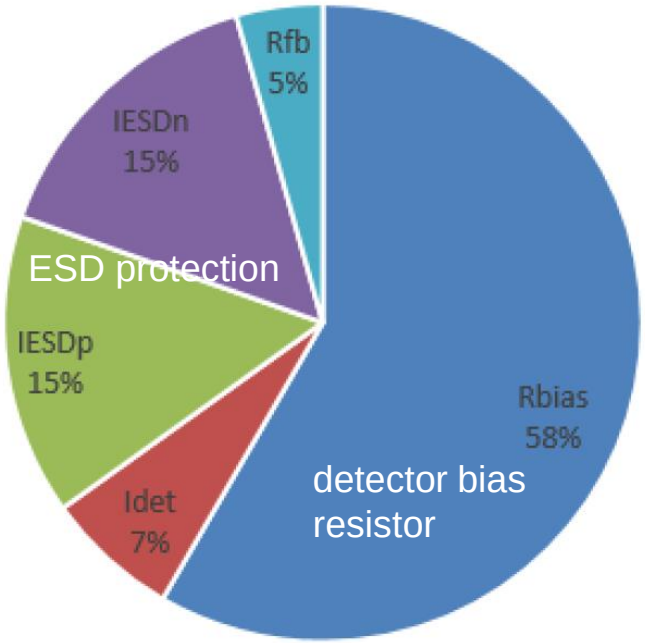


$C_T = C_{det} + C_{cable} + C_{ESD\_n/p} + C_{gs1} + C_{gd1} + C_{PCB}$

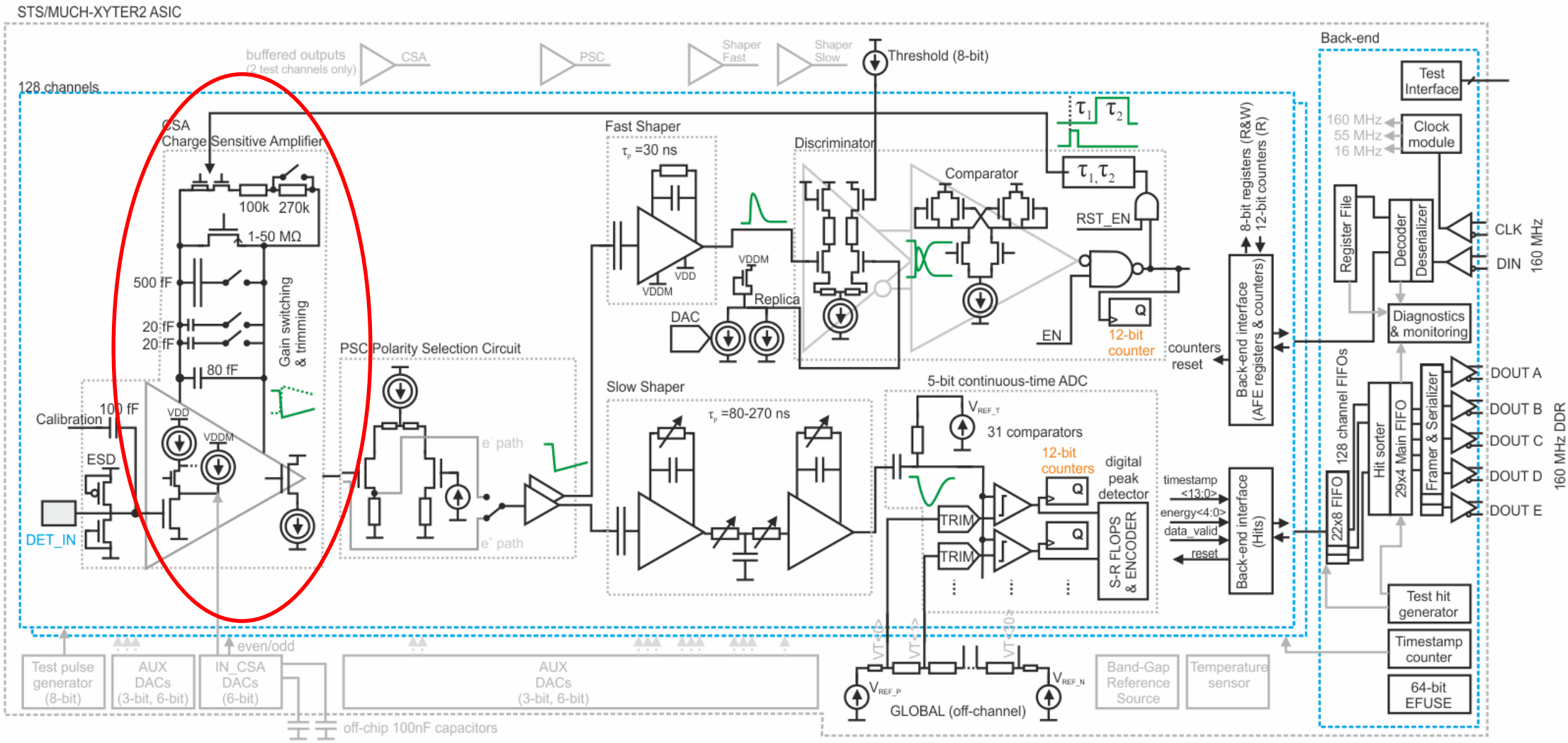
voltage noise



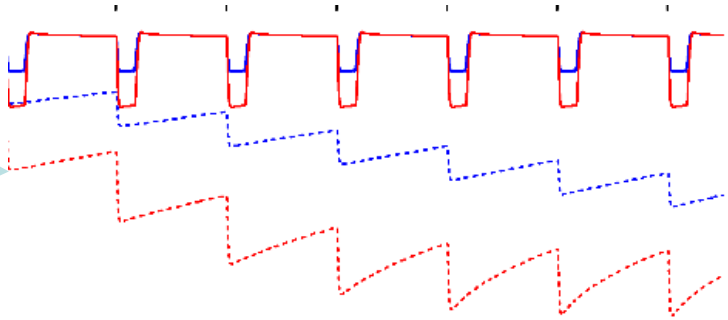
current noise

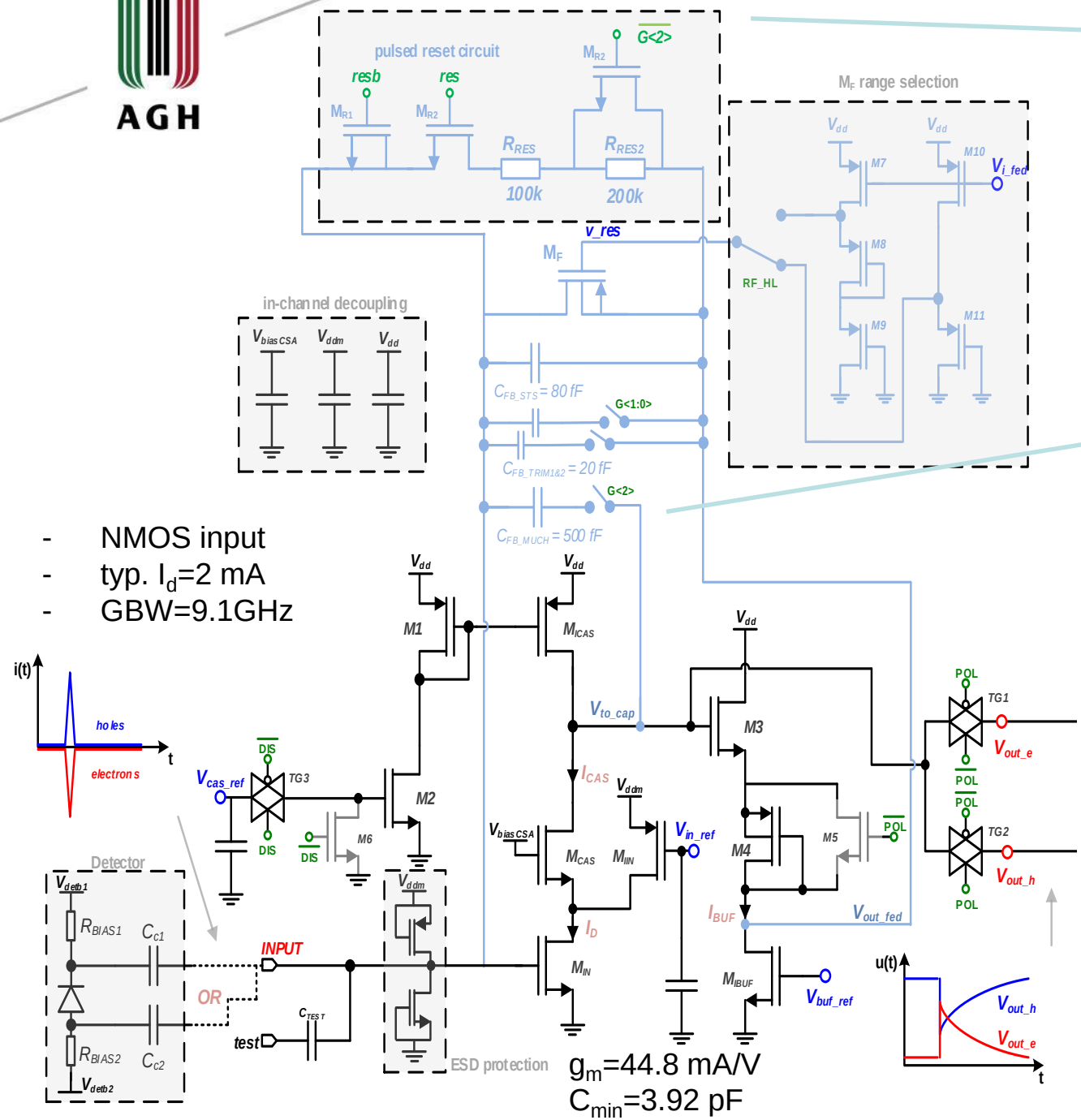


Source	Typ. value	Used for calc.
R_{bias}	500 $k\Omega$ - 1.5 $M\Omega$	1.5 $M\Omega$
I_{det}	1 - 8 nA/cm	4 nA
I_{ESDn}	1 - 10 nA	9 nA
I_{ESDp}	1 - 10 nA	9 nA
R_{fb}	5 $M\Omega$ - 30 $M\Omega$	20 $M\Omega$
R_{Al}	10.5 Ω/cm	42 Ω
R_{cable}	0.635 Ω/cm	12.7 Ω
$R_{inter.}$	10 Ω - 25 Ω	15 Ω
$M_{1,th}$	Tech. dep.	$\alpha = 0.5$, $\gamma = 1$, g_m=0.044 A/V


STS/MUCH-XYTER2 ASIC
128 channels
buffered outputs
(2 test channels only)
CSA
PSC
Shaper Fast
Shaper Slow
Threshold (8-bit)
Back-end
CSA
Charge Sensitive Amplifier
100k
270k
1-50 MΩ
500 fF
20 fF
20 fF
80 fF
Gain switching & trimming
Calibration
100 fF
ESD
DET_IN
VDD
VDDM
PSC Polarity Selection Circuit
e⁻ path
e⁺ path
Fast Shaper
τp =30 ns
VDD
VDDM
Slow Shaper
τp =80-270 ns
Discriminator
Comparator
Replica
DAC
RST_EN
EN
12-bit counter
Q
counters reset
5-bit continuous-time ADC
VREF_T
31 comparators
12-bit counters
digital peak detector
TRIM
S-R FLOPS & ENCODER
8-bit registers (R&W)
12-bit counters (R)
Back-end interface (AFE registers & counters)
timestamp <13:0>
energy<4:0>
data_valid
reset
Back-end interface (Hits)
Test Interface
160 MHz
55 MHz
16 MHz
Clock module
Register File
Decoder
Deserializer
CLK
DIN
160 MHz
Diagnostics & monitoring
128 channel FIFOs
22x8 FIFO
Hit sorter
29x4 Main FIFO
Framer & Serializer
DOUT A
DOUT B
DOUT C
DOUT D
DOUT E
160 MHz DDR
Test hit generator
Timestamp counter
64-bit EFUSE
Test pulse generator (8-bit)
AUX DACs (3-bit, 6-bit)
IN_CSA DACs (6-bit)
even/odd
AUX DACs (3-bit, 6-bit)
off-chip 100nF capacitors
VREF_P
VREF_N
GLOBAL (off-channel)
Band-Gap Reference Source
Temperature sensor

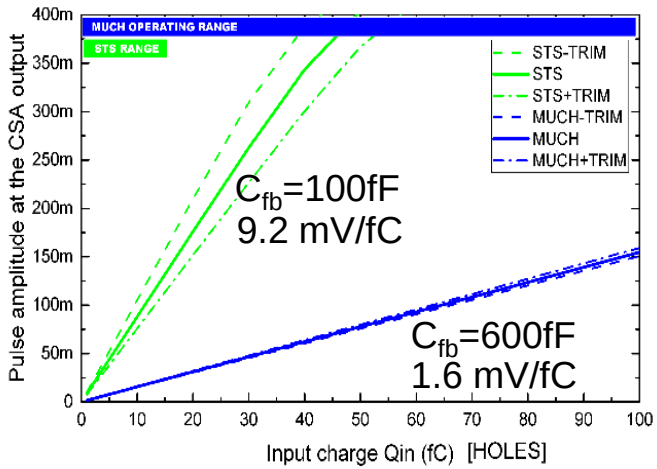
Input amplifier

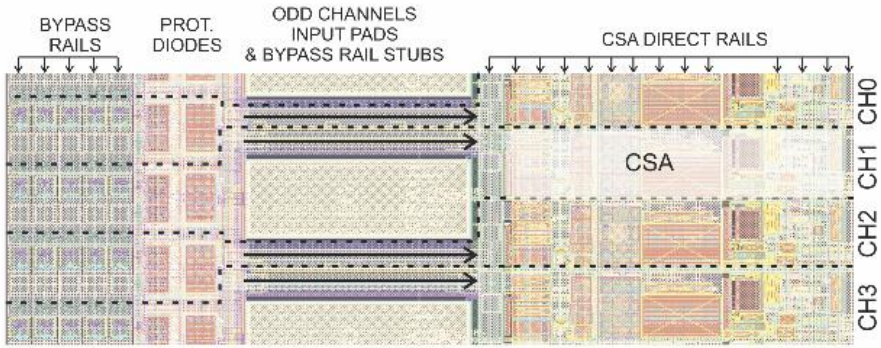




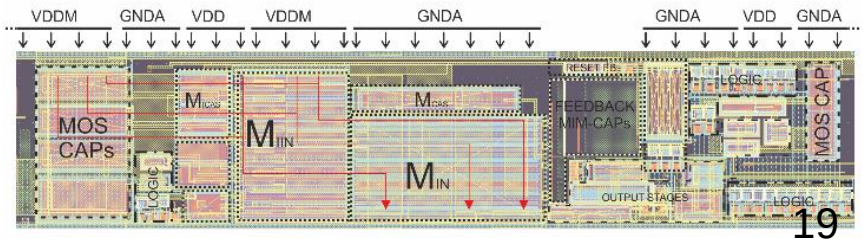
- NMOS input
- typ. I_d=2 mA
- GBW=9.1GHz

g_m=44.8 mA/V
C_{min}=3.92 pF

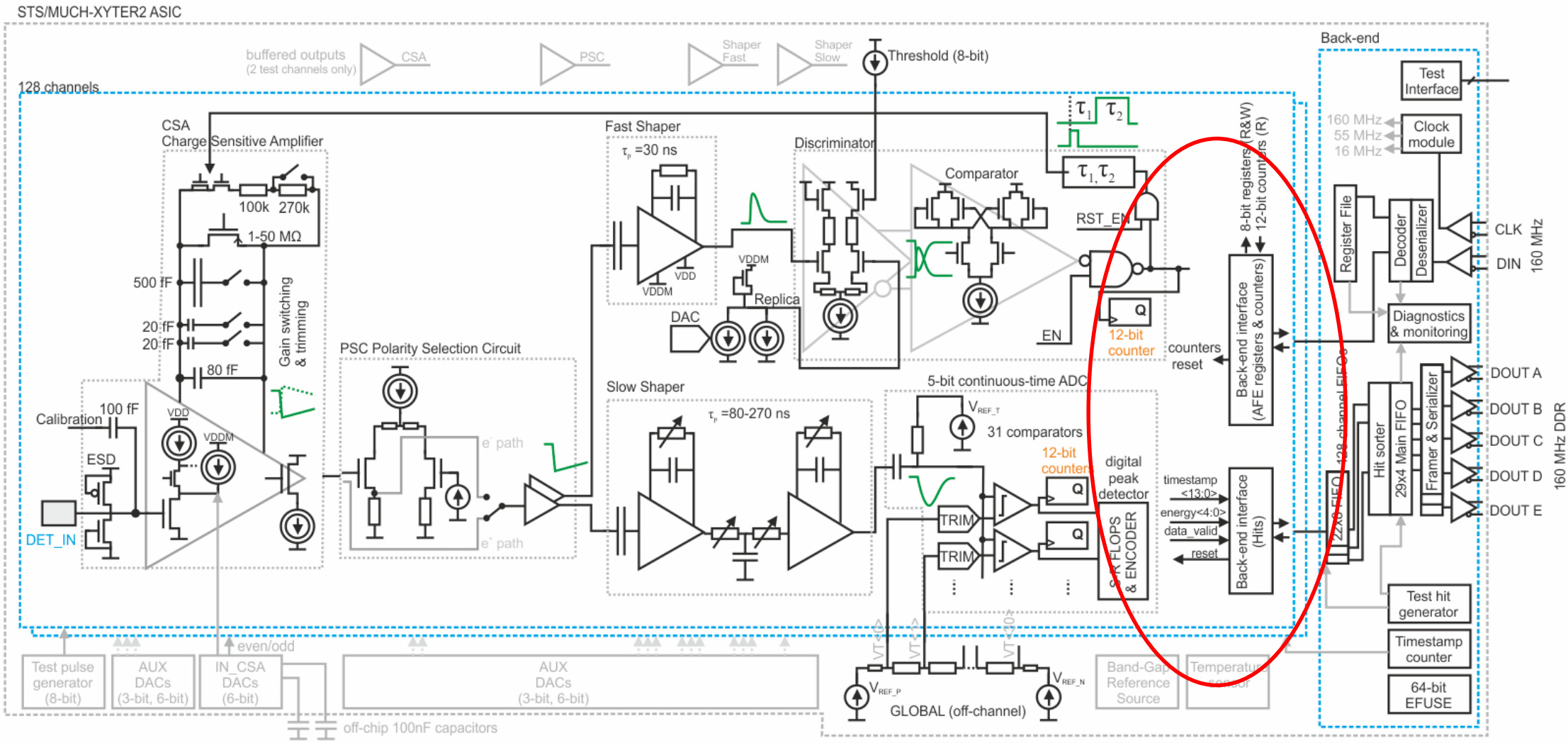




worst case ΔV=20mV



0.014 mm^2


STS/MUCH-XYTER2 ASIC
128 channels
buffered outputs
(2 test channels only)
CSA
PSC
Shaper Fast
Shaper Slow
Threshold (8-bit)
Back-end
Test Interface
160 MHz
55 MHz
16 MHz
Clock module
CSA
Charge Sensitive Amplifier
100k
270k
1-50 MΩ
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Hit sorter
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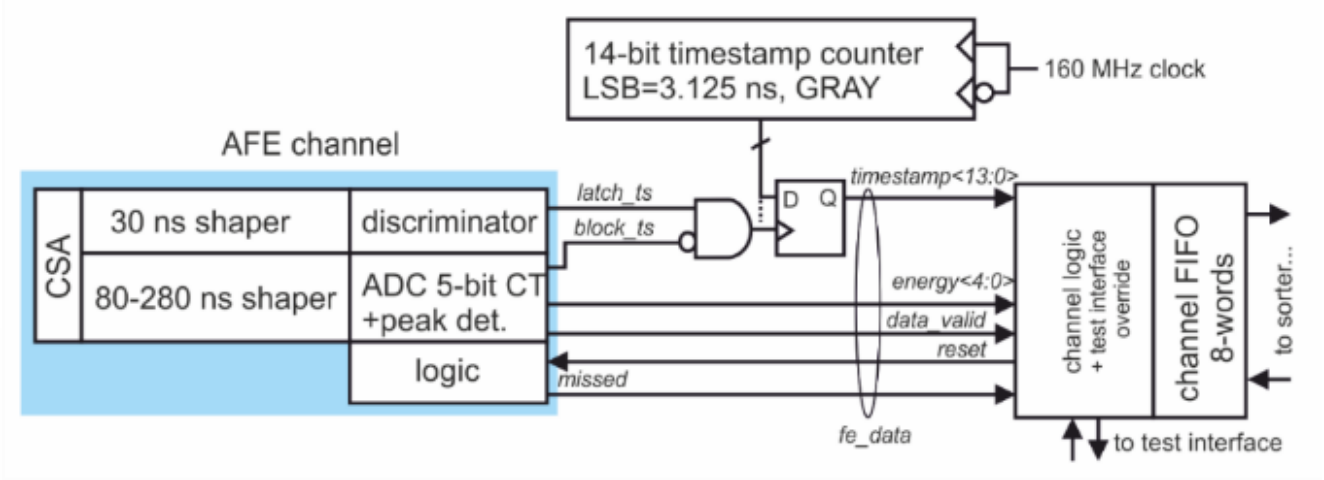
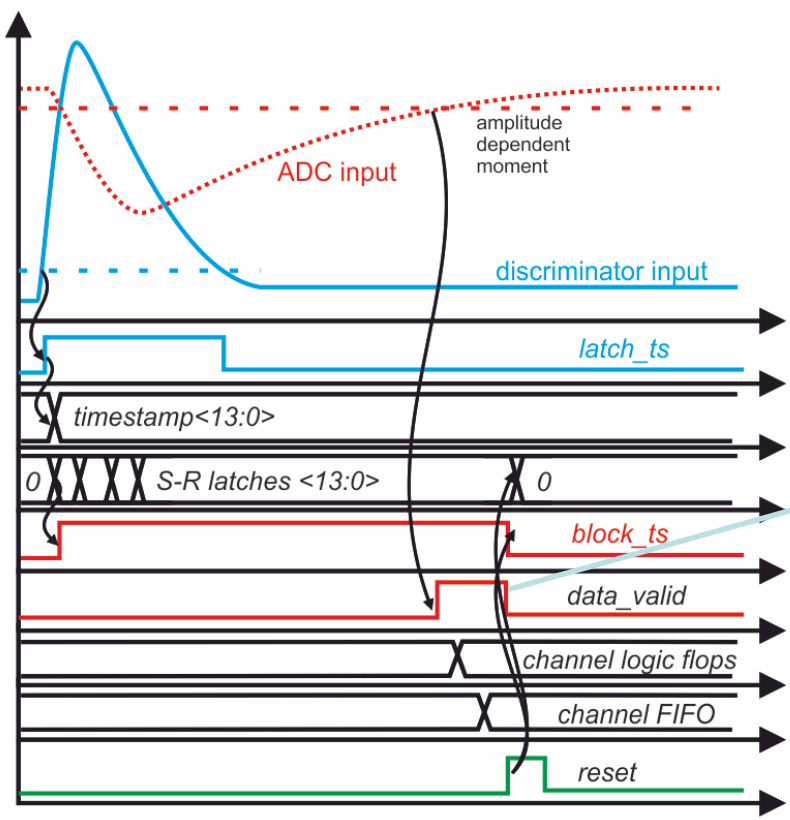
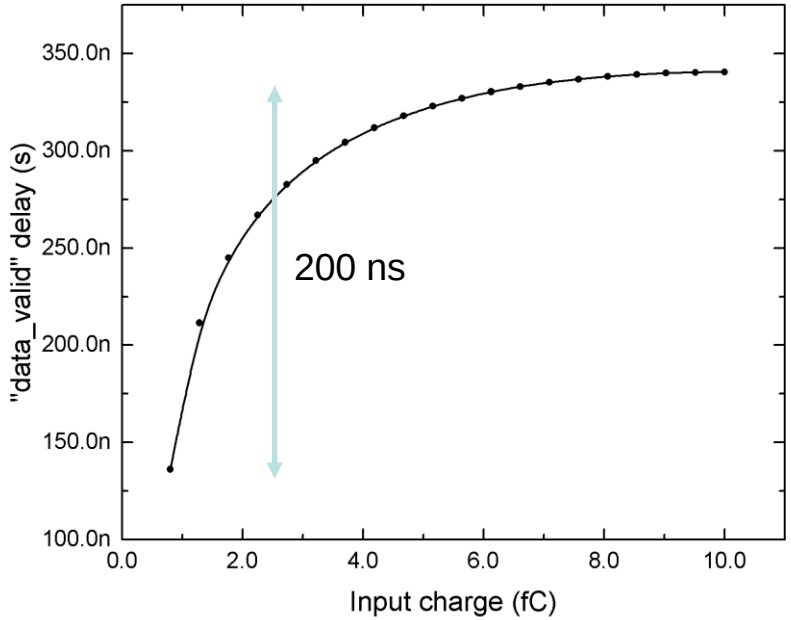
AUX DACs (3-bit, 6-bit)
off-chip 100nF capacitors
VREF_P
VREF_N
GLOBAL (off-channel)
Band-Gap Reference Source
Temperature sensor

Hit digitization mechanism

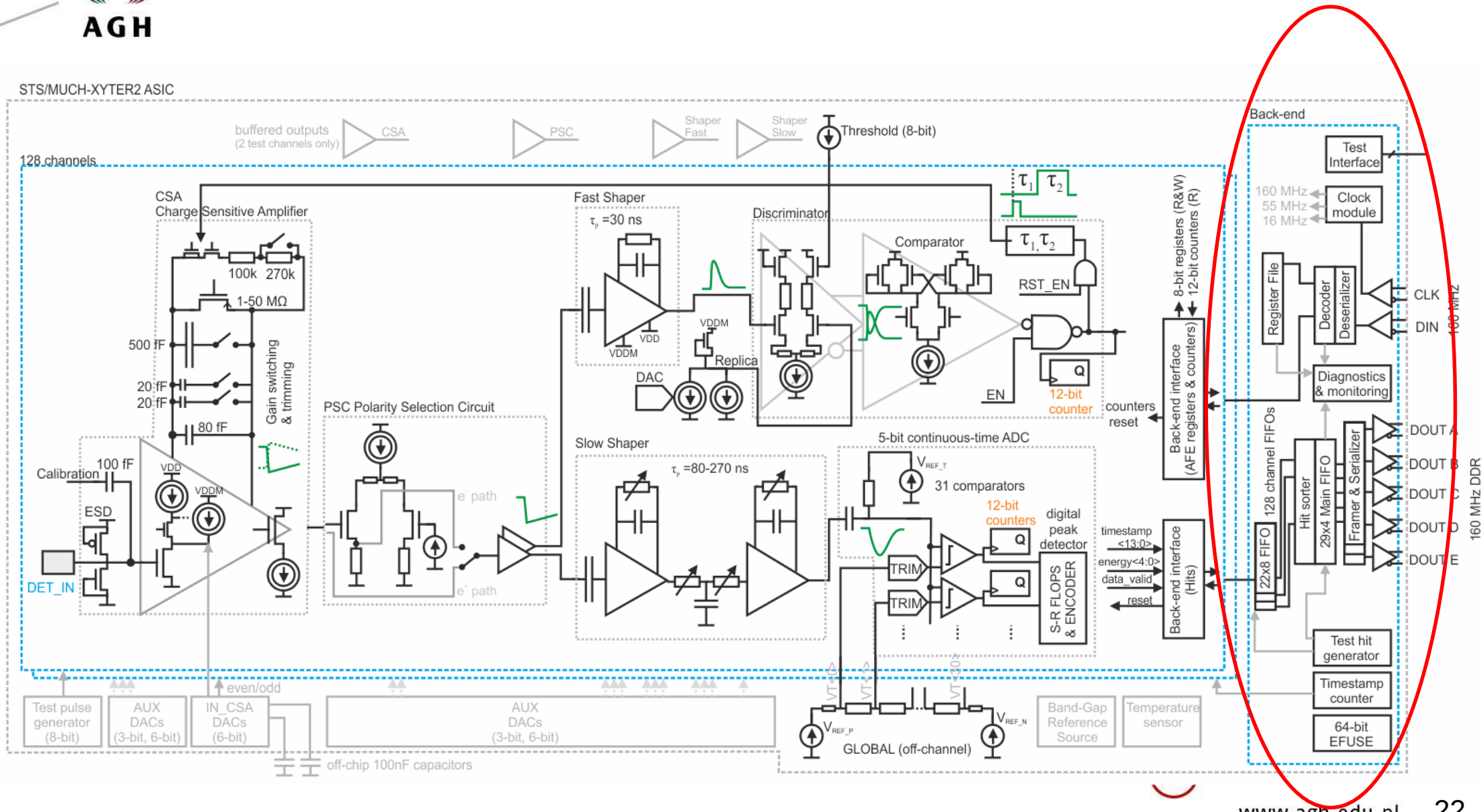




SELF-TRIGGERED MODE



Hits leave channel out of order depending on their amplitude.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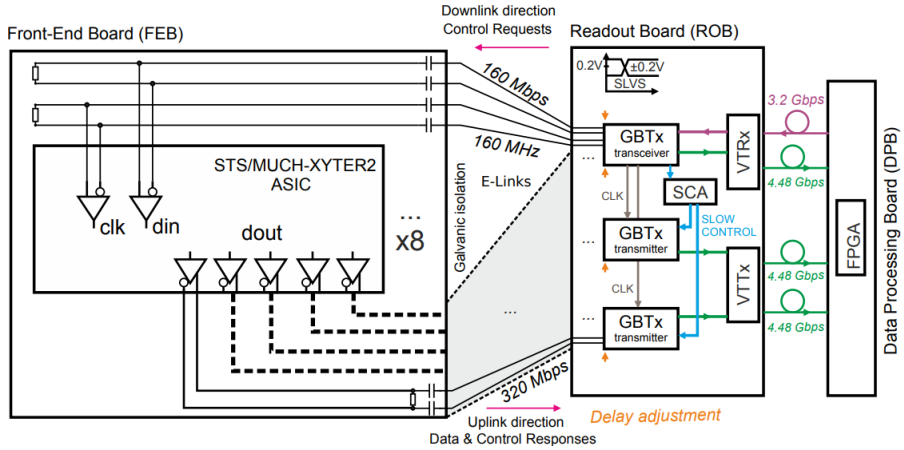
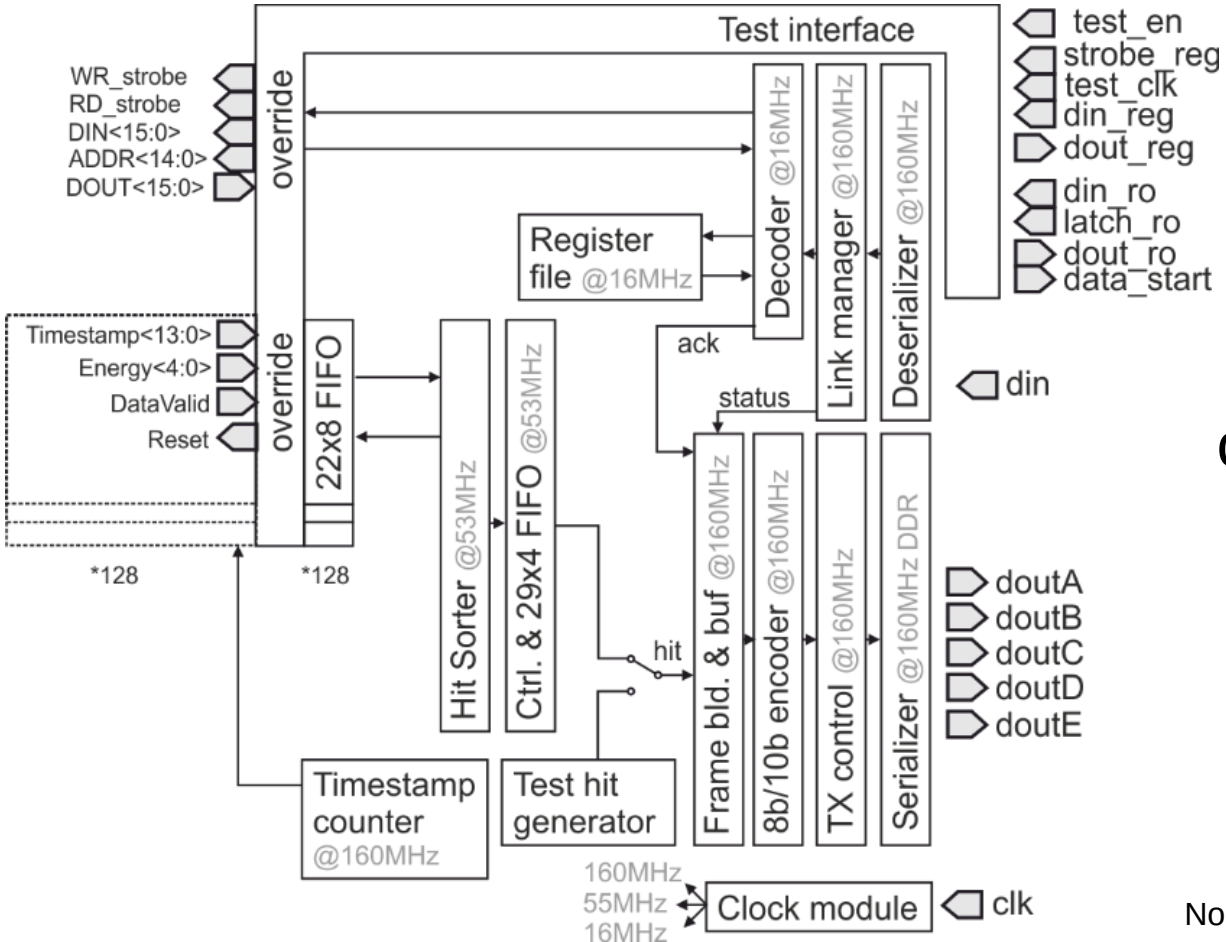
AUX DACs (3-bit, 6-bit)
off-chip 100nF capacitors
V_{REF_P}
V_{REF_N}
GLOBAL (off-channel)
Band-Gap Reference Source
Temperature sensor

Back-end

Physical interface on FEB

- DOWNLINK: shared, multi-drop, AC-coupled 160 Mbps clock & data lines, SLVS (e-links of GBTx)
- UPLINK: individual, AC-coupled, 320 Mbps
- Dedicated protocol: STS-HCTSP (shown later)





test path 20 Mbps

to evaluate noise
introduced by digital part

control path 2.6 Mframes/s

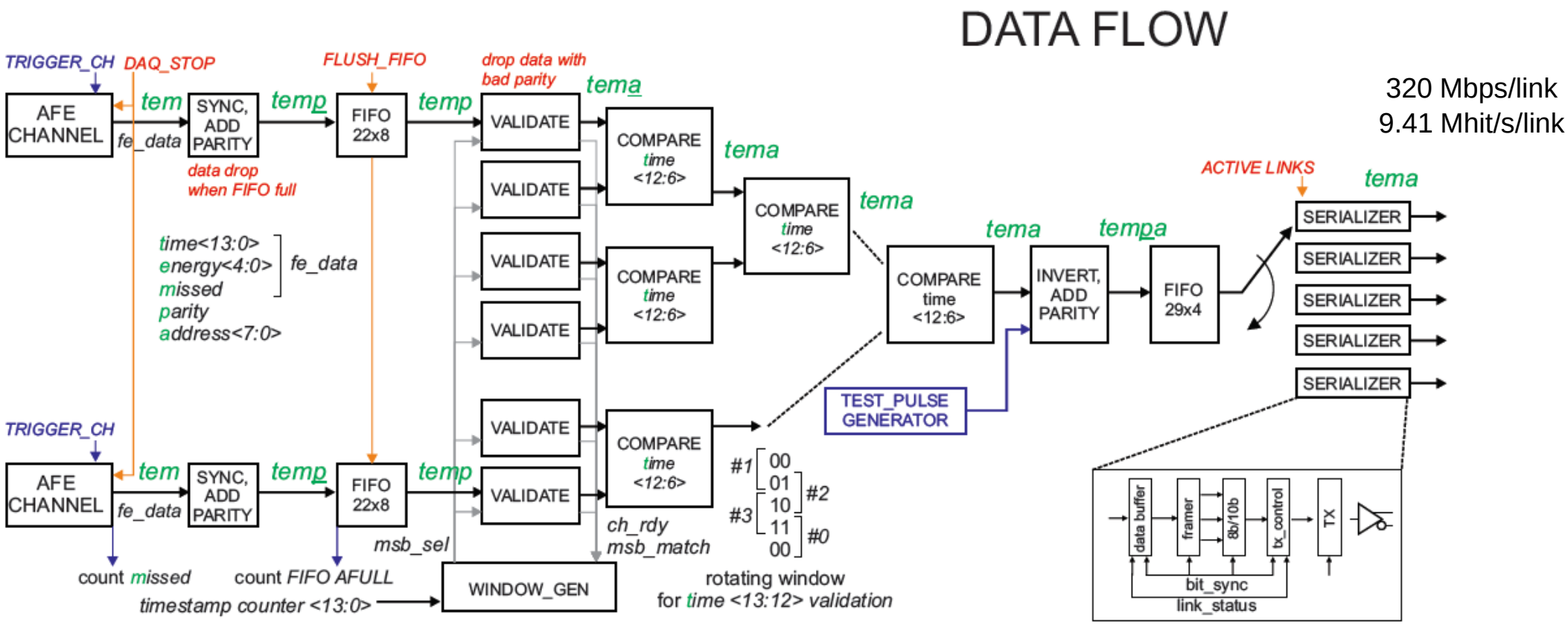
secure configuration

data path 9.41 – 47 Mhit/s/ASIC

fast hit data streaming
ctr. requests ack.

No separate slow control interface.

AFE > Channel FIFO > Sorter > 5 output serializers



Pre-sorting based on timestamp <13:6>

Hit from any channel can leave via any link

Diagnostic / throttling features:

- test hit generator (multi level, separate generator (rate & content control), channel triggering)
- counting of: event missed, channel FIFO almost full
- channel masking & data drop & FIFOs

STS-HCTSP Protocol

protocol adapted for other CBM-related ASICs

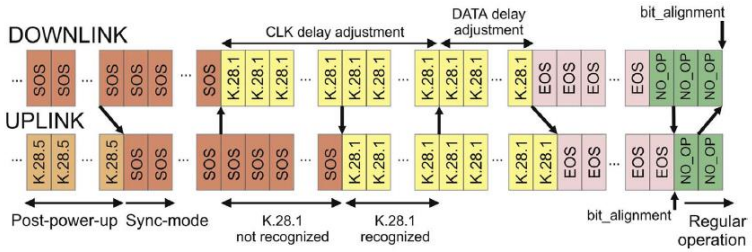
		Downlink frame (60 bits after encoding)						
Frame type / bits	8b/10b block	8b/10b block		8b/10b block		8b/10b block	8b/10b block	8b/10b block
	1-8	9-12	13-16	17-18	19-24	25-32	33-40	41-48
GENERAL FRAME STRUCTURE								
frame	K 28.5 comma	Payload <33:30>	4-bit Sequence No.	Frame type	Payload <29:0>			
STS-SPECIFIC FRAME STRUCTURE								
No_op	K 28.5 comma	Chip Address (0x0..0x7, 0x15)	4-bit Sequence No.	0x0	Payload<14:9>	Payload<8:1>	Payload <0> CRC<14:8>	CRC<7:0>
WRaddr	K 28.5 comma	Chip Address (0x0..0x7, 0x15)	4-bit Sequence No.	0x1	Payload<14:9>	Payload<8:1>	Payload <0> CRC<14:8>	CRC<7:0>
WRdata	K 28.5 comma	Chip Address (0x0..0x7, 0x15)	4-bit Sequence No.	0x2	Payload<14:9>	Payload<8:1>	Payload <0> CRC<14:8>	CRC<7:0>
RData	K 28.5 comma	Chip Address (0x0..0x7, 0x15)	4-bit Sequence No.	0x3	Payload<14:9>	Payload<8:1>	Payload <0> CRC<14:8>	CRC<7:0>

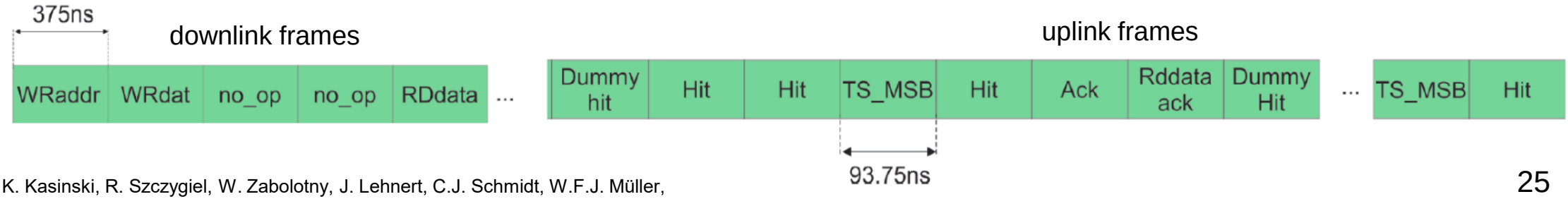
	Uplink frame (30 bits after encoding)																							
	8b/10b block								8b/10b block								8b/10b block							
Frame type	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
GENERAL FRAME STRUCTURE																								
Frame	*Huffman-encoded header + up to 23 bits of user-defined payload*																							
STS-SPECIFIC FRAME STRUCTURE																								
Dummy Hit	0	7-bit channel address = 0x0							5-bit ADC = 0x0					0x0	0x0 / Time-stamp TS<13:6>									0
Hit	0	7-bit channel address (0..127)							5-bit ADC > 0x0					Time-stamp TS<9:8> (overlap)	Time-stamp TS<7:0>									EM Event Missed
TS_MSB	1	1	Time-stamp TS<13:8>						Time-stamp TS<13:8>						Time-stamp TS<13:8>						4-bit CRC (0x9)			
RDdata_ack	1	0	1	15-bit payload (register content)																3-bit Sequence No.		3-bit CRC (0x2C)		
Ack	1	0	0	ACK status	4-bit Sequence Number			CP Control Parity	4-bit status						Time-stamp TS<7:2>						4-bit CRC (0x9)			

	Special uplink frames		
Frame type	8b/10b block	8b/10b block	8b/10b block
Sync	K 28.5	K 28.5	K 28.5
Post_Reset	K 28.5		
	Low-level reset frames* (not in 8b/10b encoding)		
SOS	00000111111111100000		
EOS	11001111110000001100		

- fully synchronous
- constant frame lenghts
- 8b/10b encoding
- huffman encoding
- periodic sync frames (comma)
- lossless compression
- special synchronization method

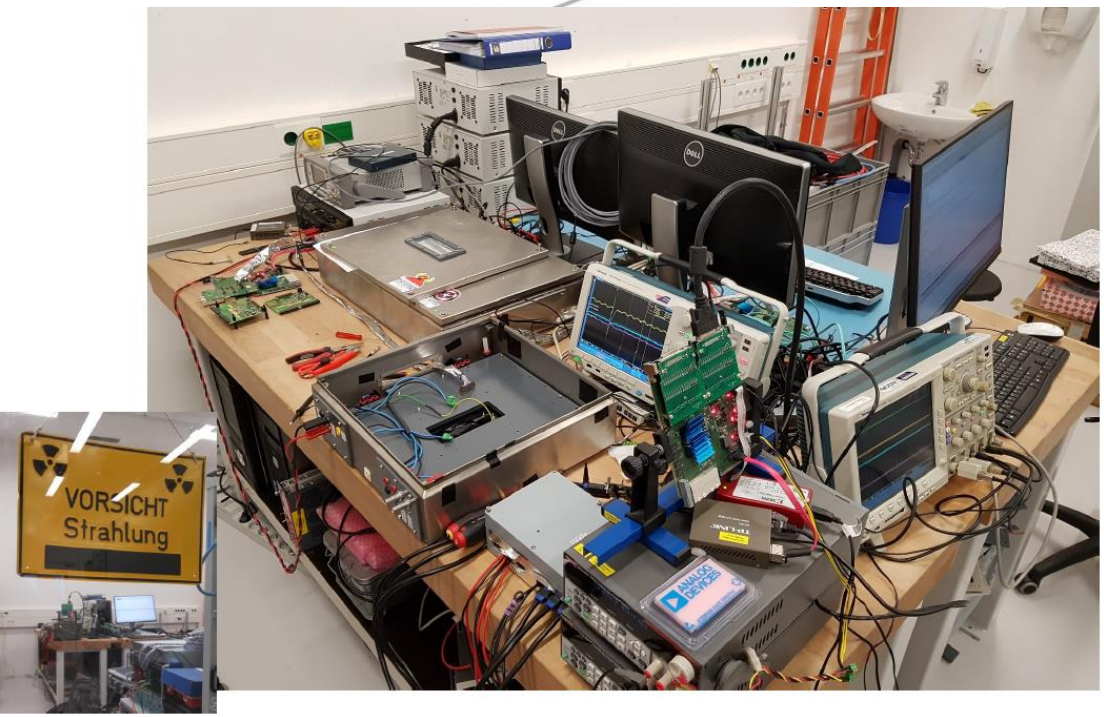
(setting up GBTx delays)

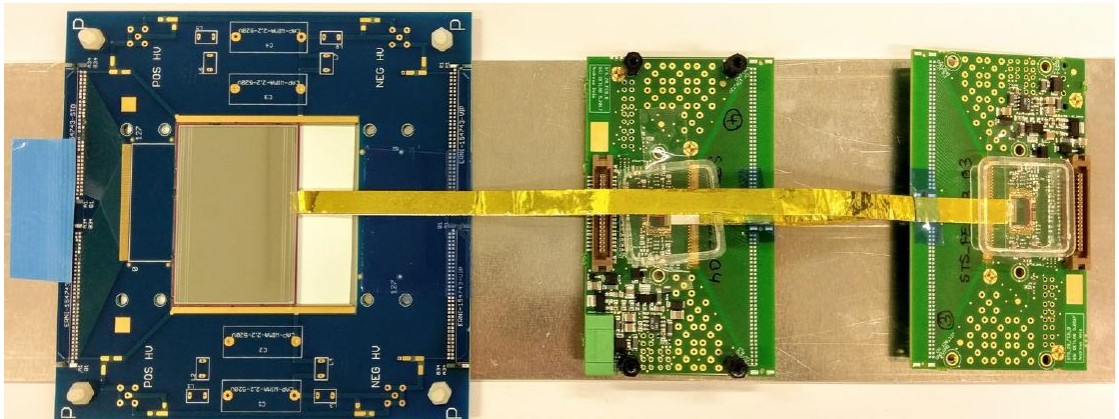


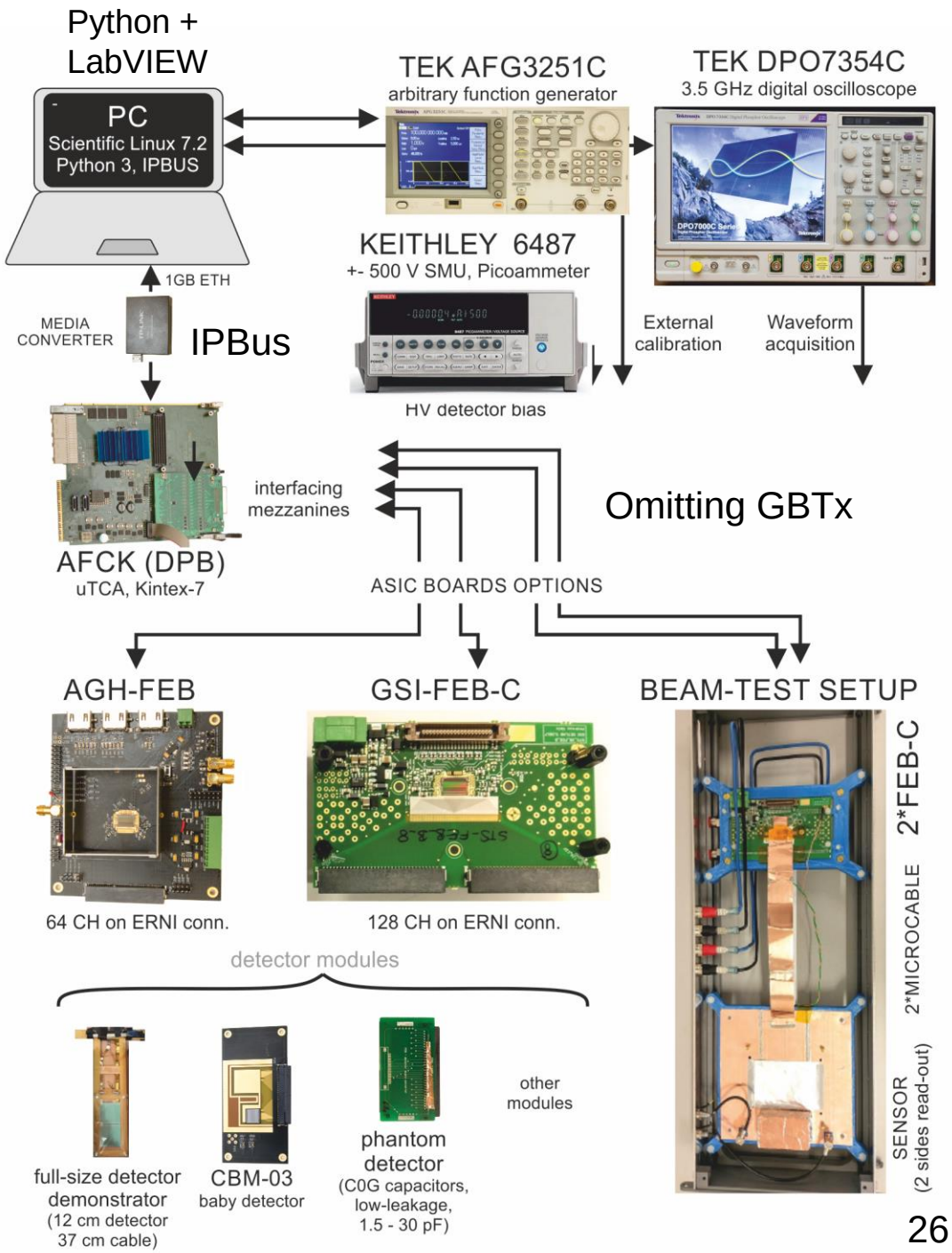


K. Kasinski, R. Szczygiel, W. Zabolotny, J. Lehnert, C.J. Schmidt, W.F.J. Müller,
A protocol for hit and control synchronous transfer for the front-end electronics at the CBM experiment, NIM A 835 (2016) 66–73.

Test setup

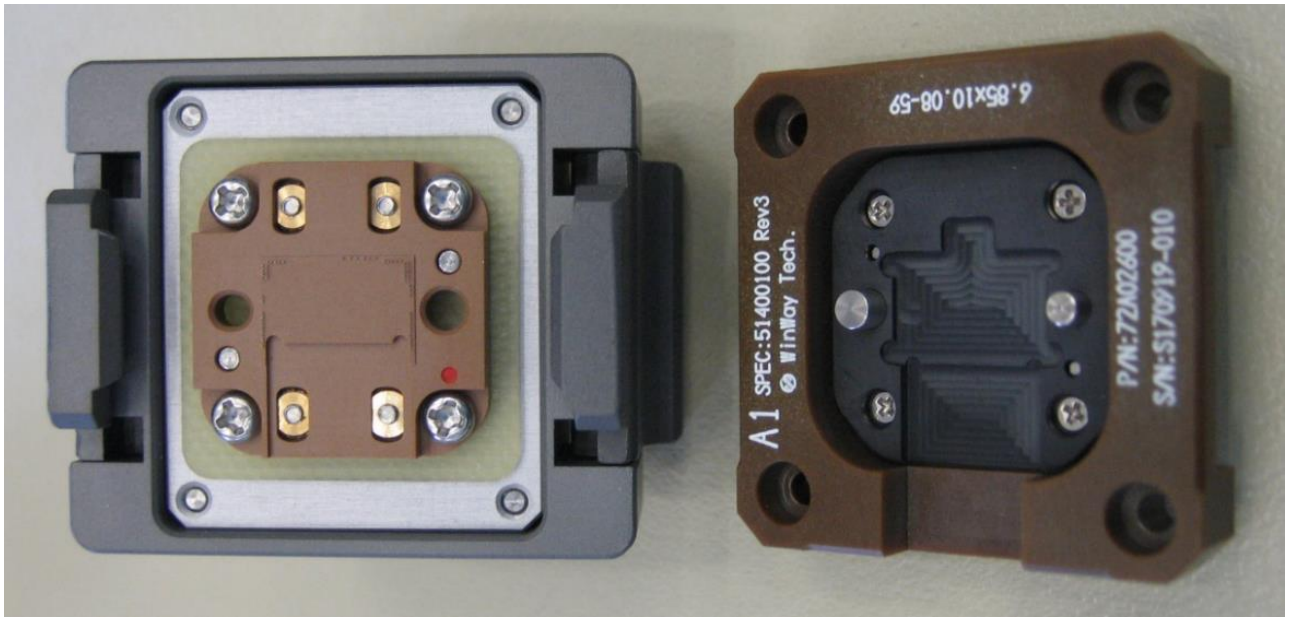

VORSICHT
Strahlung




Python +
LabVIEW
PC
Scientific Linux 7.2
Python 3, IPBUS
TEK AFG3251C
arbitrary function generator
TEK DPO7354C
3.5 GHz digital oscilloscope
KEITHLEY 6487
+- 500 V SMU, Picoammeter
1GB ETH
MEDIA
CONVERTER
IPBus
External
calibration
Waveform
acquisition
HV detector bias
interfacing
mezzanines
Omitting GBTx
AFCK (DPB)
uTCA, Kintex-7
ASIC BOARDS OPTIONS
AGH-FEB
GSI-FEB-C
BEAM-TEST SETUP
64 CH on ERNI conn.
128 CH on ERNI conn.
detector modules
full-size detector
demonstrator
(12 cm detector
37 cm cable)
CBM-03
baby detector
phantom
detector
(C0G capacitors,
low-leakage,
1.5 - 30 pF)
other
modules
2*FEB-C
2*MICROCABLE
SENSOR
(2 sides read-out)

Inter-assembly testing with pogo-prober

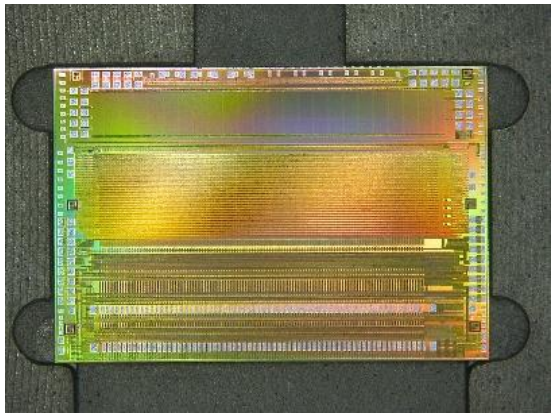
Aim: check connectivity of ASIC – CABLE – SENSOR prior to wire-bonding onto PCB

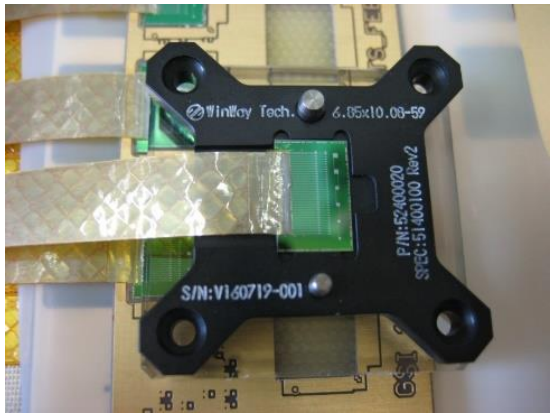


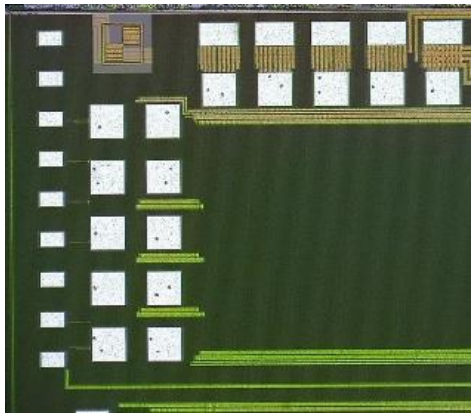
Winway Tech. GmbH

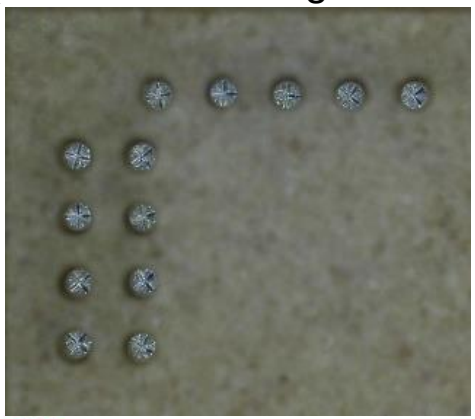
additional set of pads
150x150, pitch 240 µm

pads are wire-bondable
afterwards (multi-tier bonding of VDD)





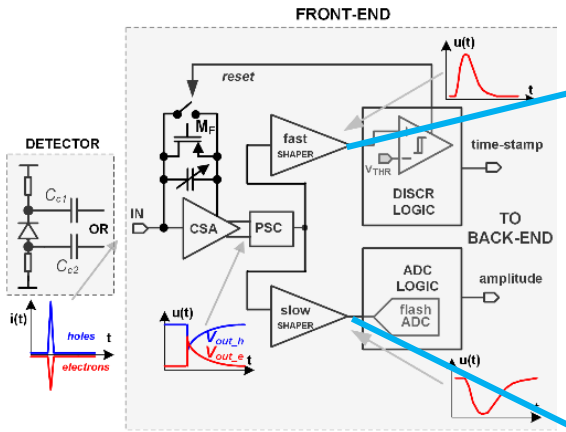


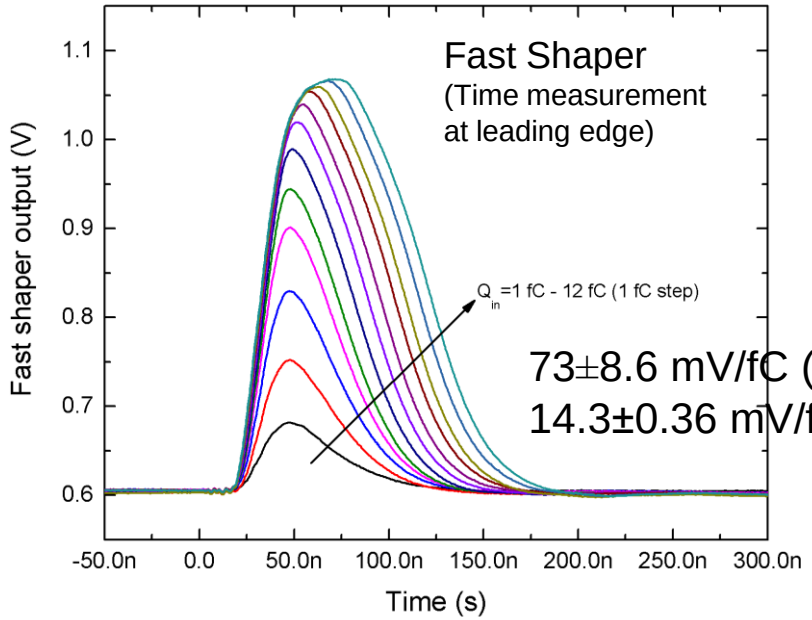


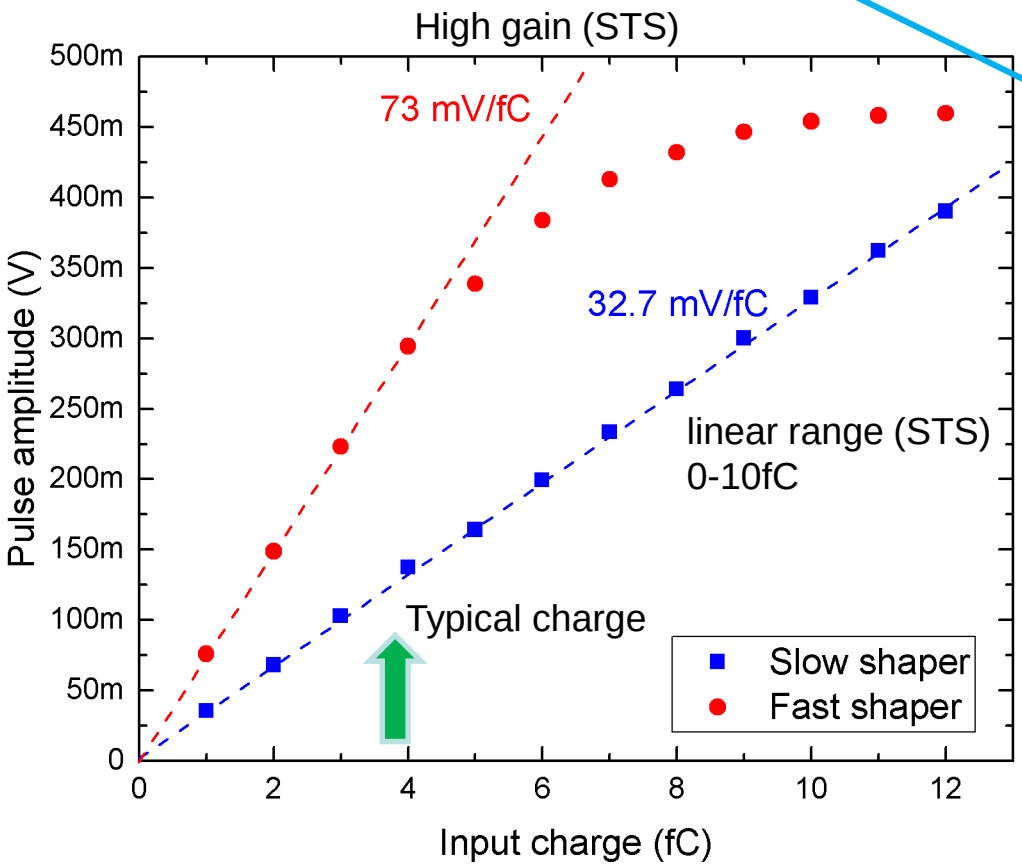
Bring chip into operation and quickly evaluate noise growth.
Tab-bonding can be reworked at this level.

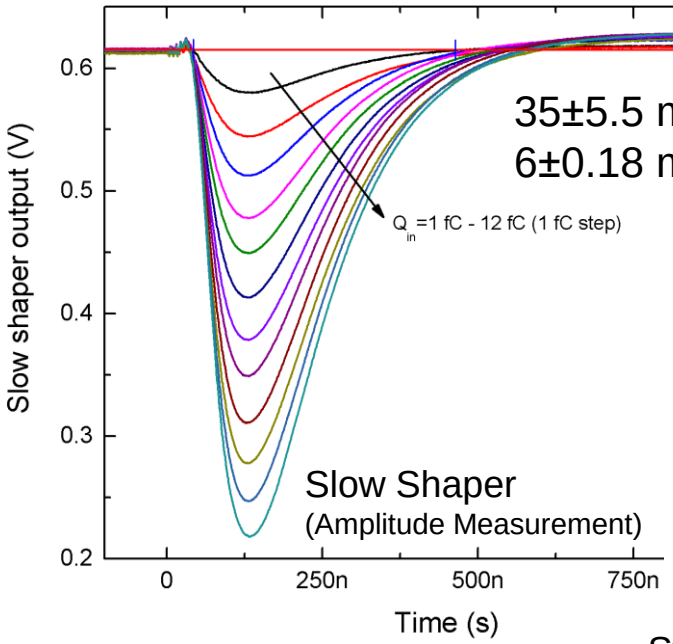
C. Simons (GSI, Darmstadt, Germany)

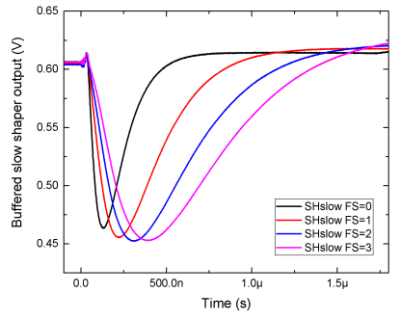
Measured waveforms



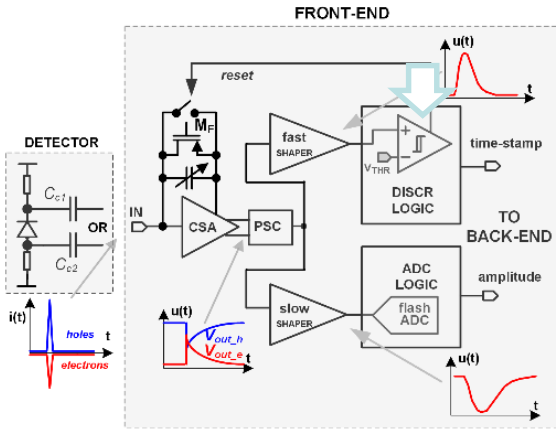


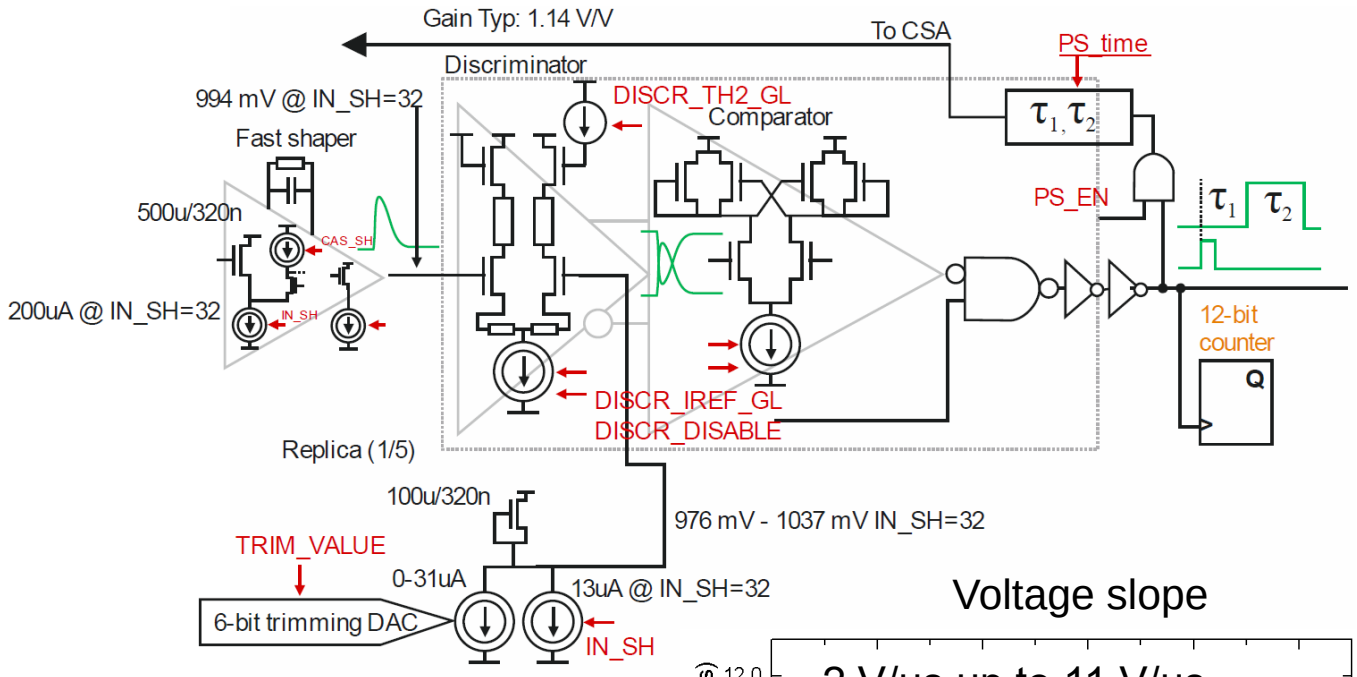




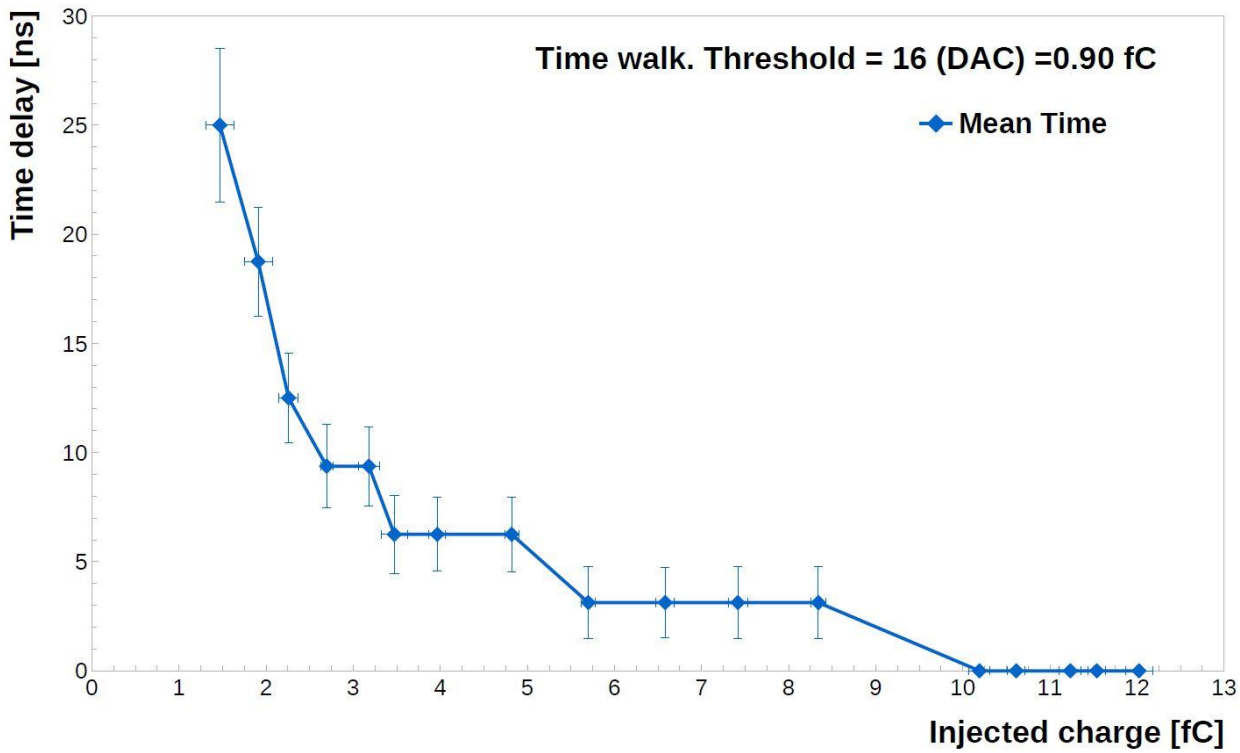


Switchable Shaping Time

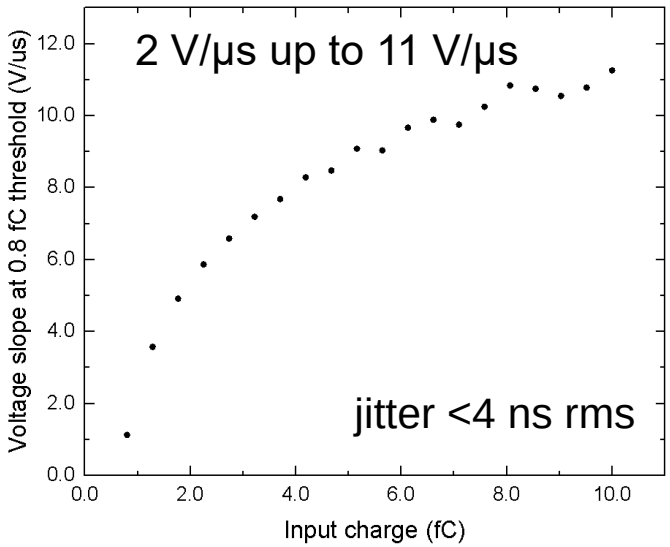




Time walk of comparator



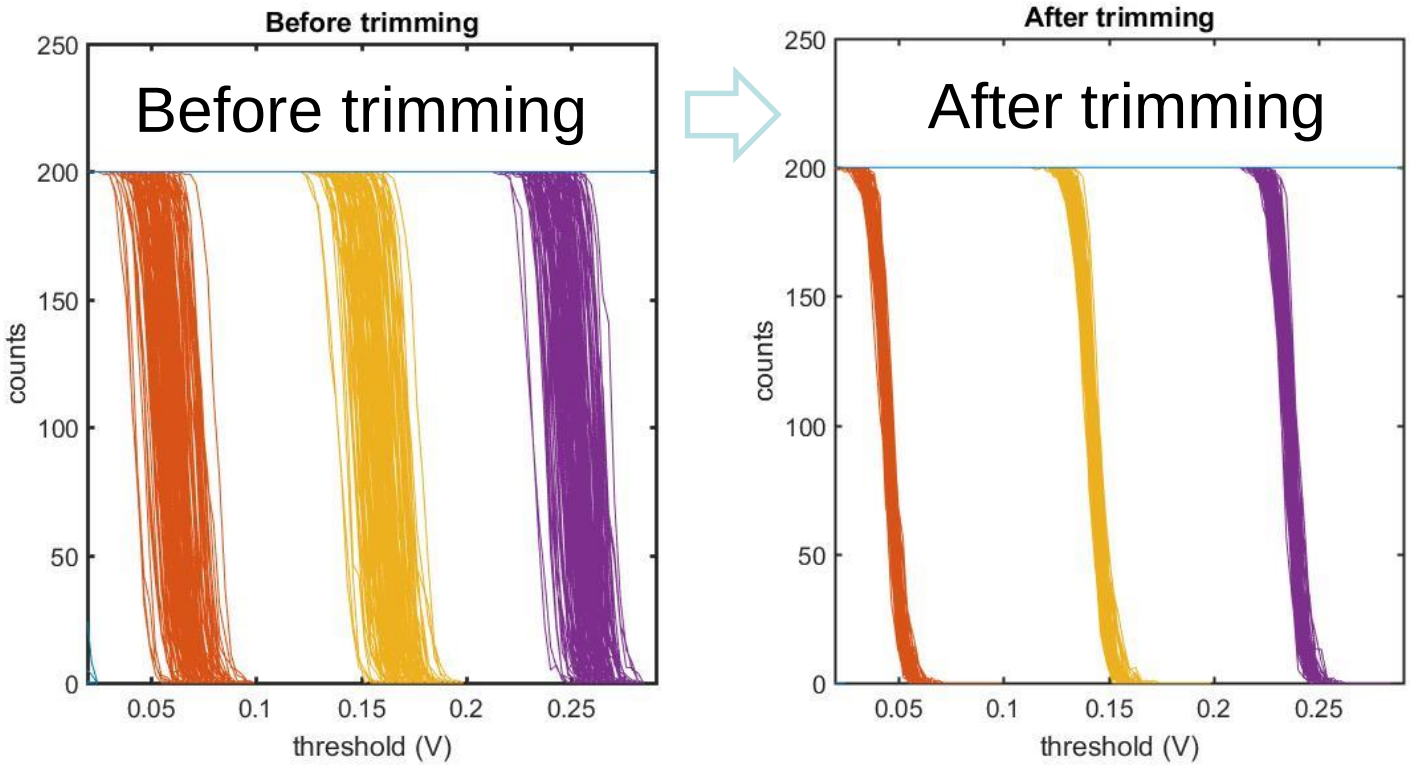
Voltage slope

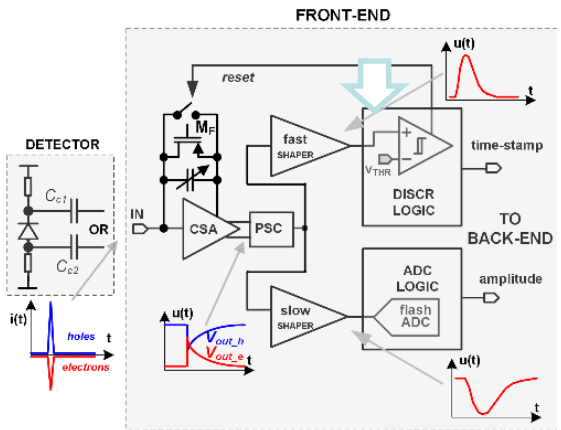


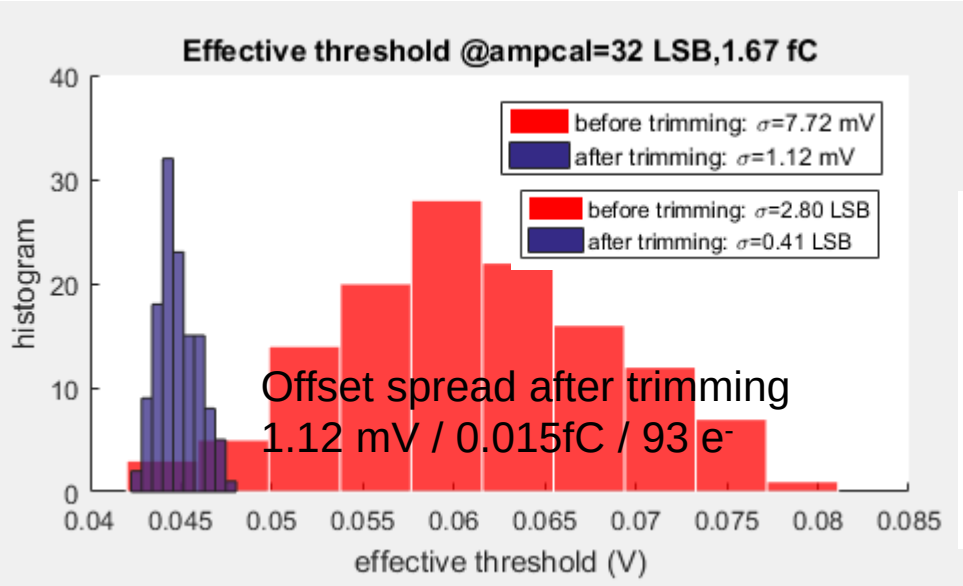
Timestamp will be corrected based on 5-bit amplitude value.

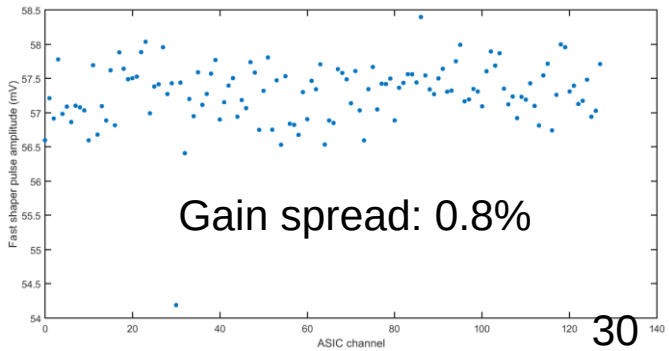
Measured effective fast discriminator offset spread (128 channels)

s-curves

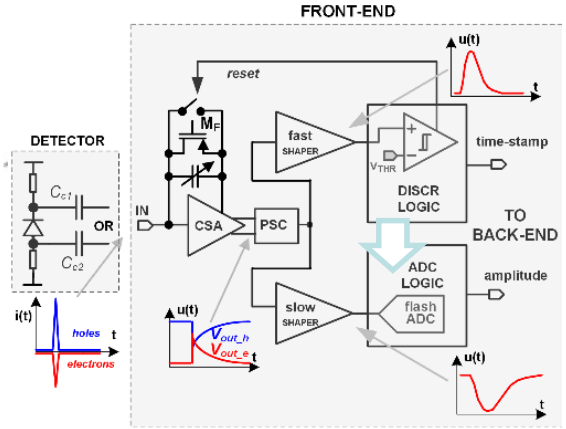


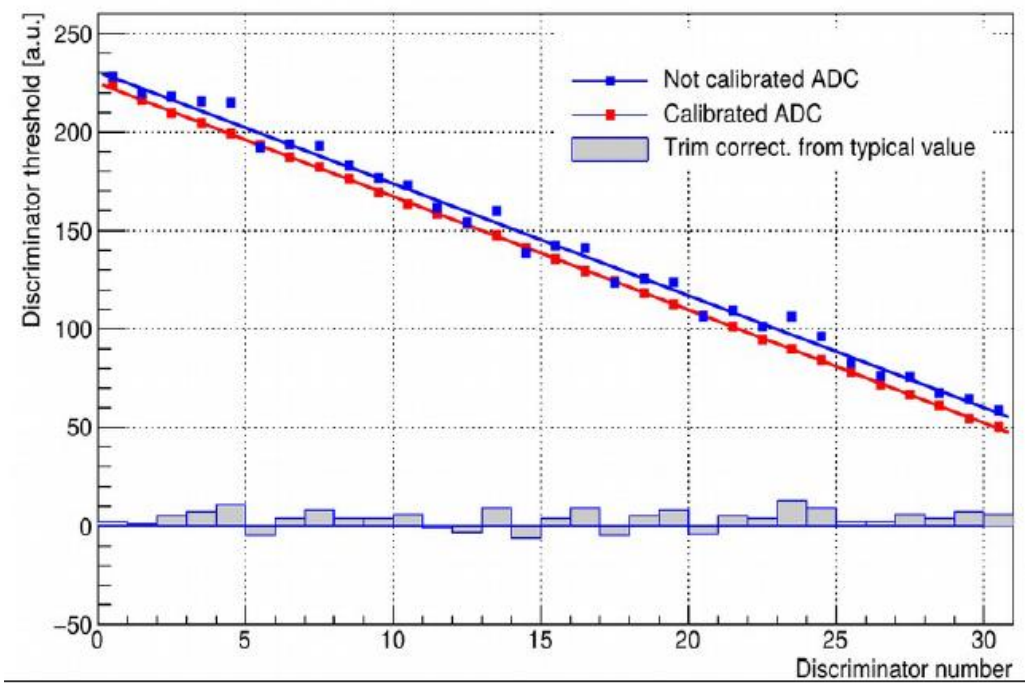




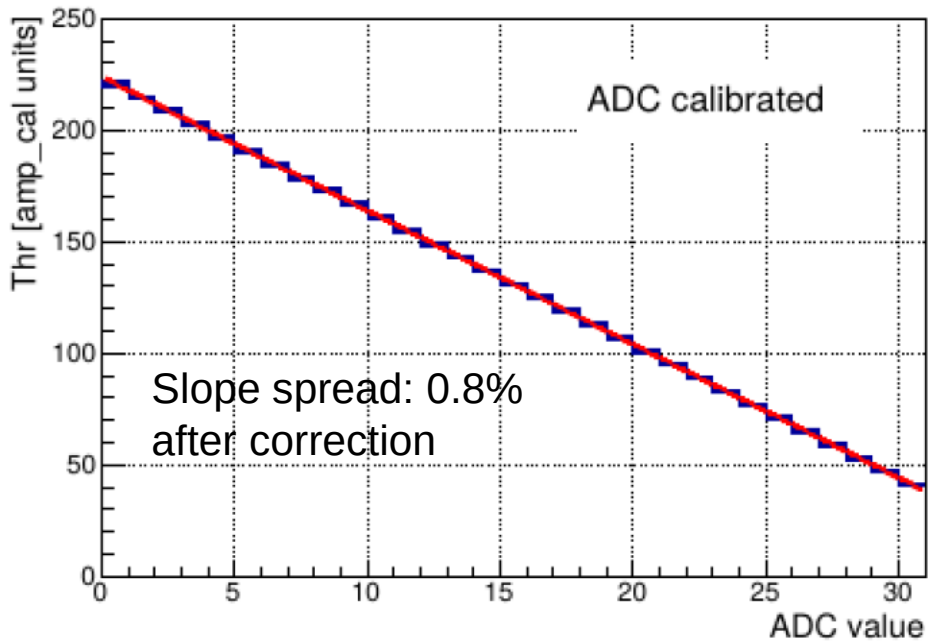


ADC response

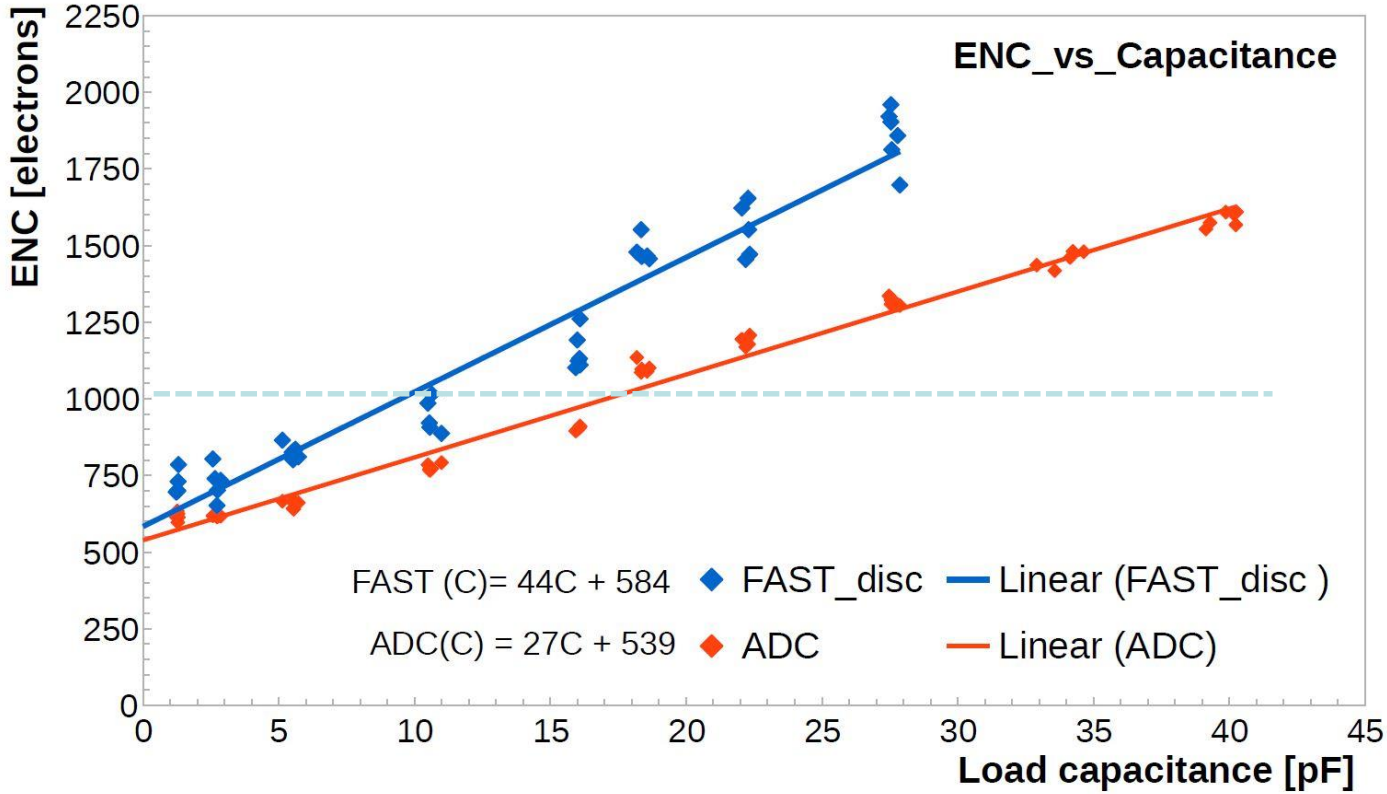


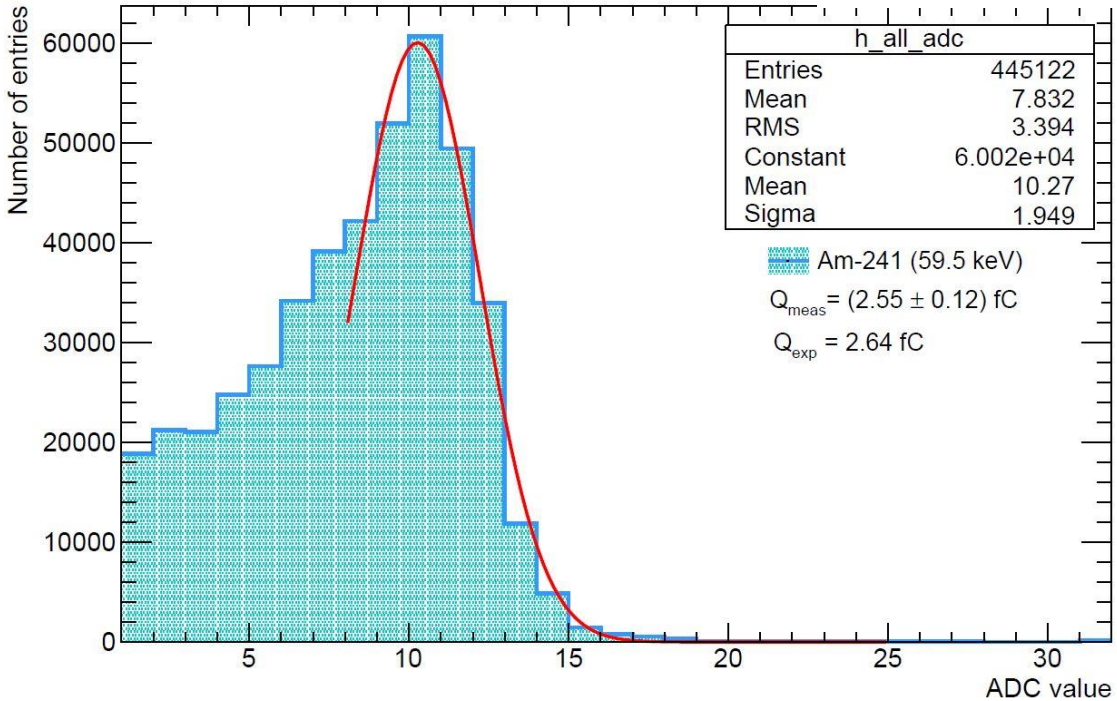


Single channel



All channels

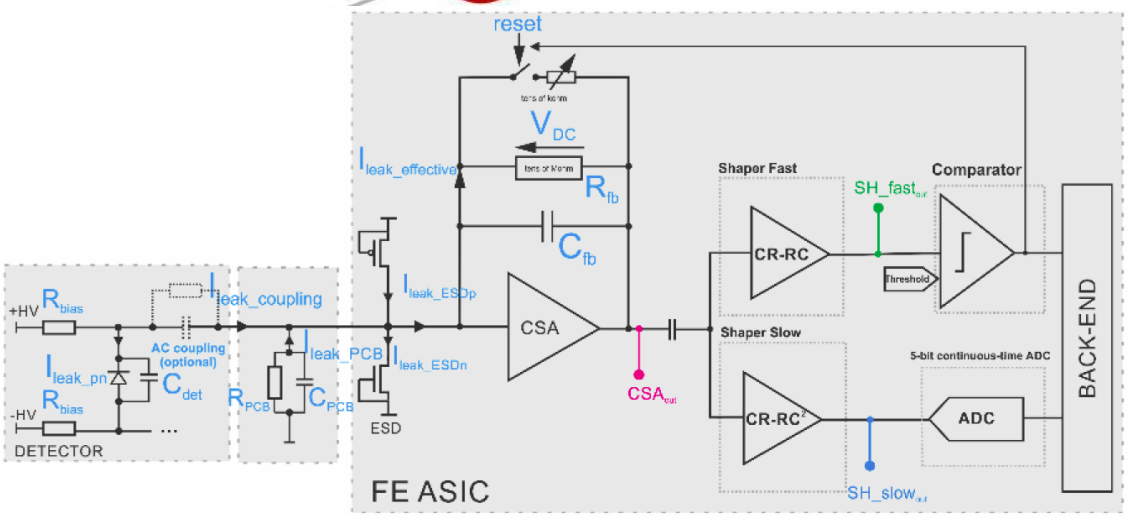

ENC_vs_Capacitance
ENC [electrons]
Load capacitance [pF]
FAST (C)= 44C + 584
ADC(C) = 27C + 539
FAST_disc
ADC
Linear (FAST_disc)
Linear (ADC)

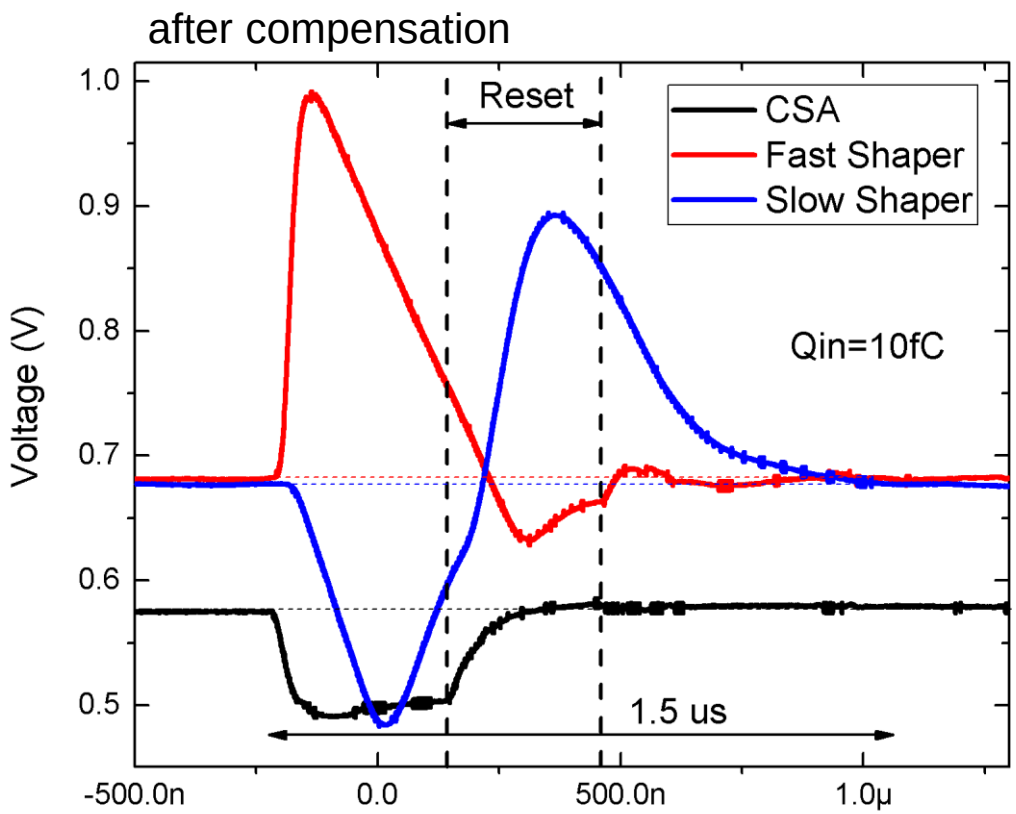

h_all_adc
Entries 445122
Mean 7.832
RMS 3.394
Constant 6.002e+04
Mean 10.27
Sigma 1.949
Am-241 (59.5 keV)
Q_meas = (2.55 ± 0.12) fC
Q_exp = 2.64 fC
Number of entries
ADC value

Lessons learned

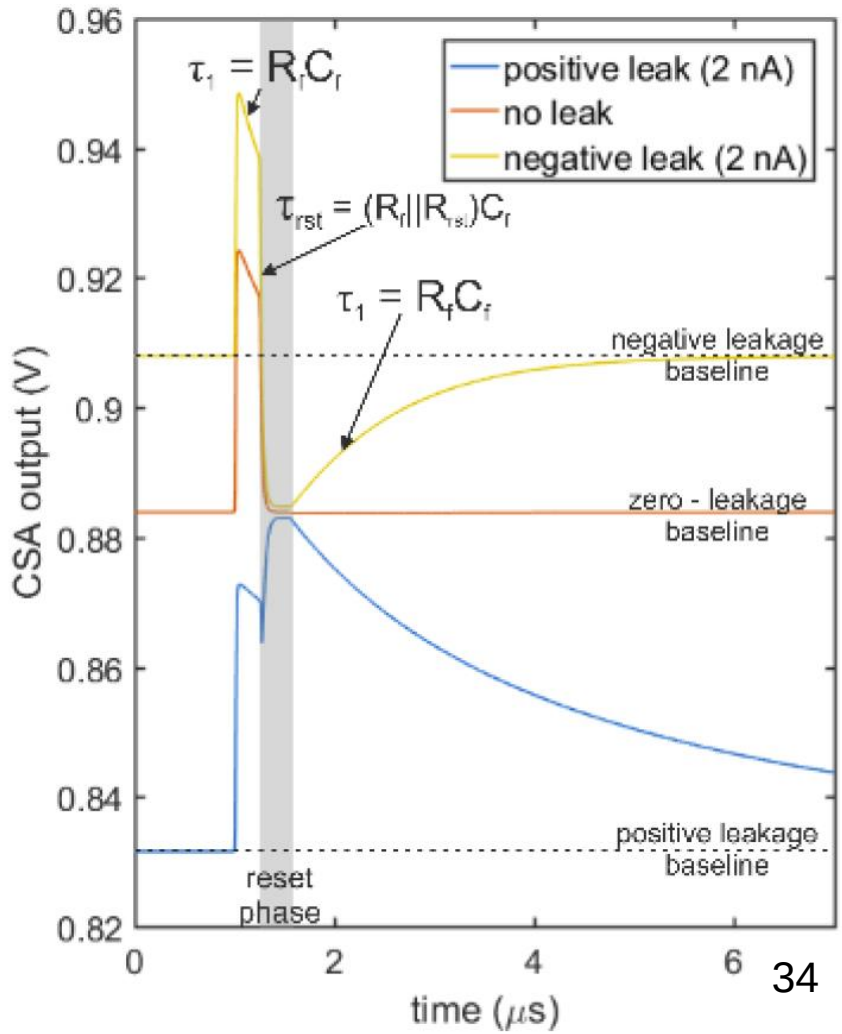
- ESD protection structure leakage (vs. simulation).
- Rad-Hard Memory Cells SEU immunity.
- Input transistor current source reference decoupling.

CSA reset





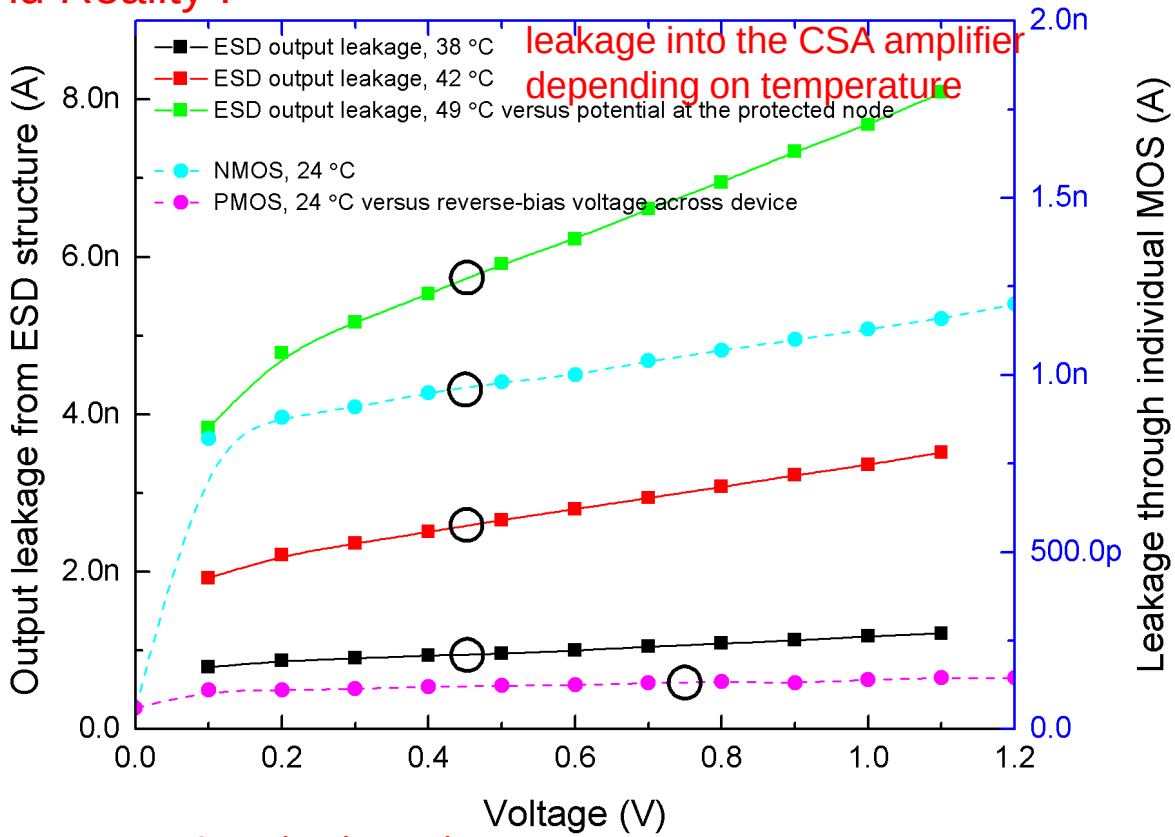
F_{max}~ 600 kHz

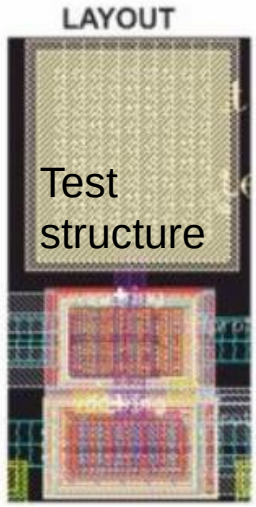


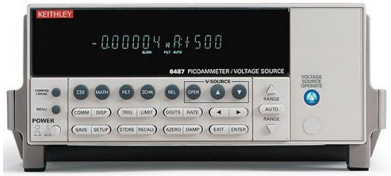
Fast reset – ESD diode leakage

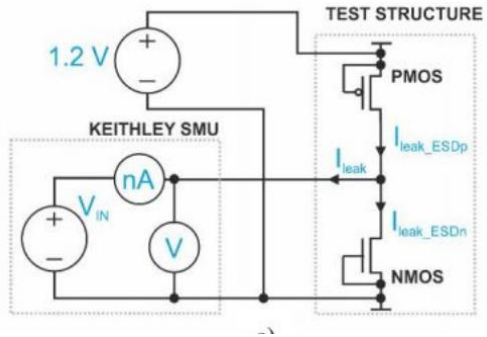
Simulated leakage: I_{leak_total} = 1.3nA , $I_{leak\_to\_amplifier}$=700pA, @ 430mV V_{pad}, 60 ºC.

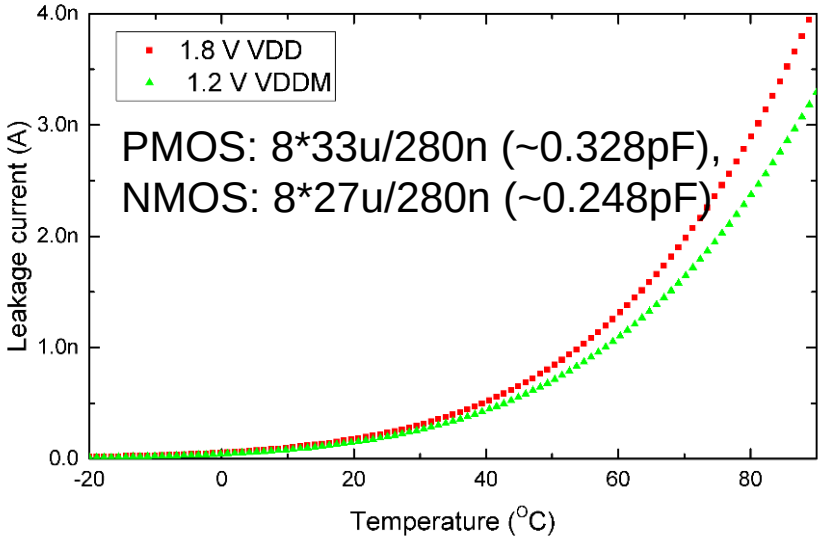
.... and Reality :









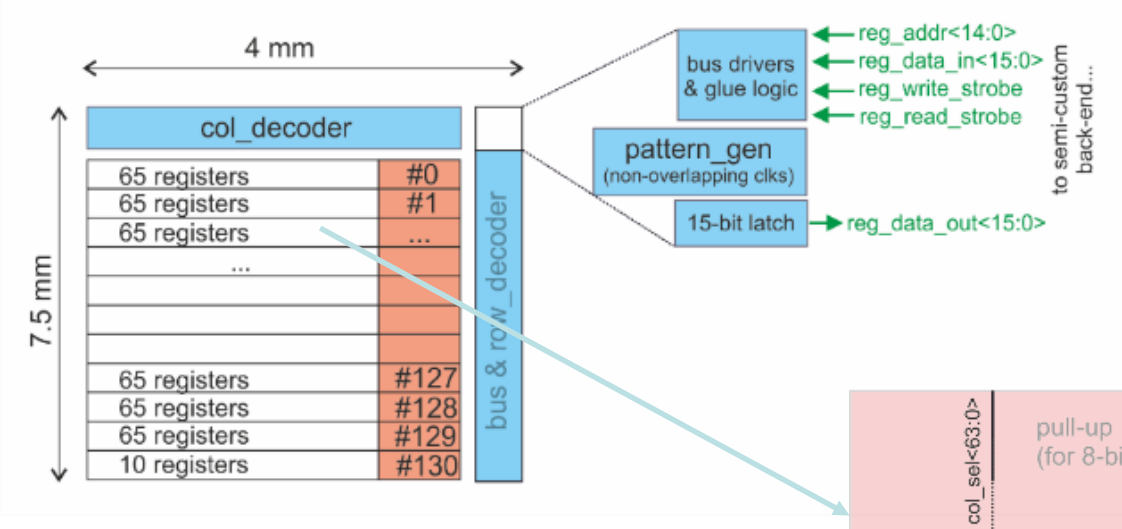


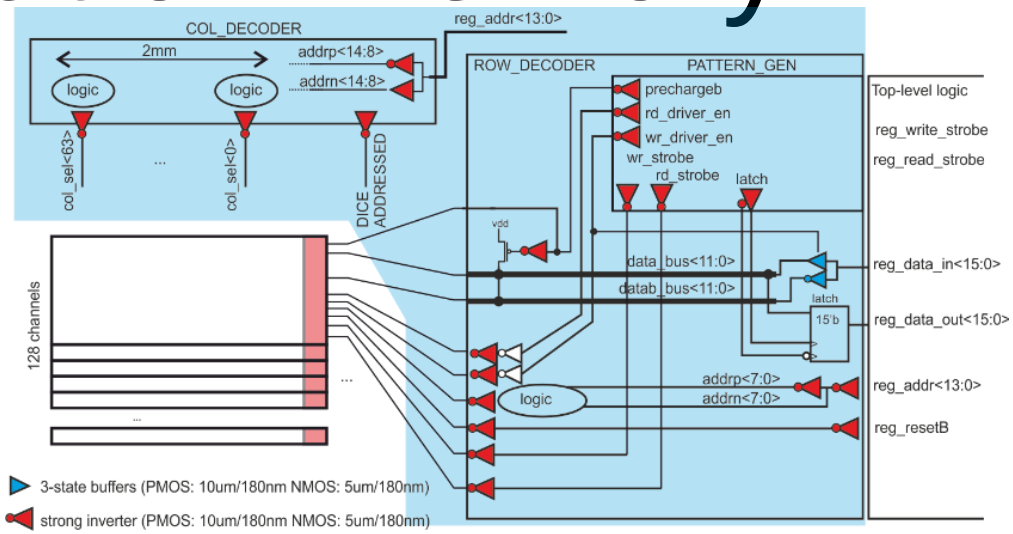
Between 1 nA – 6 nA (and more)
(approx. 8 times more than simulated)
NMOS leaks 10* more than PMOS

Affects:
Noise, Feedback Resistor (speed & noise),
Fast reset (speed)

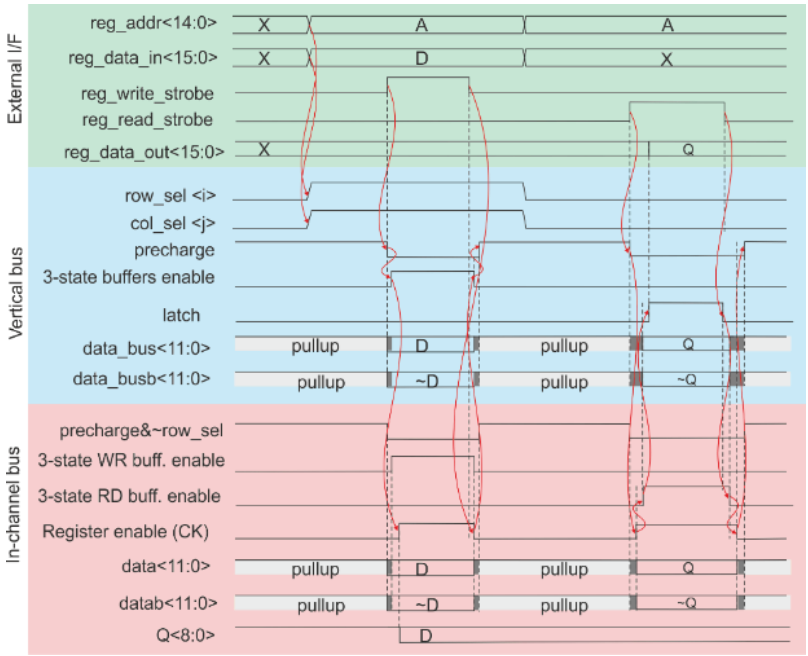
For STS: no protection
For MUCH: external ESD protection chip

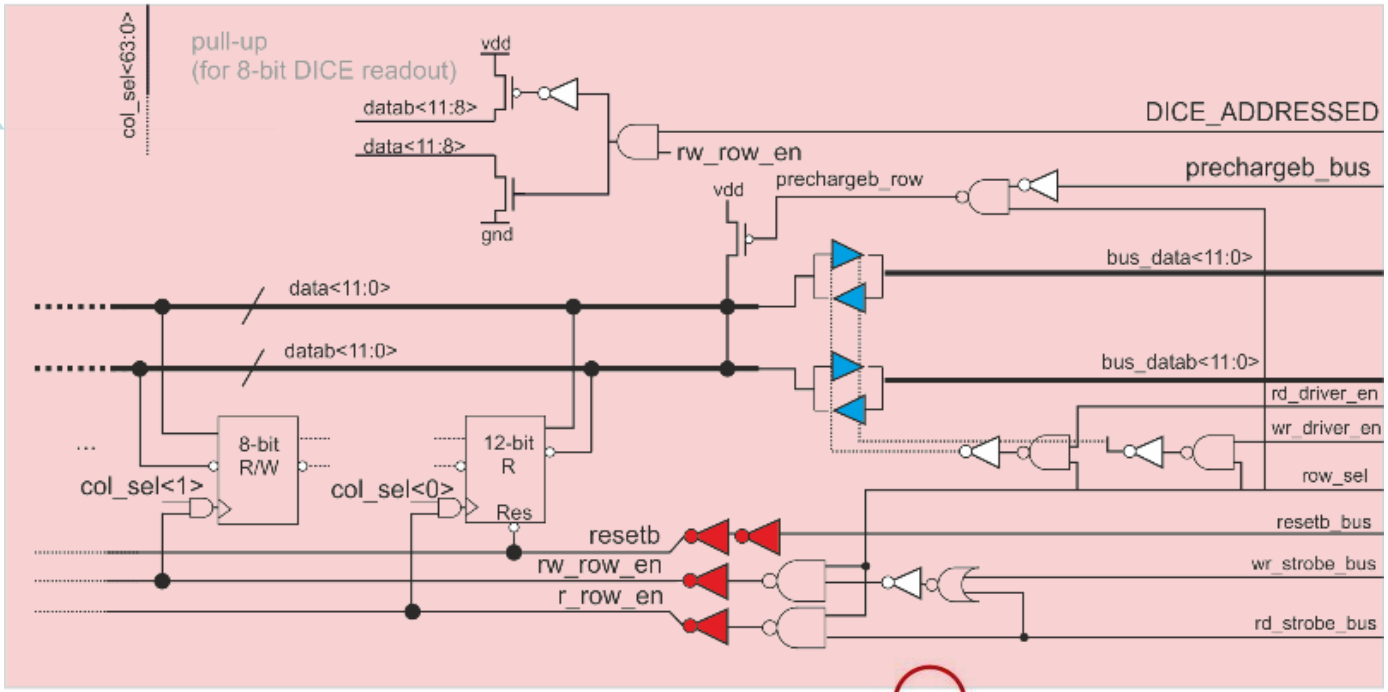
AFE configuration memory





in-channel logic related to register access

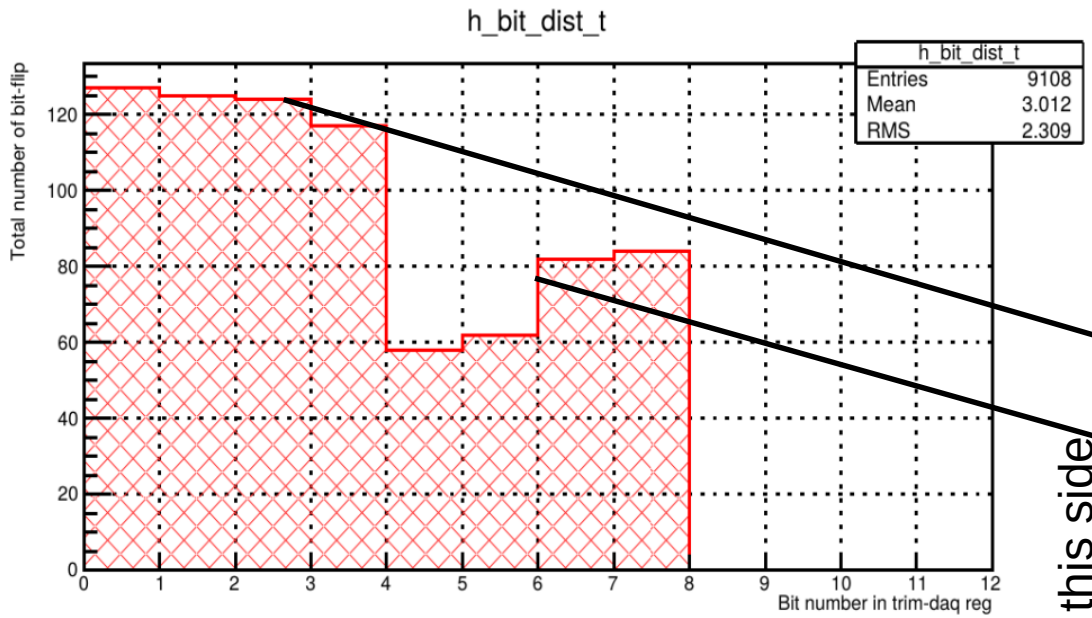




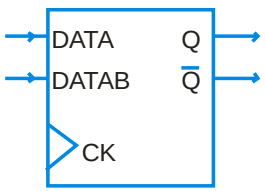
3-state buffers (PMOS: 10um/180nm NMOS: 5um/180nm)

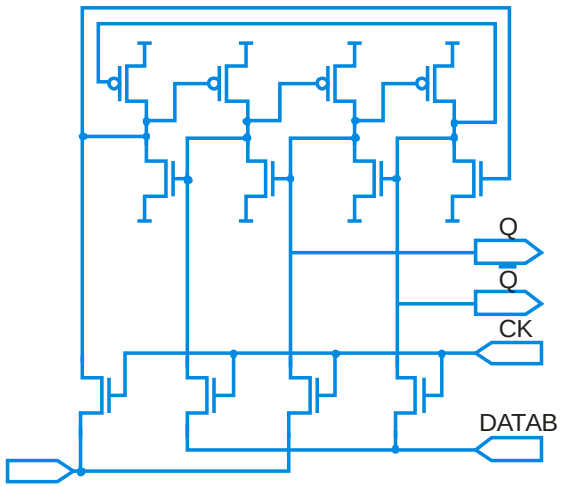
strong inverter (PMOS: 10um/180nm NMOS: 5um/180nm)

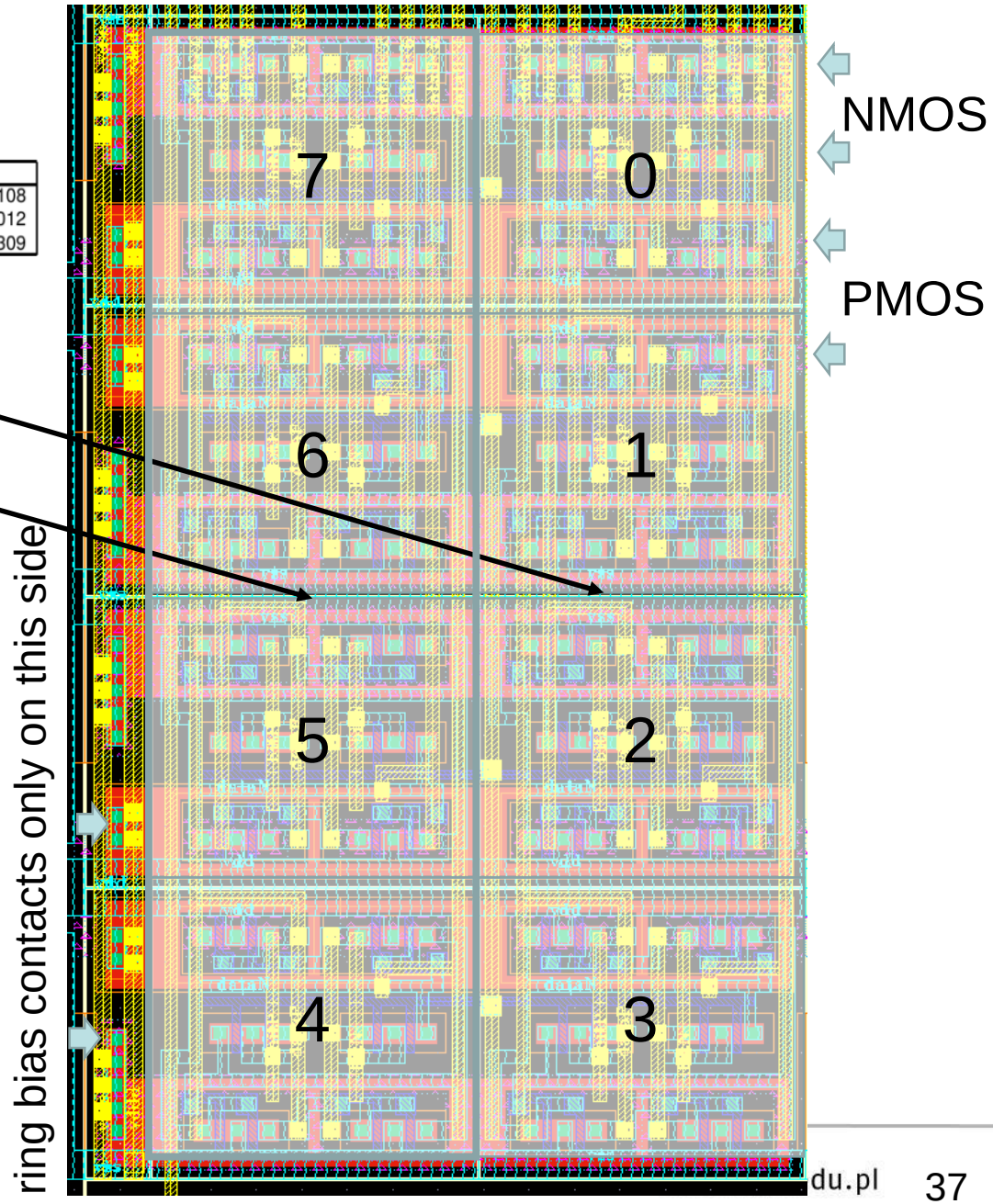
DICE used for AFE configuration memory layout-related SEU immunity



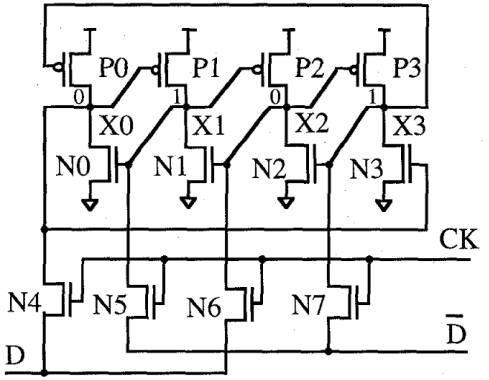
Observation: Better performance for 4-7 bits

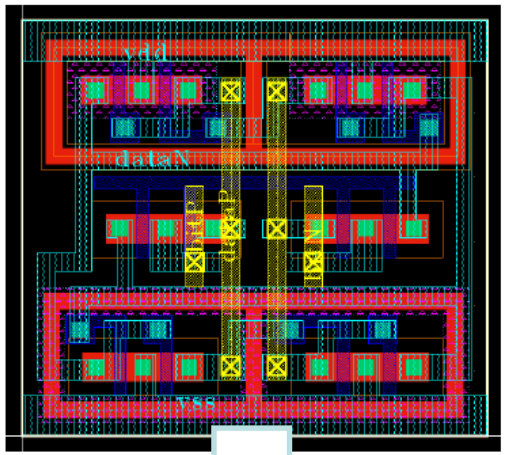




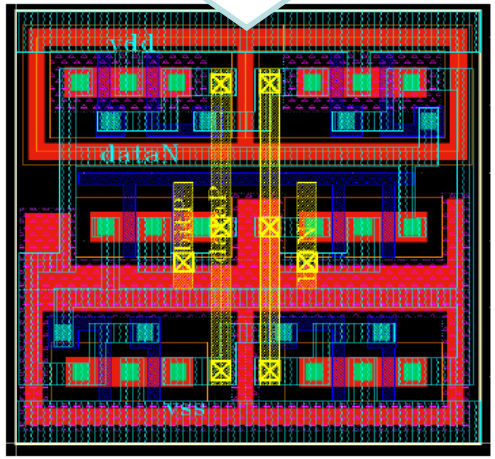


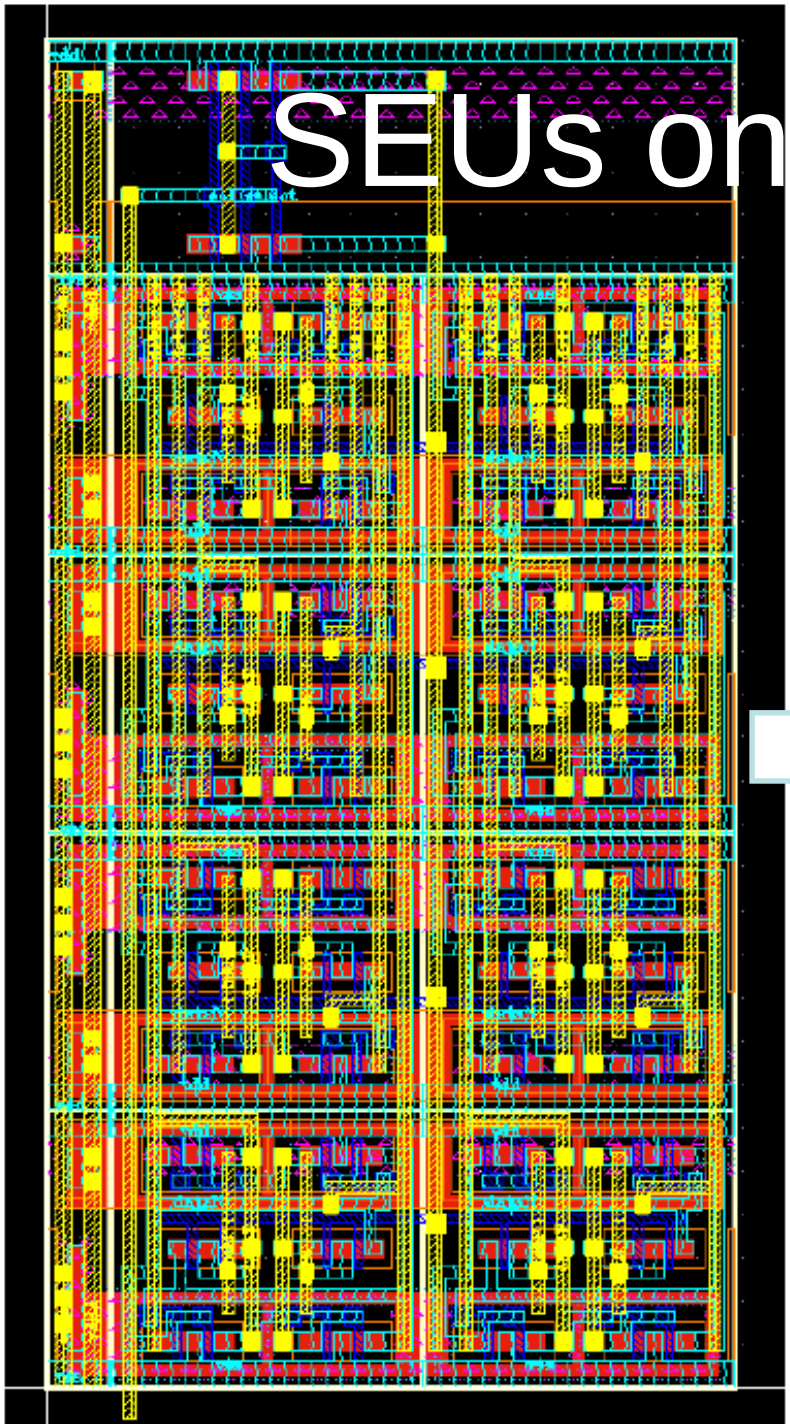
SEUs on DICEs

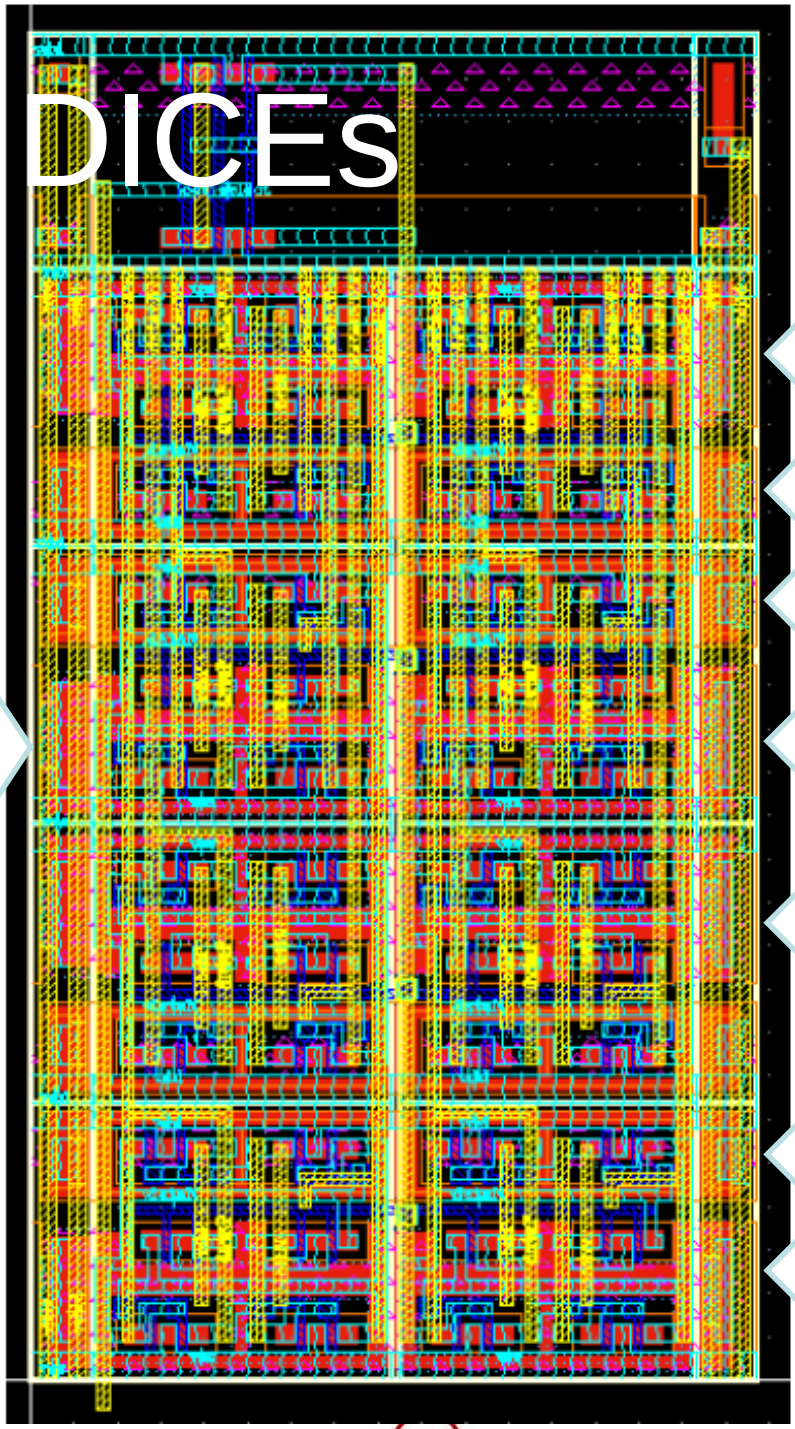




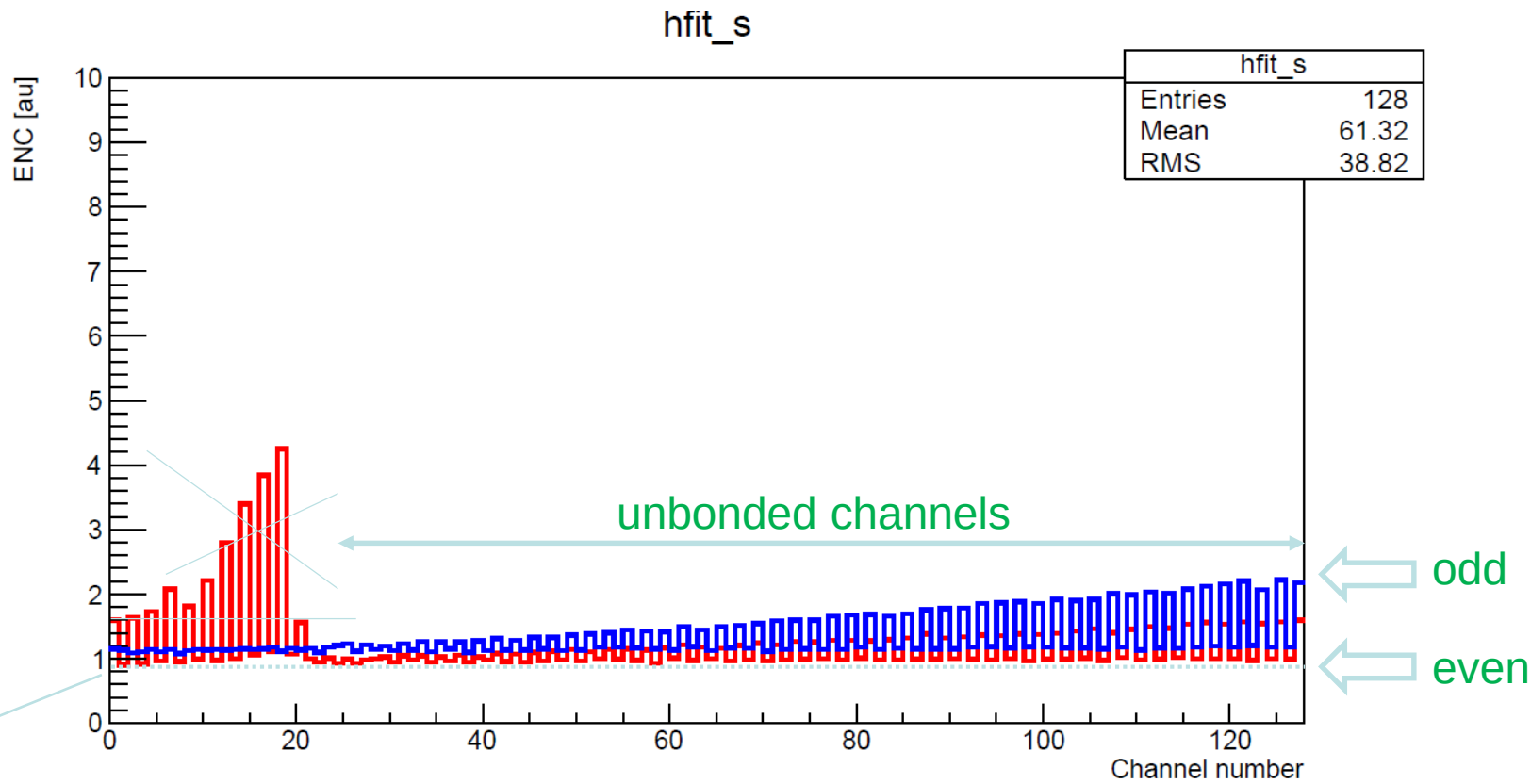
Rys. 3.4. Plan masek kom... ...zed wprowadzeniem zmian





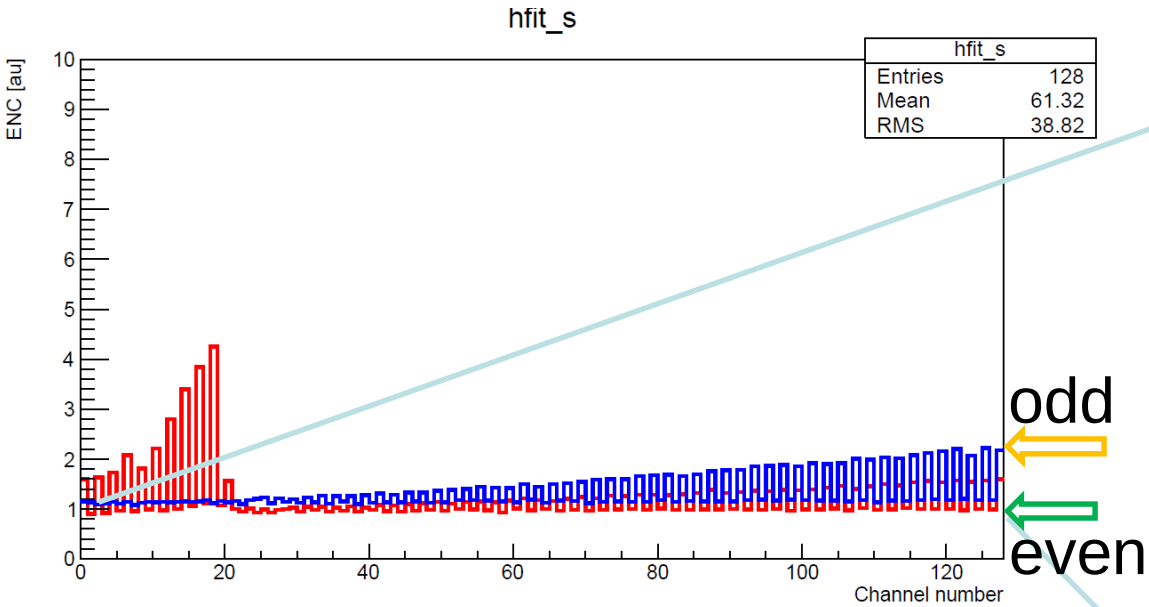


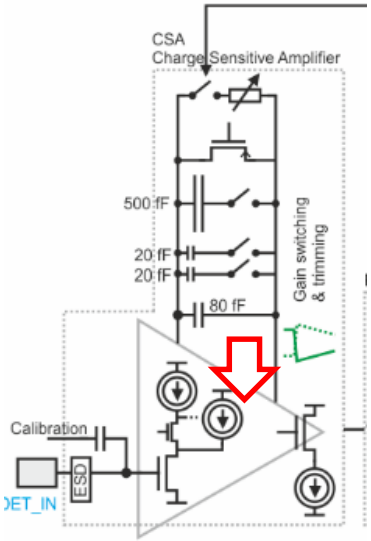
Observation:
Noise difference bewteen even/odd channels



~ 280 e-

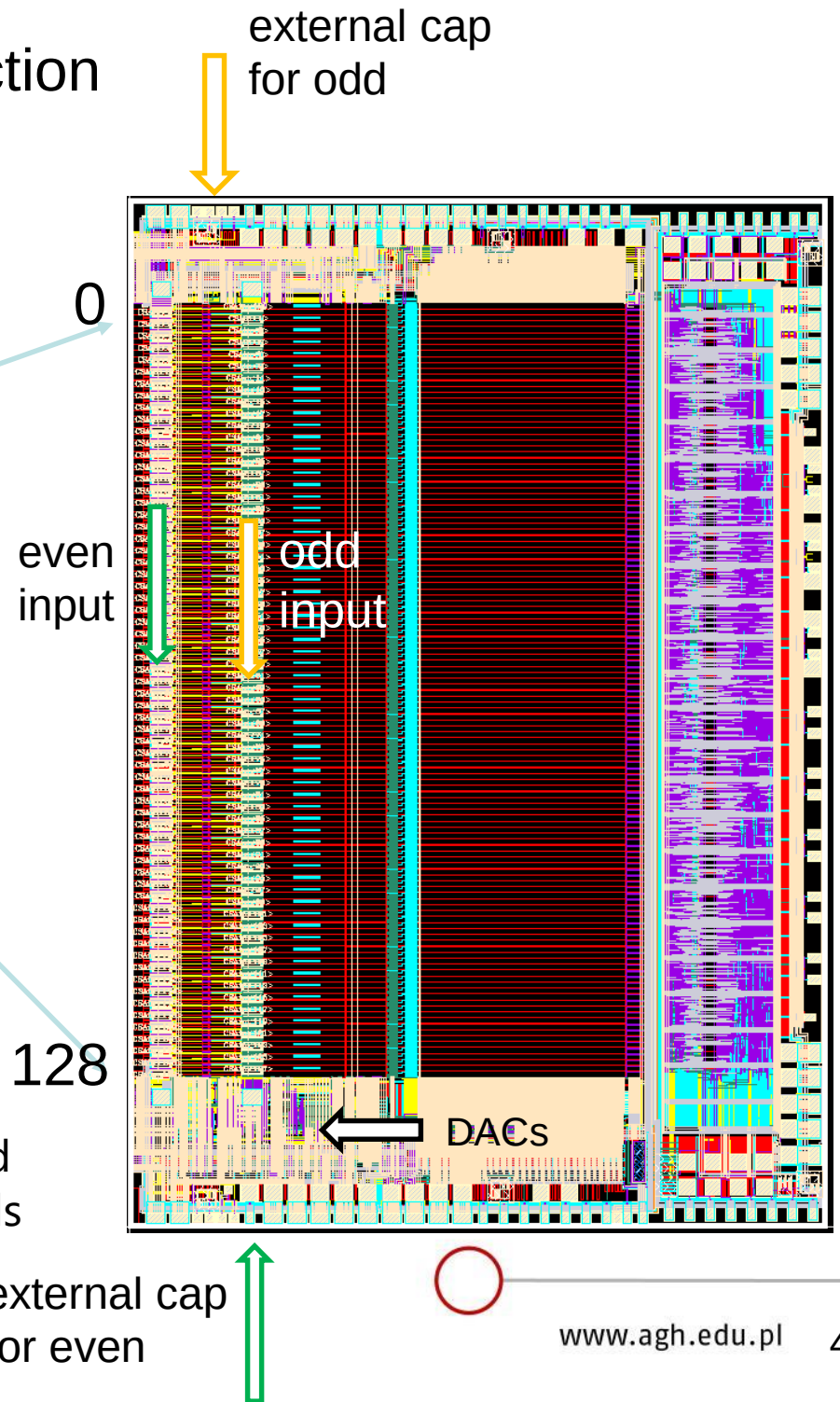
External capacitors for noise reduction



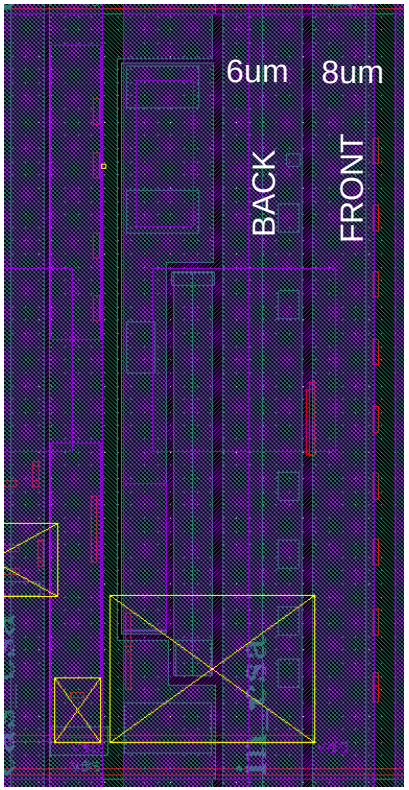


Input transistor current source reference noise is crucial for noise performance.

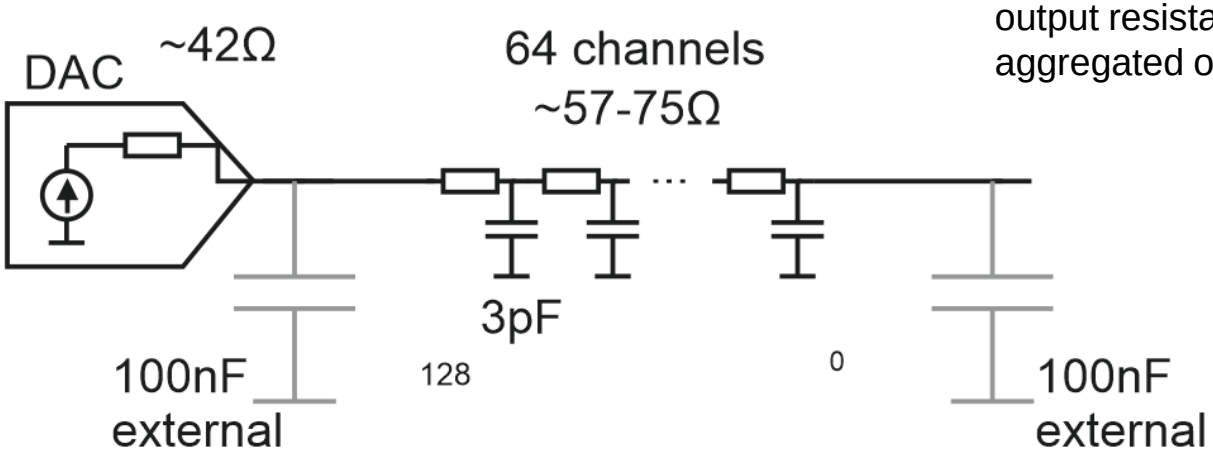
Separate control of input transistor currents in even/odd channels is needed (STS: all channels / MUCH: even channels only).

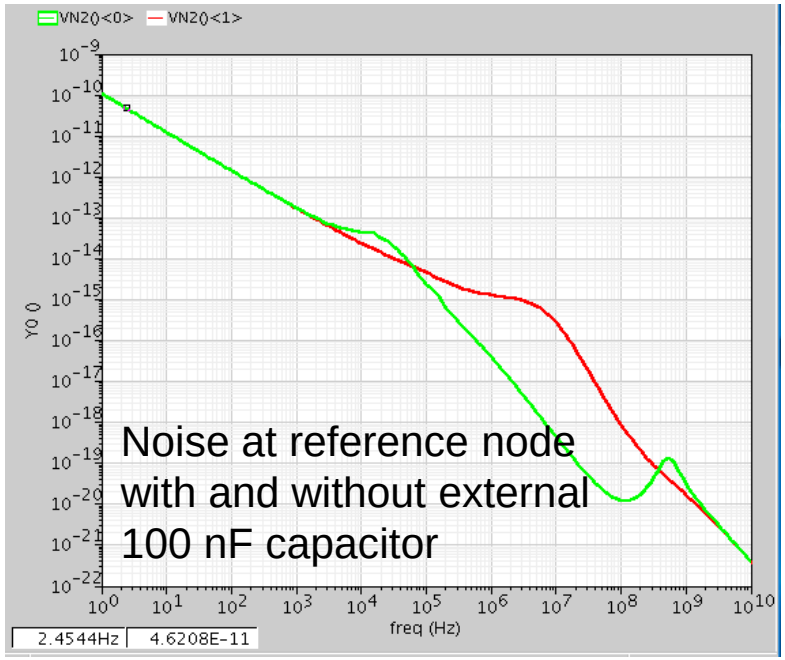


The problem pops-up when DAC has low output resistance (comparable to series R aggregated on the line)



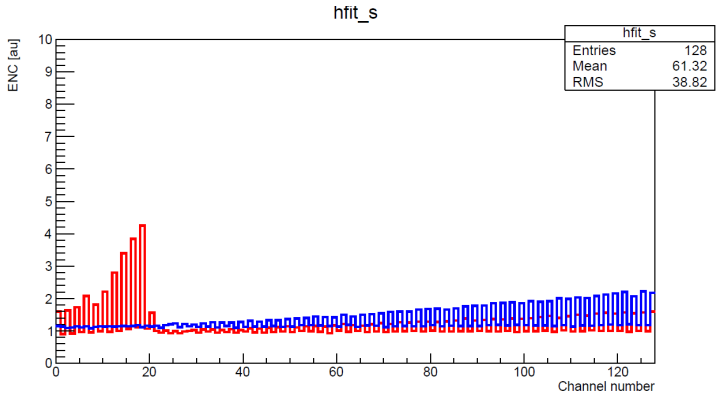
Vertical bias lines.
Sum up to:
57 ohms and 75 ohms





Solution: place external capacitor close to the DAC.

OR
Use in-channel R-C filtering.



Summary

- STS/MUCH-XYTER2 (or SMX2) ASIC was developed, fabricated and tested
  - Long Si microstrip sensors & GEM read-out
  - Self-triggered read-out
  - Dedicated for STS/MUCH Detectors in the CBM experiment

- New version (SMX2.1)
  - Submission -> june 2018
  - High-volume production planned Q1 2018

- Caveats were presented:
  - ESD leakage much different than simulation
  - Negative effect on pused reset circuits
  - Layout-related effects on DICE memory SEU immunity
  - Importance of DAC noise filter placement when small R_{out}.

Parameter	Value
Names	STS/MUCH-XYTER2 / SMX2
Process	180 nm CMOS MM/RF
Chip area	10.0 mm × 6.75 mm
Channel number	128 + 2 test
ADC bits	5
Input charge frequency	max. 500 kHz
Power Consumption: Uninitialized Initialized	 0.6 – 1.2 W/chip 1.023 W/chip @ I_d=2 mA 8 mW/channel
Offset spread of fast channel	1.12 mV rms / 0.015 fC rms (after correction)
Offset spread of ADC [fC]	0.09 (before correction) [39] 0.02 (after correction)
Gain Fast shaper (STS) Slow shaper (STS)	 73 mV/fC 32.7 mV/fC
Gain spread: Fast shaper Slow shaper	 0.8 % 0.5 % (after calibration)
ENC (Equivalent Noise Charge) Fast shaper Slow shaper	 44 e^-/pF + 583 e^- rms 27 e^-/pF + 538 e^- rms
Slow shaper peaking time [ns]	90 / 180 / 262 / 332
Yield	>91% (146 ASICs tested on PCBs)

Thank you for your attention

Acknowledgements:
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GSI, Darmstadt, Germany: M. Teklishyn, A. Lymanets, M. Dogan, A. Weiss, C. Simons, W. F. Müller

http://www.kmet.agh.edu.pl/katedra-metrologii/zespoly-badawcze/asics/?lang=en

List of STS/MUCH-XYTER related papers

- [GSI-2013-05499] Technical Design Report for the CBM Silicon Tracking System (STS), GSI, Darmstadt, 2013. http://repository.gsi.de/record/54798.
- [GSI-2015-02580] Technical Design Report for the CBM Muon Chambers, GSI, Darmstadt, (2015), http://repository.gsi.de/record/161297
- CBM Progress Report 2015, Darmstadt (2016).
- CBM Progress Report 2016, Darmstadt (2017).
- CBM Progress Report 2017, Darmstadt (2018).
- W. Zubrzycka, K. Kasinski, “Performance Evaluation of the Detector and Ultra-Light Micro-cable Assembly for Tracking Application in the CBM experiment”, Proc. SPIE, vol 10445 (2017).
- K. Kasinski, R. Kleczek, C.J. Schmidt, Optimization of the microcable and detector parameters towards low noise in the STS readout system, in: Proc. SPIE - Int. Soc. Opt. Eng., 2015. doi:10.1117/12.2205699.
- K. Kasinski, R. Szczygiel, W. Zabolotny, J. Lehnert, C.J. Schmidt, W.F.J. Müller, A protocol for hit and control synchronous transfer for the front-end electronics at the {CBM} experiment, Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip. 835 (2016) 66–73. doi:http://dx.doi.org/10.1016/j.nima.2016.08.005.
- J. Lehnert, A.P. Byszuk, D. Emschermann, K. Kasinski, W.F.J. Müller, C.J. Schmidt, R. Szczygiel, W.M. Zabolotny, GBT based readout in the CBM experiment, J. Instrum. 12 (2017) C02061. http://stacks.iop.org/1748-0221/12/i=02/a=C02061.
- R. Kleczek, Analog front-end design of the STS/MUCH-XYTER2—full size prototype ASIC for the CBM experiment, J. Instrum. 12 (2017) C01053. http://stacks.iop.org/1748-0221/12/i=01/a=C01053.
- K. Kasinski, R. Szczygiel, W. Zabolotny, Back-end and interface implementation of the STS-XYTER2 prototype ASIC for the CBM experiment, J. Instrum. 11 (2016) C11018. http://stacks.iop.org/1748-0221/11/i=11/a=C11018.
- K. Kasinski, R. Kleczek, R. Szczygiel, Front-end readout electronics considerations for Silicon Tracking System and Muon Chamber, J. Instrum. 11 (2016). doi:10.1088/1748-0221/11/02/C02024.
- K. Kasinski, R. Kleczek, A flexible, low-noise charge-sensitive amplifier for particle tracking application, 2016 Mixdes - 23rd Int. Conf. Mix. Des. Integr. Circuits Syst., 2016: pp. 124–129. doi:10.1109/MIXDES.2016.7529715.
- Zubrzycka, W., & Kasinski, K. (2018). Leakage current-induced effects in the silicon microstrip and gas electron multiplier readout chain and their compensation method. *Journal of Instrumentation*, *13*(4), T04003. Retrieved from http://stacks.iop.org/1748-0221/13/i=04/a=T04003
- P. Otfinowski, P. Grybos, R. Szczygiel, K. Kasinski, Offset correction system for 128-channel self-triggering readout chip with in-channel 5-bit energy measurement functionality, Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip. 780 (2015) 114–118. doi:http://dx.doi.org/10.1016/j.nima.2015.01.048.
- K. Kasinski, W. Zubrzycka, Test systems of the STS-XYTER2 ASIC: from wafer-level to in-system verification, Proc. SPIE. 10031 (2016) 100313N–100313N–10. doi:10.1117/12.2249137.
- W.M. Zabołotny, A.P. Byszuk, D. Emschermann, M. Gumiński, B. Juszczyk, K. Kasiński, G. Kasprowicz, J. Lehnert, W.F.J. Müller, K. Poźniak, R. Romaniuk, R. Szczygieł, Design of versatile ASIC and protocol tester for CBM readout system, J. Instrum. 12 (2017) C02060. http://stacks.iop.org/1748-0221/12/i=02/a=C02060.
- K. Kasinski, P. Koczon, S. Ayet, S. Löchner, C.J. Schmidt, System-level considerations for the front-end readout ASIC in the CBM experiment from the power supply perspective, J. Instrum. 12 (2017) C03023. http://stacks.iop.org/1748-0221/12/i=03/a=C03023.