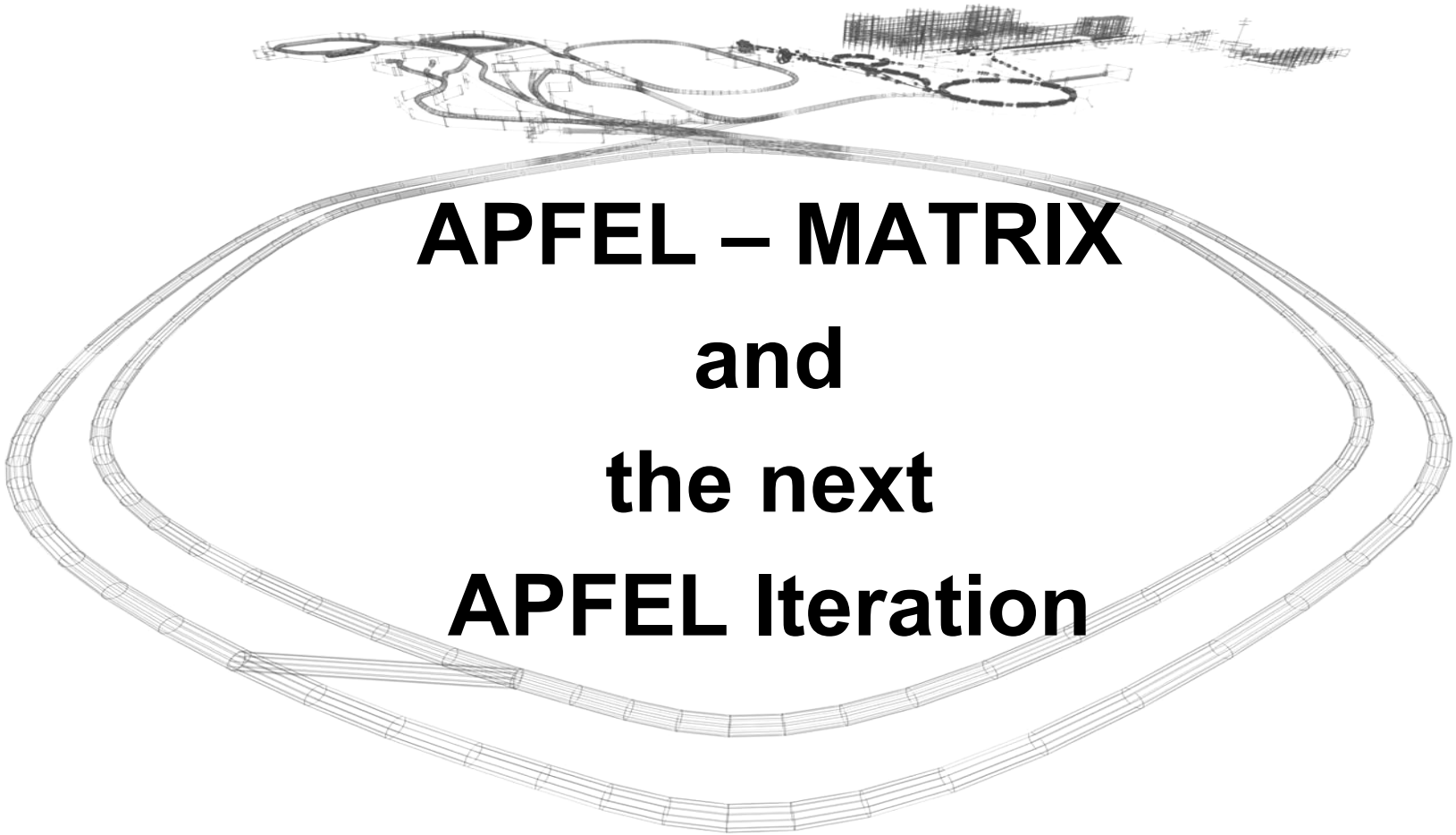
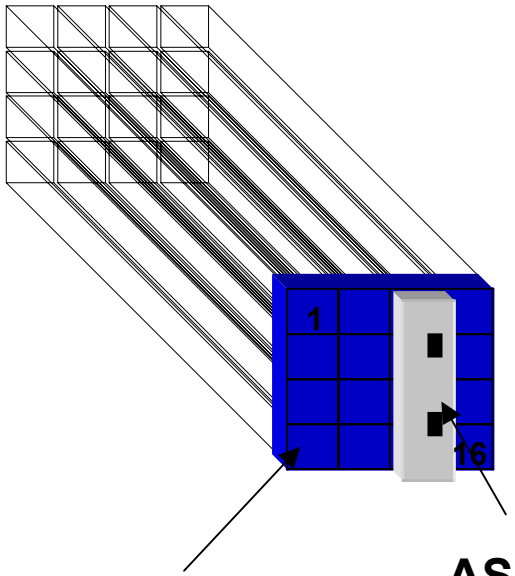


APFEL – MATRIX
and
the next
APFEL Iteration

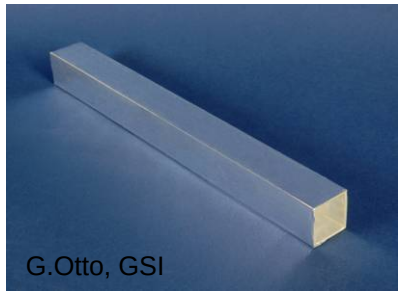
Overview

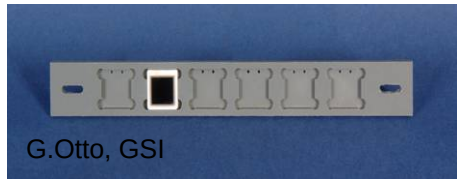
1. APFEL – MATRIX
    - Setup of 16 crystals
    - Readout system
    - Data acquisition
2. Next APFEL Iteration
    - APFEL design 2010
    - Outlook

APFEL - MATRIX

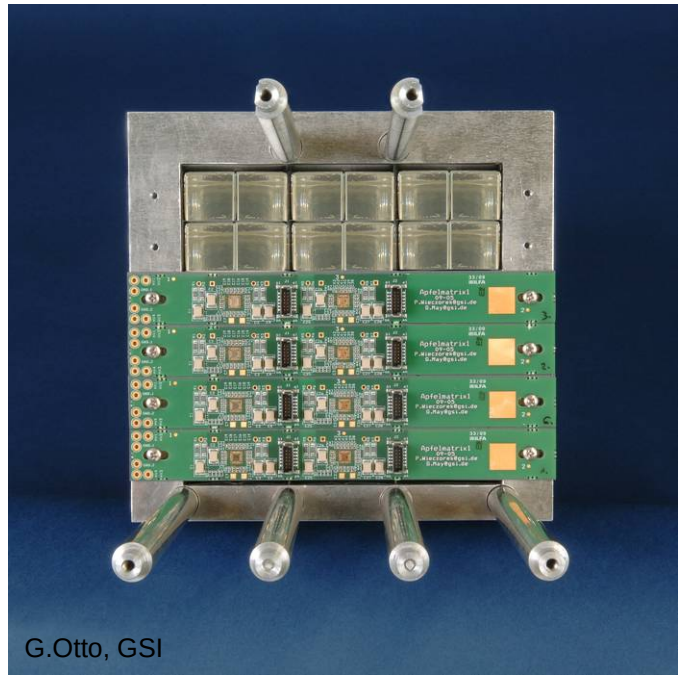


APD matrix

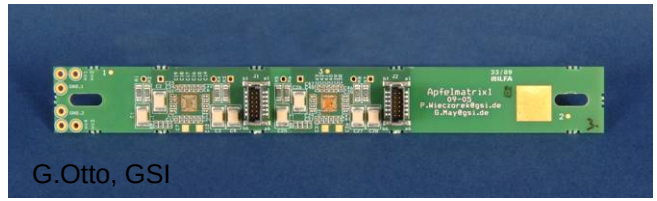




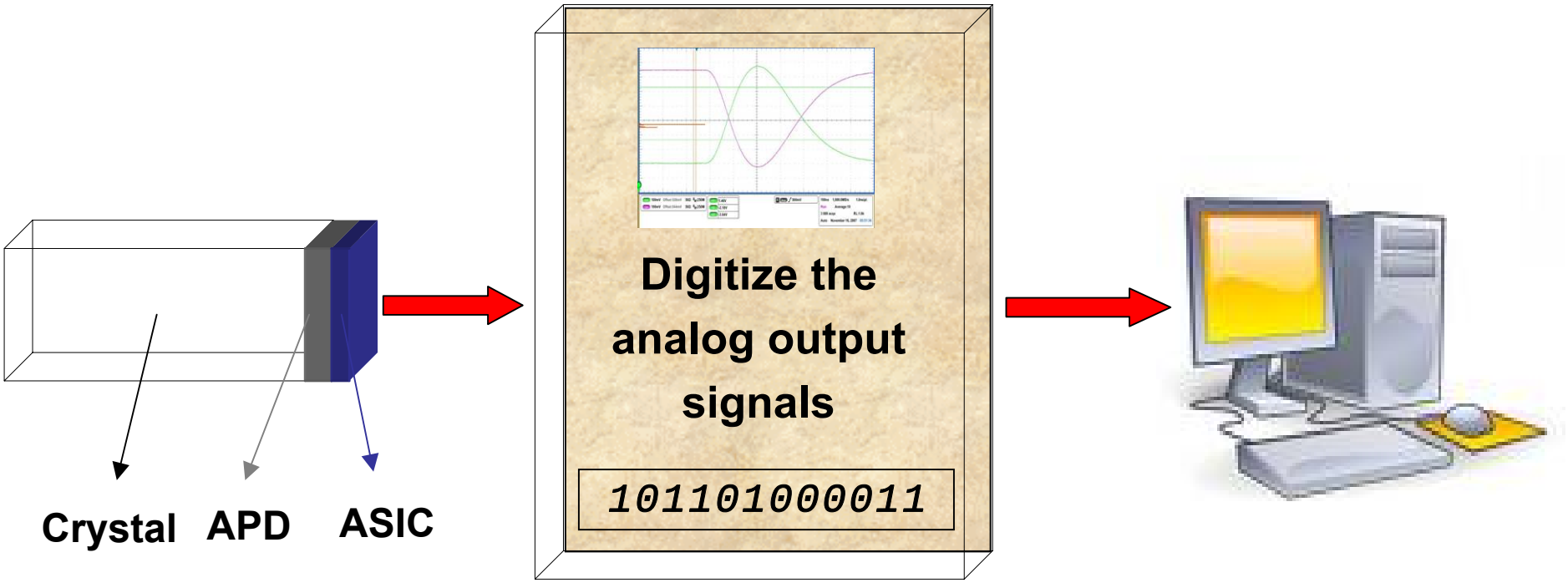
ASIC on a PCB



- **Matrix readout**
  - **16 channels (one APD per crystal)**
  - **Separate high voltages**
  - **Two channel read out by one ASIC**

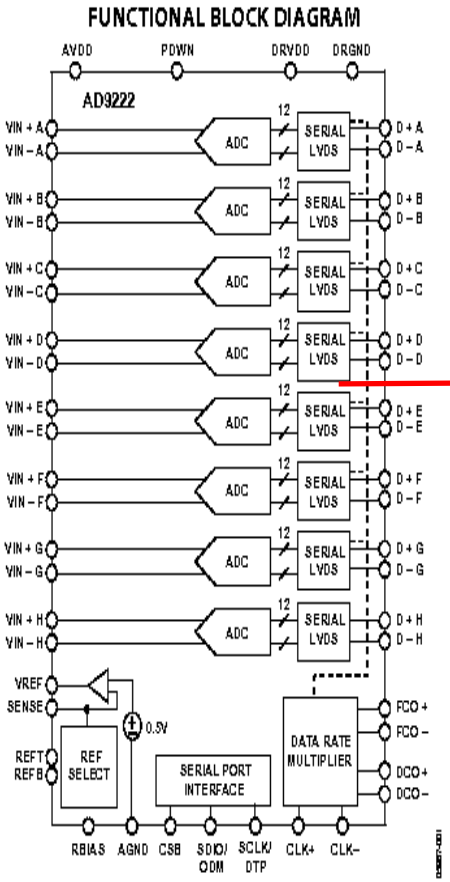


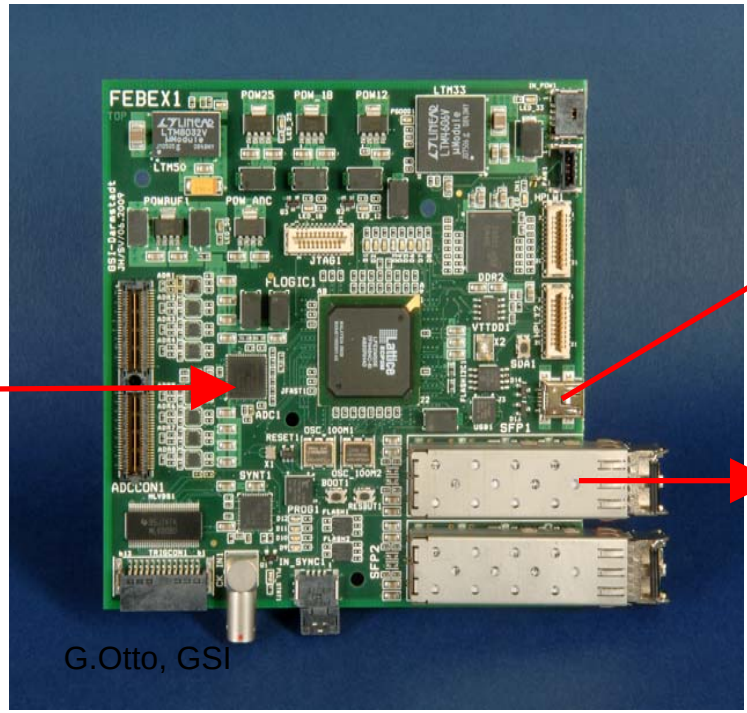
DAQ



- For the digitization
  → FEBEX – Board developed at GSI is used

FEBEX - Board Developed by J.Hoffmann



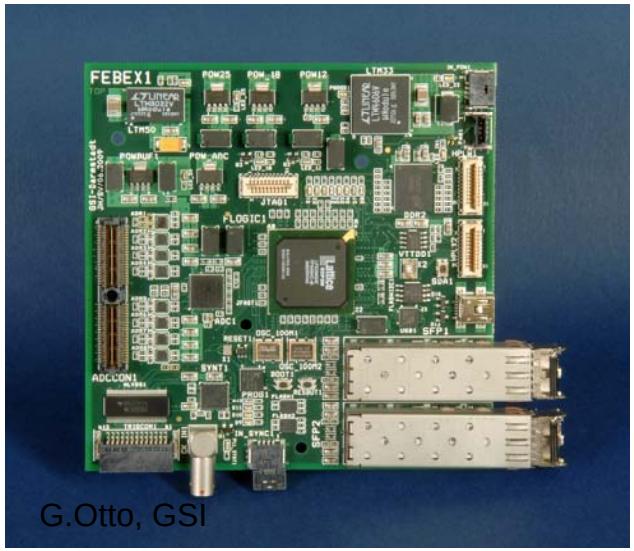


LAB:
USB - Interface

Optical Gbit Interface to DAQ

- 8 differential analog inputs
- ADC input range: ± 1 V
- ADC: 12 Bit, 65 MS/s
- 2 x 2.5 Gbit/s optical interface

FEBEX 2010



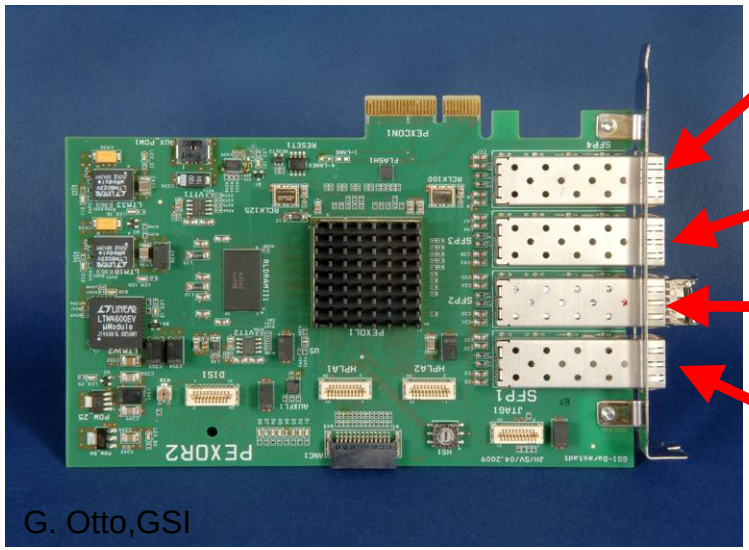
- **Existing FEBEX – Board is a first prototype**
  - Pulse shape analysis on the FPGA in development
  - 8 channels readout version
  - Internal FPGA memory buffer is large enough for 8 (30) µs traces

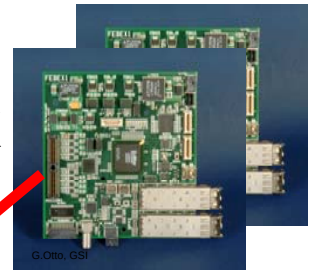
- **Next FEBEX - Board (design 2010)**
  - Upgrade to 16 (32) channels
  - More powerful FPGA
  - Pulse shape analysis on the FPGA (will be done at KVI)
  - Compatible ADCs (10, 12 or 14 Bit; 50 -100 MS/s)
  - Larger memory (store more than 30 µs time information)
  - Prototype for a readout of 400 channels

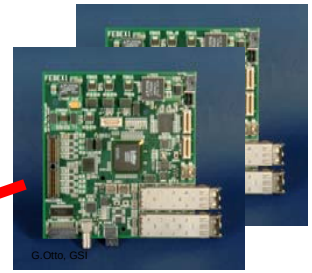
PEXOR – FEBEX Connection

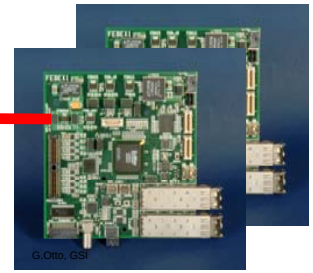
FEBEX

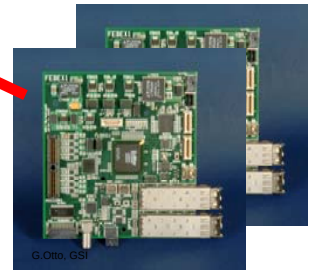
PEXOR – Board (PCIe)











4x up to
16 FEBEX
in series

- PEXOR – Board was designed by Jan Hoffmann
- Programming was done by Wolfgang Ott

DAQ Summary

To measure 16 differential outputs from the APFEL – Matrix existing DAQ components from GSI are used

- **Digitization and data transport: FEBEX – PEXOR – Board (contact: Jan Hoffmann)**
- **DAQ – System: Multi Branch System (MBS) (contact: Wolfgang Ott, Nikolaus Kurz, *http://www-win.gsi.de/daq/)***
- **Online monitoring / offline analysis: GSI Object Oriented On-line Off-line system (GO4) (contact: Jörn Adamczewski-Musch, *http://www-win.gsi.de/go4/*)**

Go4 MATRIX Display

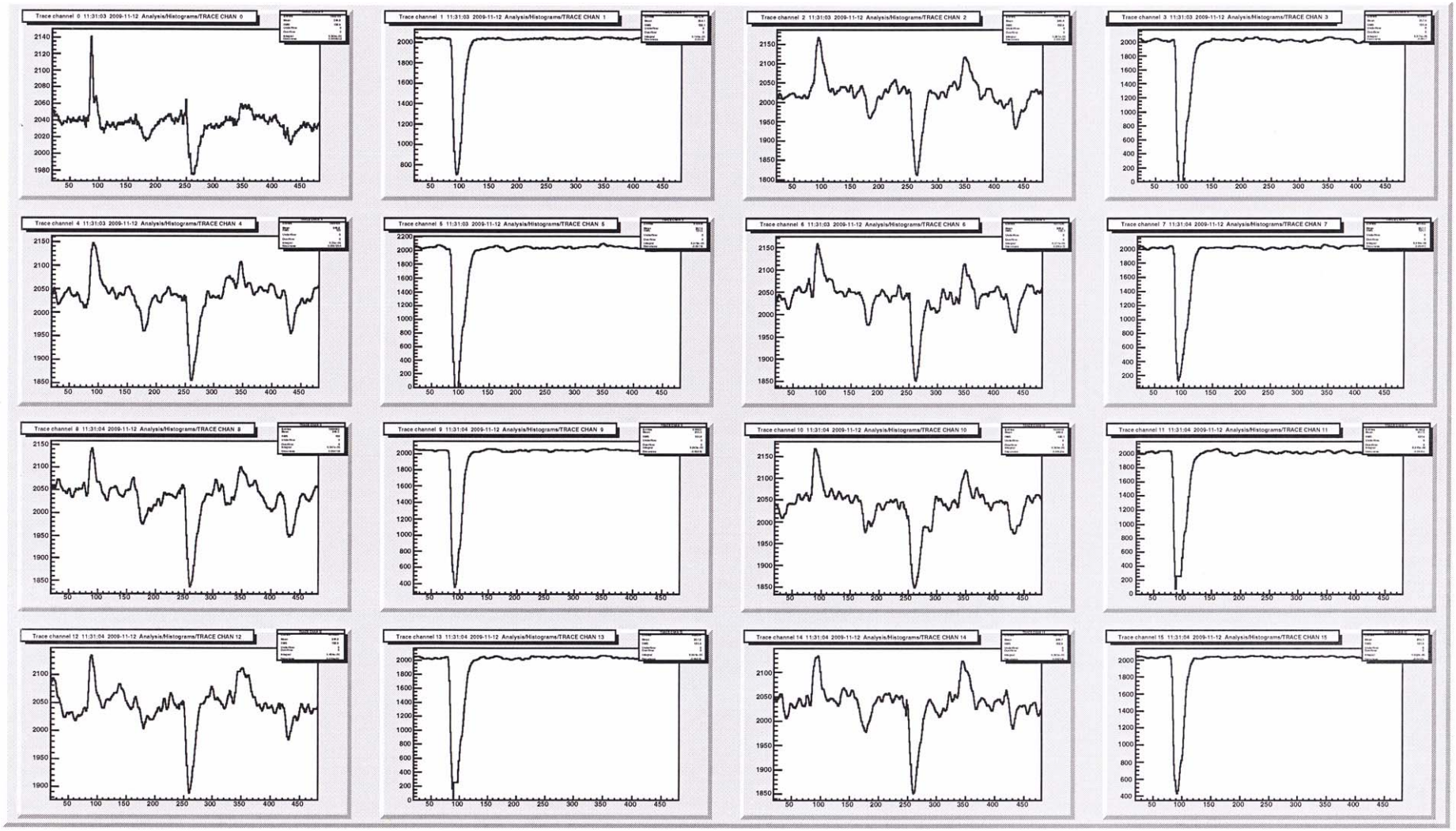
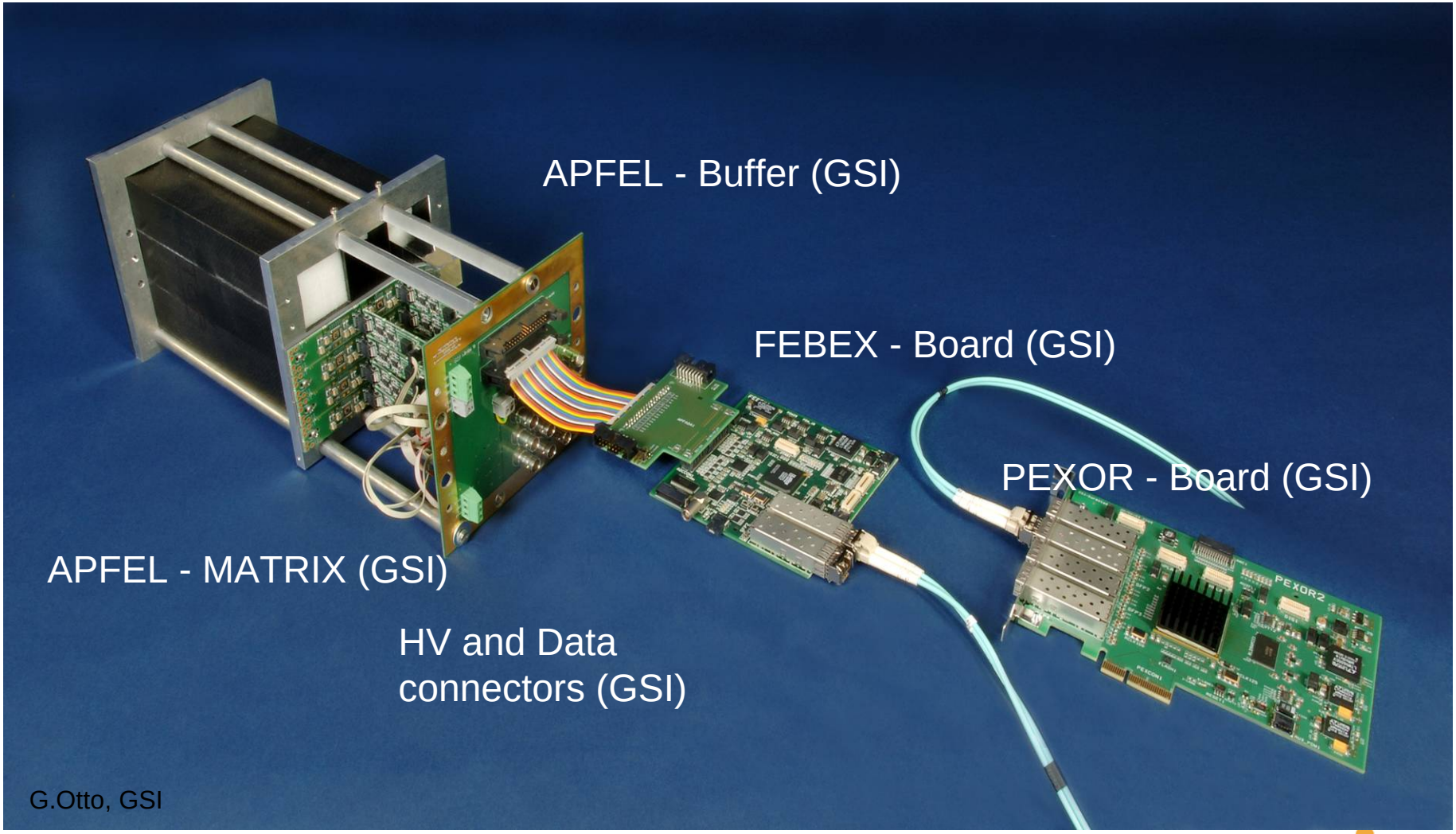
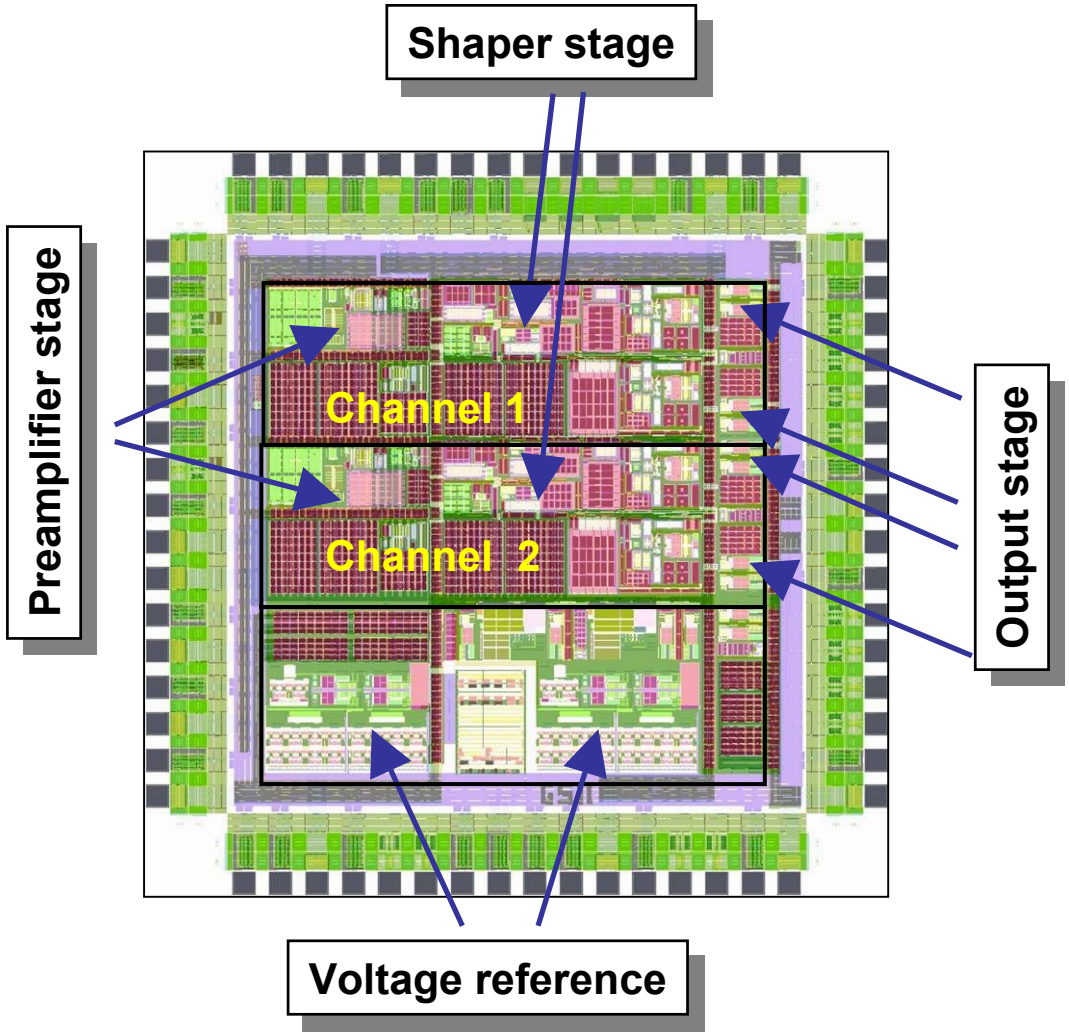


Photo of the APFEL - MATRIX Setup



Next Iteration of the APFEL - ASIC

Layout of the existing ASIC



- Process: 350 nm – CMOS (AMS)
- Two equivalent readout channels
- Programmable voltage references
- Dimension: 3.3 mm x 3.3 mm
- Pad connections: 64

Next Iteration

- APFEL03: Manuel voltage reference progamming with lookup tables for different temperatures is necessary
  → An autocalibration has been developed
- To operate the high and low amplification path of a channel in parallel an additional voltage reference DAC has been implemented
- For chip identification
  → Bugfix in chip – ID selection
- Open question: Output buffer ??? (final call !!)
- Status of the next APFEL – iteration:
  - Schematic review is done
  - Layout of the chip is in progress

Outlook

- First cosmic tests with the APFEL – MATRIX (Spring 2010)
- Submission of the next APFEL – ASIC iteration (Spring 2010)
- Commissioning of next APFEL iteration (Summer 2010)
- Do we need additional ASICs for further tests (more than 20)?