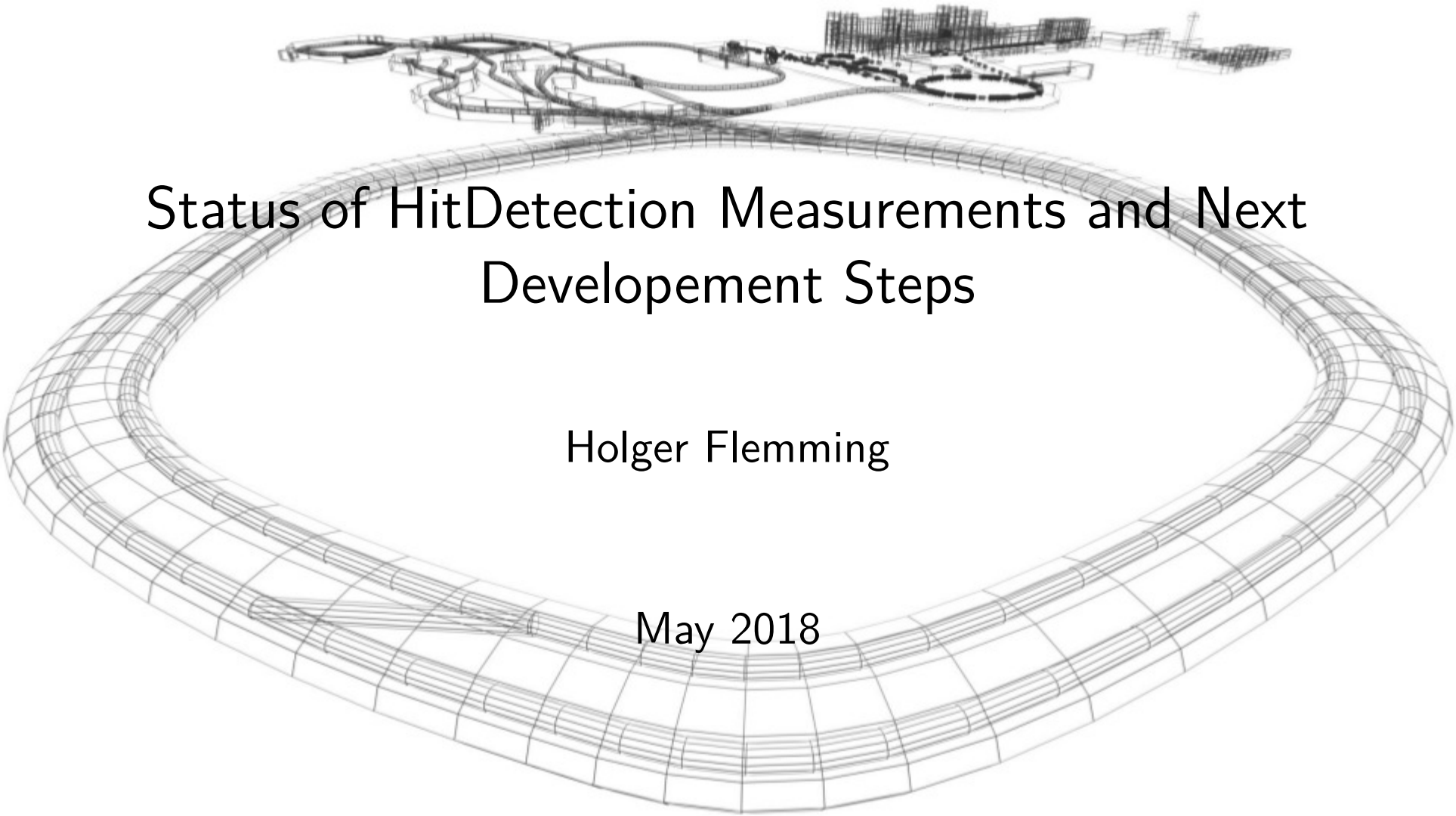


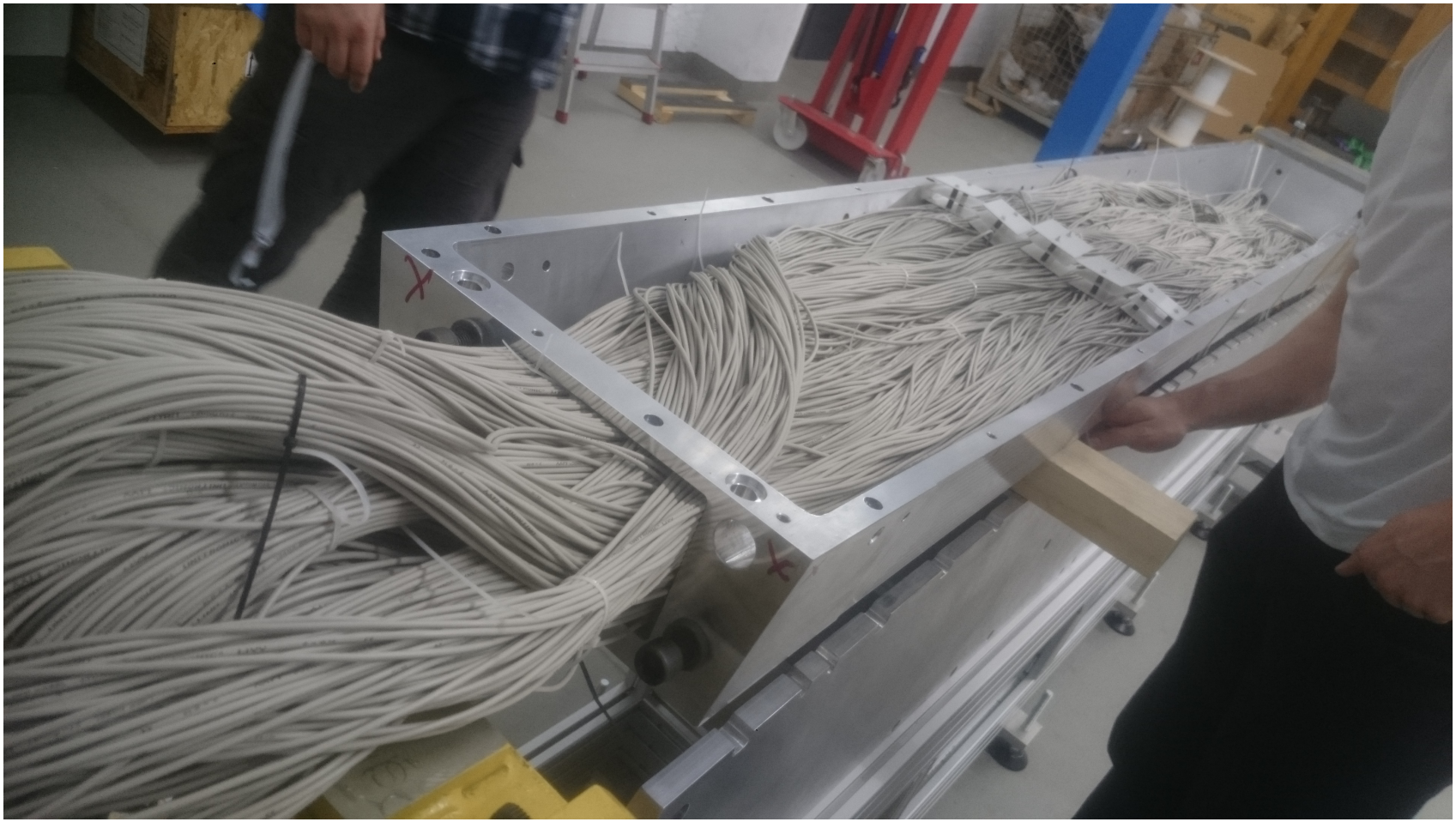
Status of HitDetection Measurements and Next Developement Steps

Holger Flemming

May 2018

Outline

Outline



Courtesy of Markus Moritz, Uni Giessen

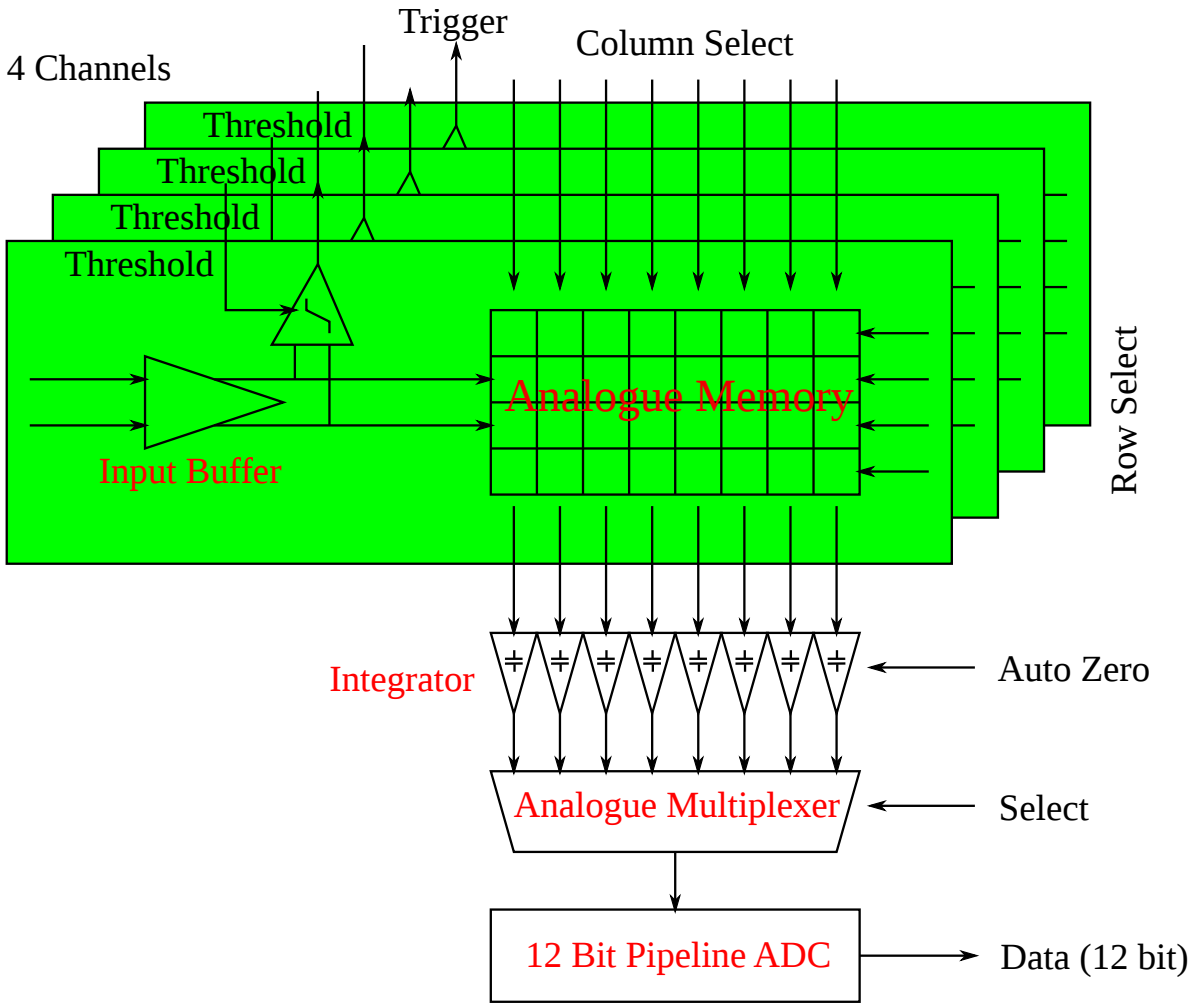
Required cables

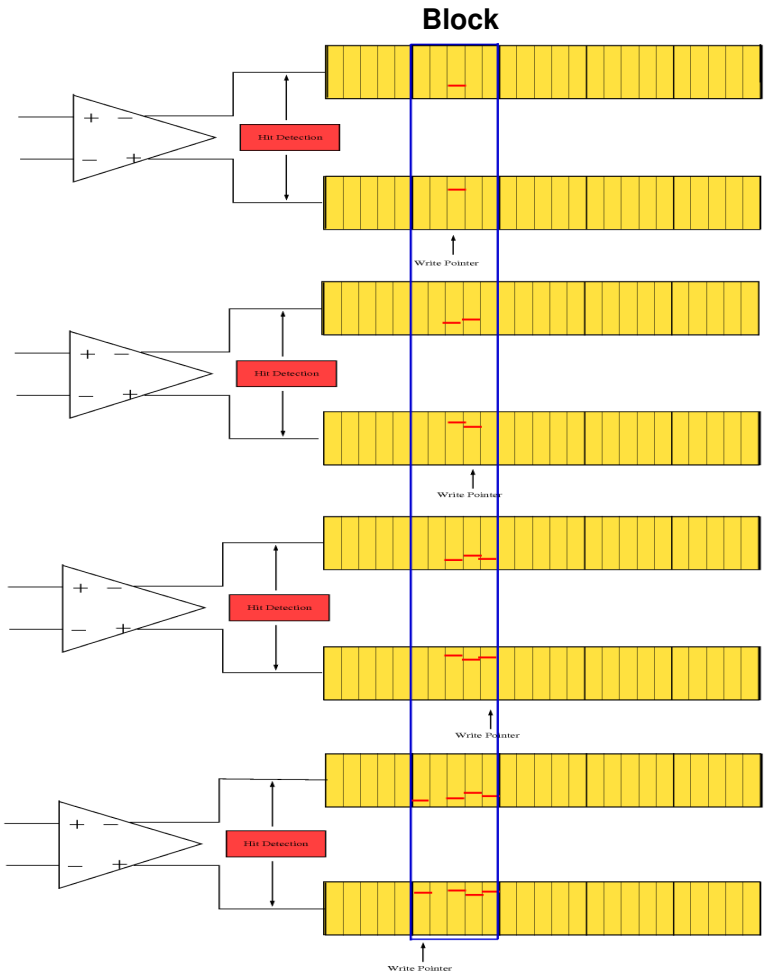
	ext. ADC	HitDet.
Analogue Signals	16 pairs	
SerialAdapter	4 pairs	
Serial clock		1 pair
Upstream data		1 pair
Downstream data		1 pair
	20 pairs	3 pairs

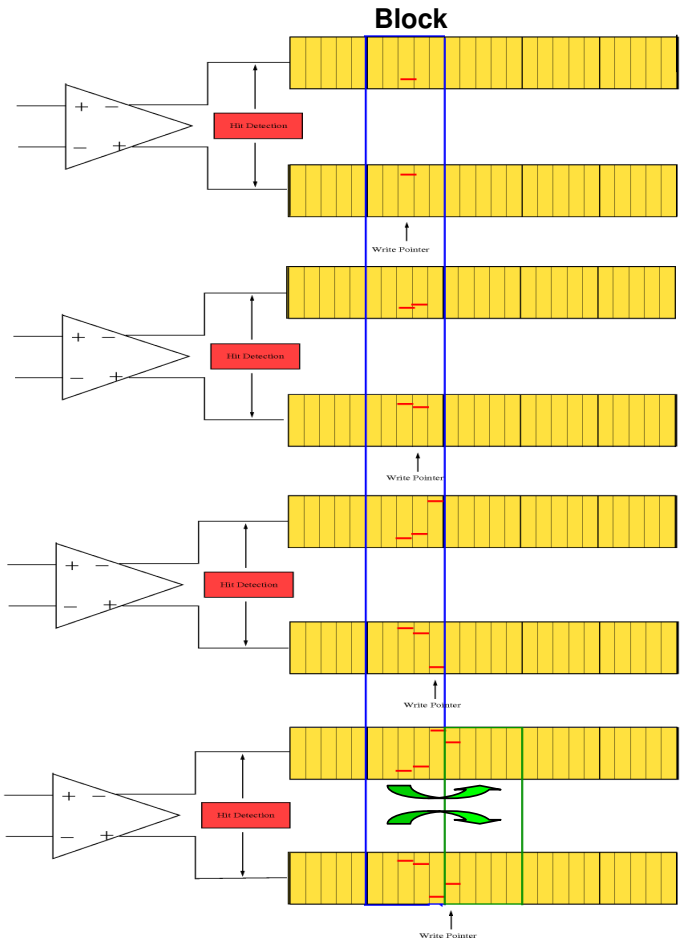
In additions: global clock and sync signal has to be distributed to each board

HitDetection ASIC as an integrated digitiser placed close to the front end on the back plane boards inside the barrel slice

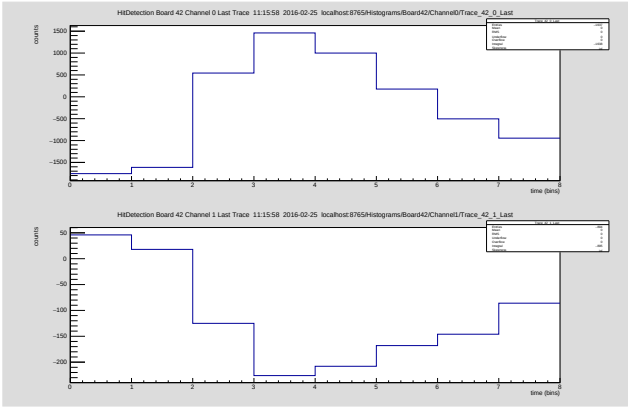
- Less cable cross section
- Digitiser close to front end $\Rightarrow$ less pick up
- Less components
  - $\Rightarrow$ Cheaper
  - $\Rightarrow$ More reliable
- Concept: Self triggered analogue transient recorder
  - Shared ADC for many channels $\Rightarrow$ high power efficiency


Trigger
Column Select
4 Channels
Threshold
Threshold
Threshold
Threshold
Analogue Memory
Row Select
Input Buffer
Integrator
Auto Zero
Analogue Multiplexer
Select
12 Bit Pipeline ADC
Data (12 bit)

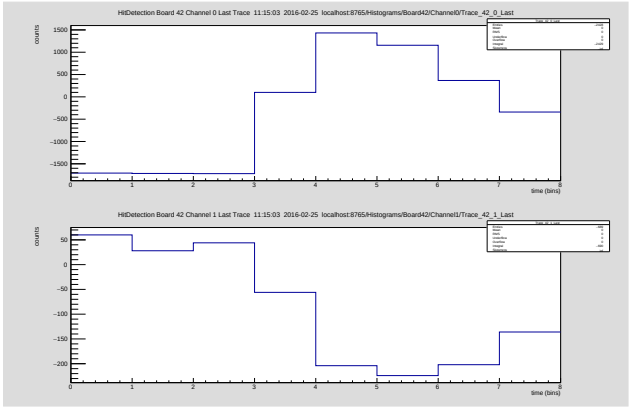

Block
Hit Detection
Write Pointer


Block
Hit Detection
Write Pointer

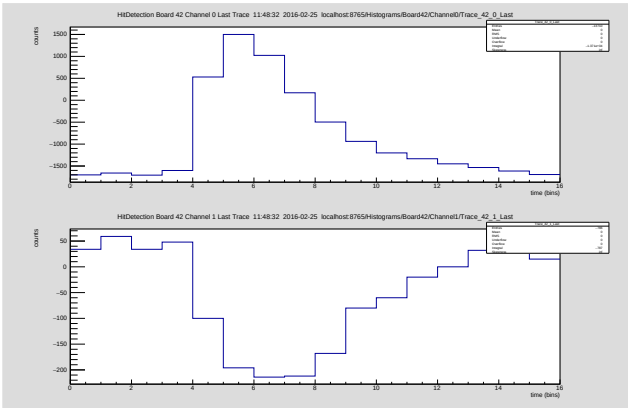
Outline



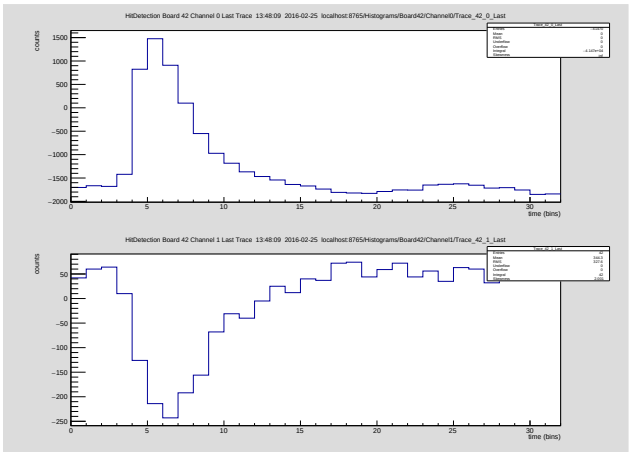
8 sample mode



8 sample mode

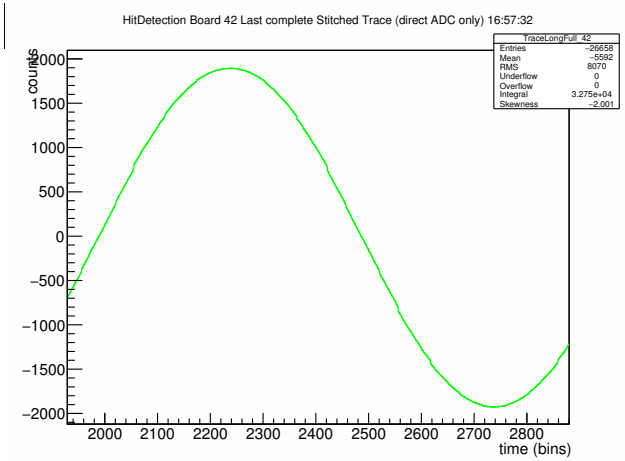


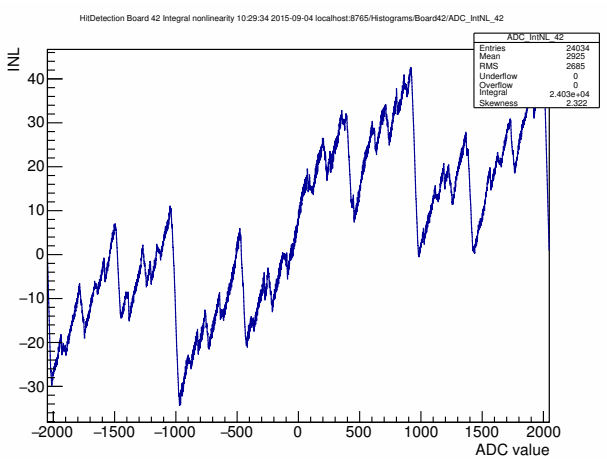
16 sample mode



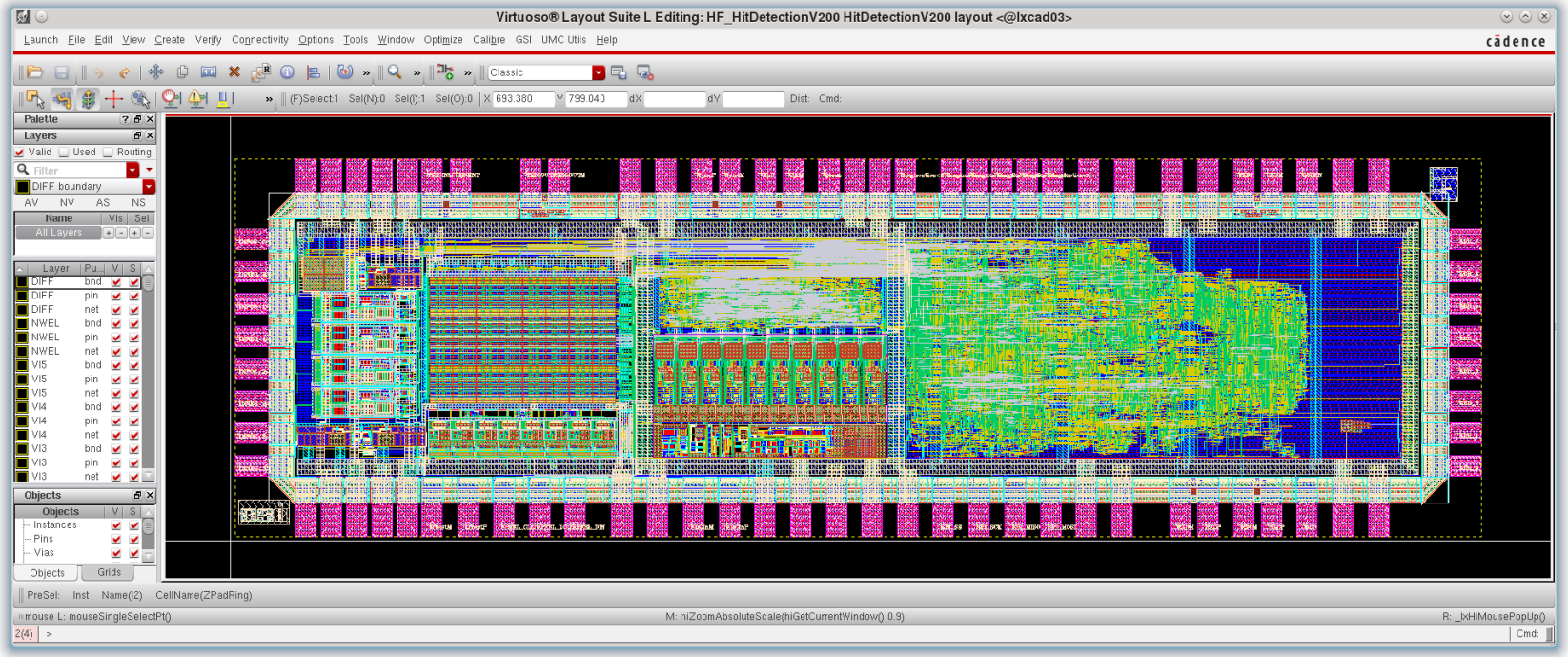
32 sample mode

- HitDetection prototype 1.00 works
- Transients of APFEL pulses shown
- But: ADC has strong non linearities



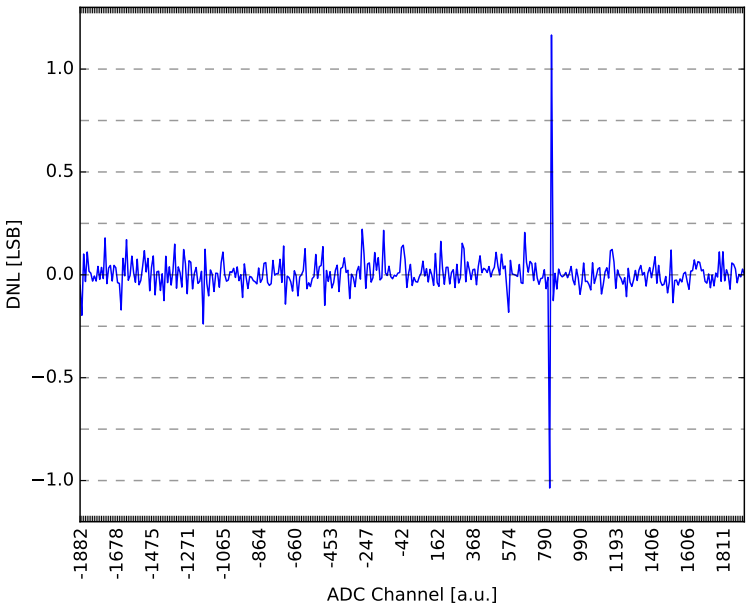


⇒ Real measurements are not possible
⇒ Redesign of the 12 bit pipeline ADC ⇒ digital calibration
⇒ Tape out of HitDetection prototype V 2.00

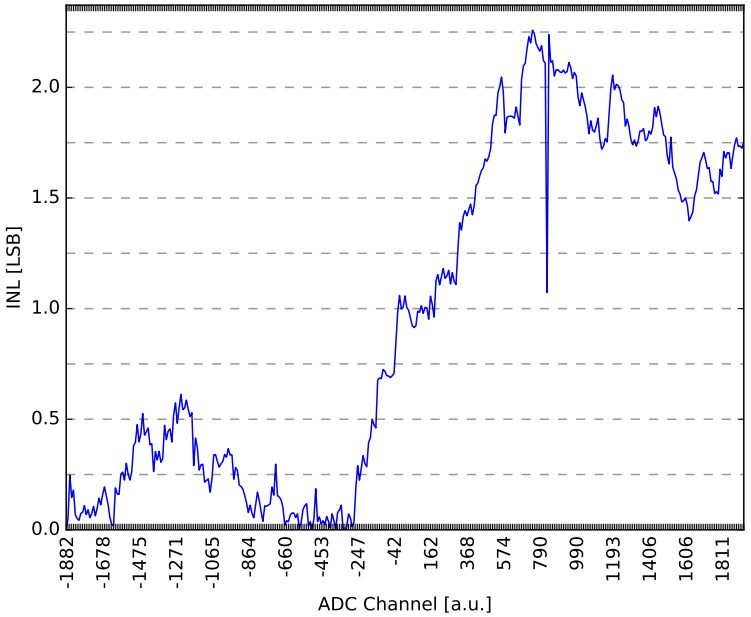


- Prototype with four analogue channels, manufactured in UMC 180 nm CMOS
- Tests and characterisation with strong support from HIM / University of Mainz

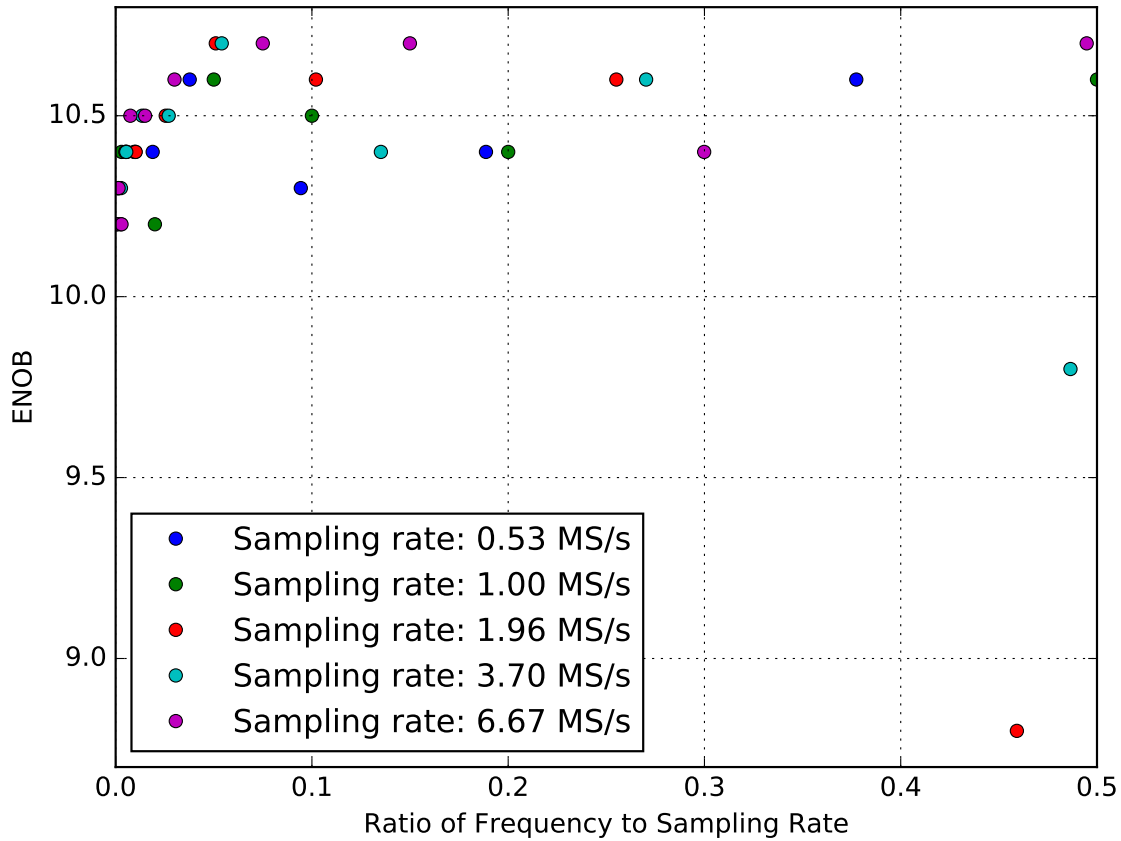
Outline


DNL [LSB]
1.0
0.5
0.0
−0.5
−1.0
-1882
-1678
-1475
-1271
-1065
-864
-660
-453
-247
-42
162
368
574
790
990
1193
1406
1606
1811
ADC Channel [a.u.]

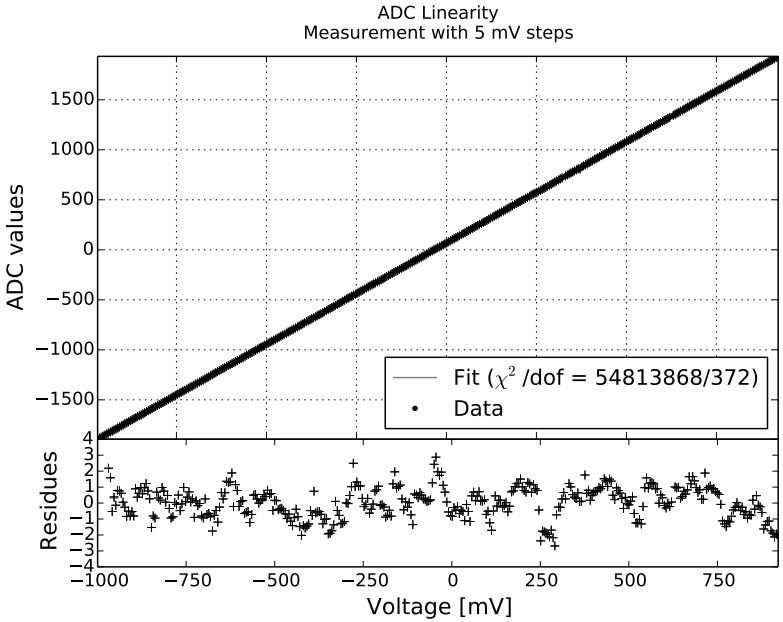
DNL


INL [LSB]
2.0
1.5
1.0
0.5
0.0
-1882
-1678
-1475
-1271
-1065
-864
-660
-453
-247
-42
162
368
574
790
990
1193
1406
1606
1811
ADC Channel [a.u.]

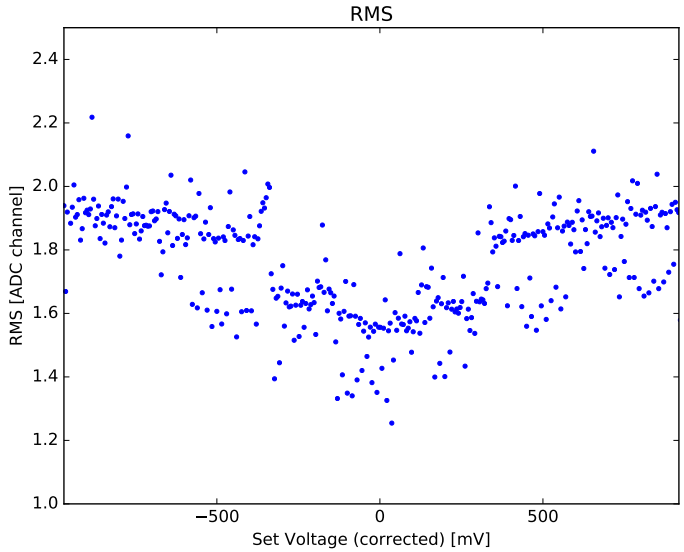
INL



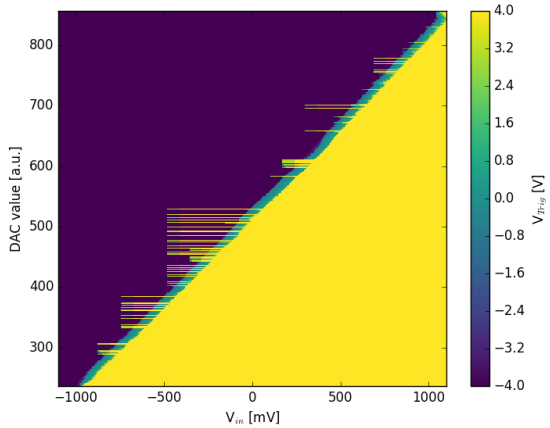
Dynamic range of ADC vs. sampling rate and input frequency



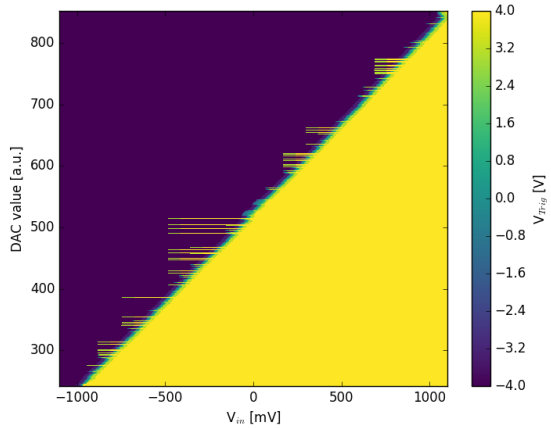
ADC DC scan



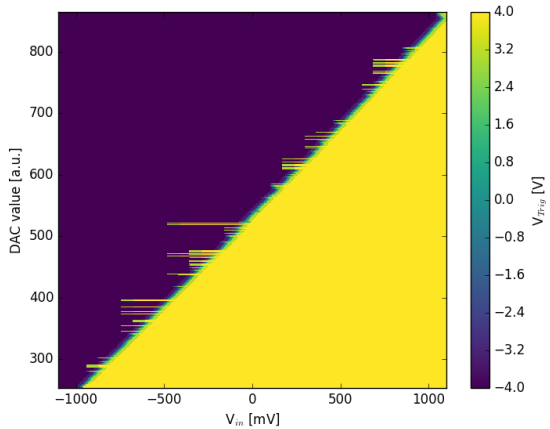
noise vs. input voltage



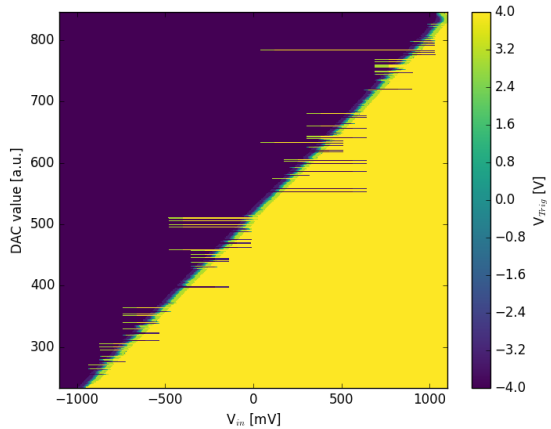
Channel 0



Channel 1



Channel 2



Channel 3

- Corrupted ADC Data observed in self triggered event mode
- Outcome of investigation: During chip synthesis timing model of old ADC was used
  - $\Rightarrow$ Unfortunately HitDetection 2 is not able to digitise and transmit recorded transients
  - $\Rightarrow$ No further measurements with APFEL pulses, detector tests are feasible.
- Measurement for characterisation of analogue memory by analogue test outputs is done, data not yet analysed.

Outline

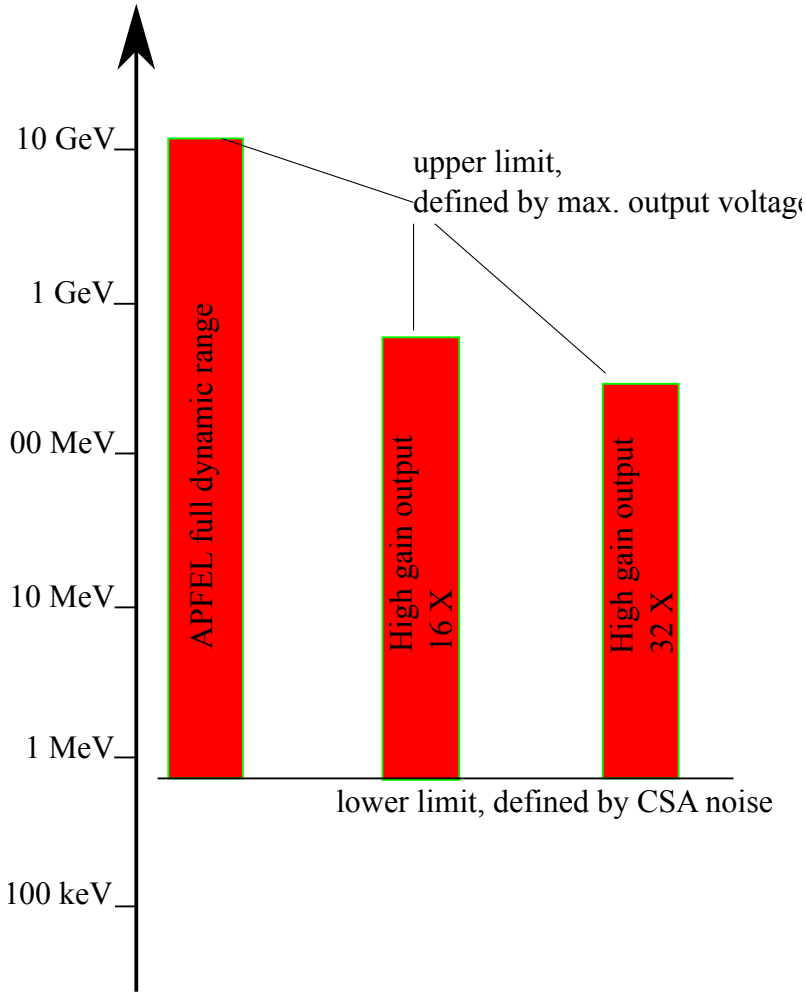
- Simulations for corrected timing model completed
- Building a new Chip with existing synthesis scripts
- Next tape out deadline: July 2018
- Corrected ASIC will be available in autumn 2018
  - Full Analogue memory characterisation
  - Detector tests with detector and APFEL front end
  - HIM evaluates usage of HitDetection prototype for phase 0 experiment in Mainz

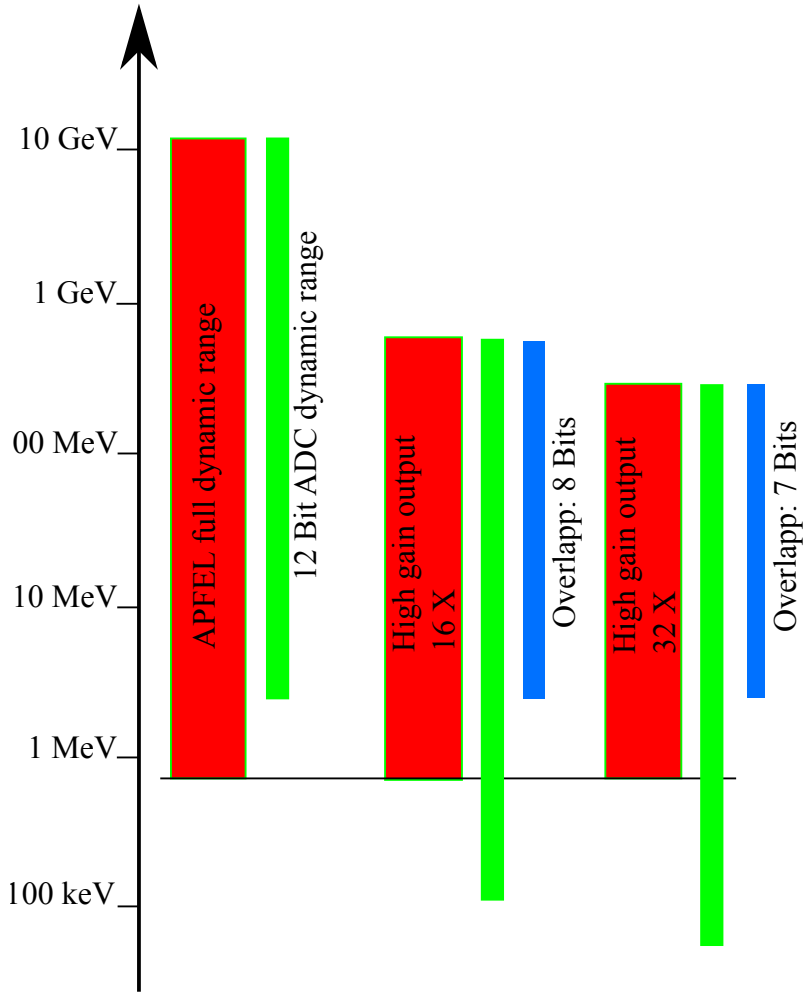
Integration Level

- Two options for placement
  - Warm end of flex PCB
  - Baseboard

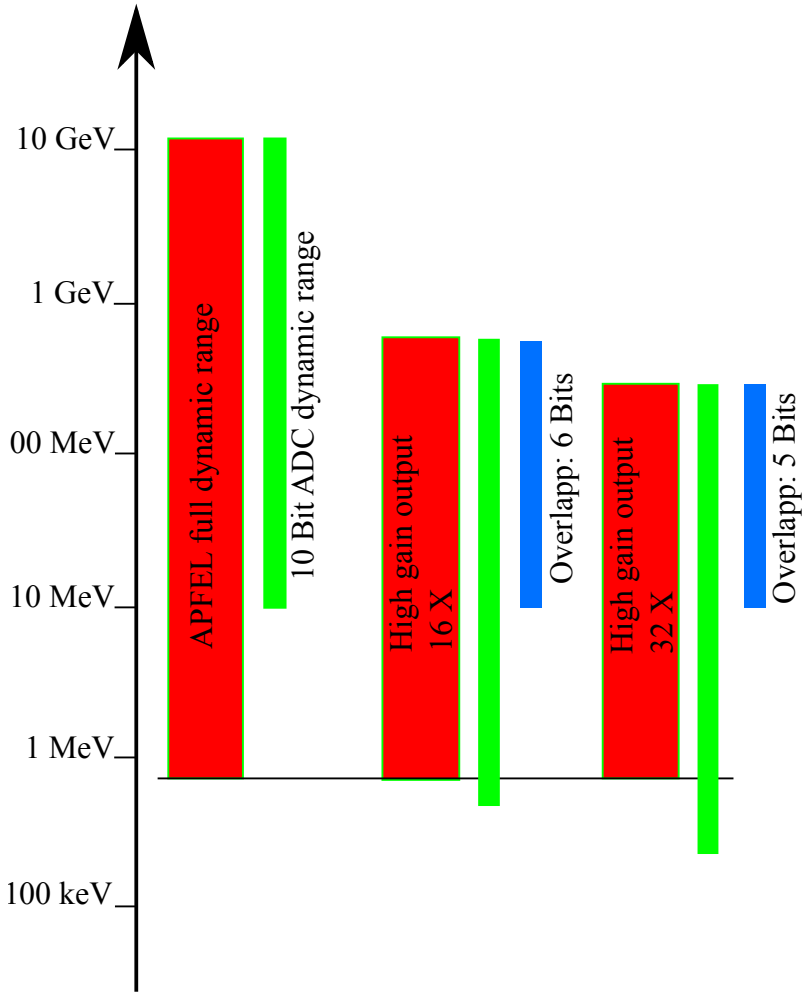
  Base board placement seems to be favoured
- Base board placed HitDetection has to cope with 16 analogue channels

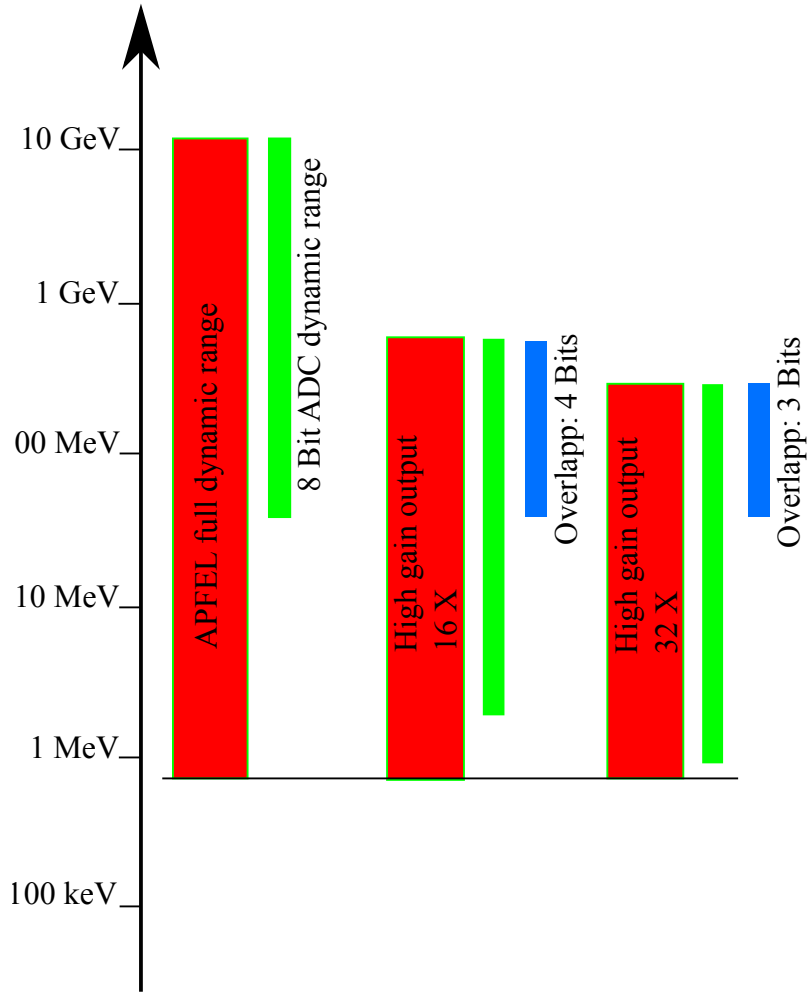
Dynamic Range





Dynamic Range

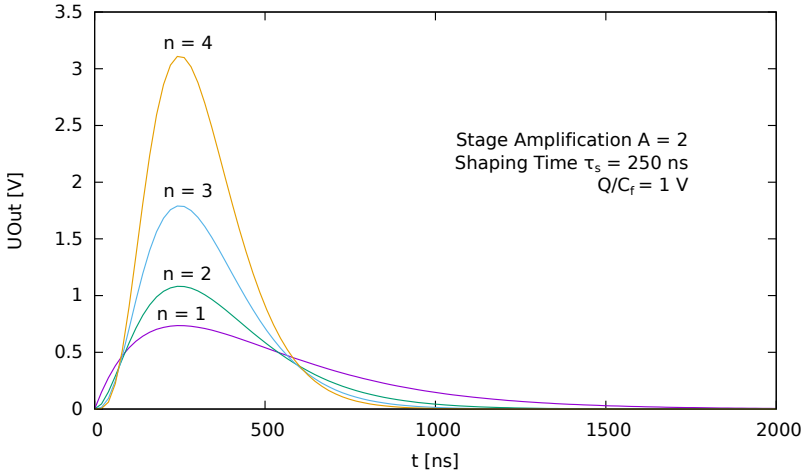




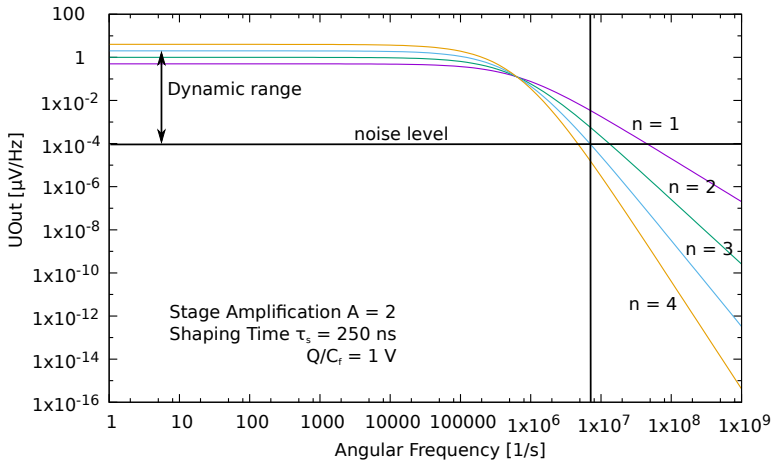
Dynamic Range

	gain X16		gain X32	
ADC dynamics	Covrg.	Overlapp	Covrg.	Overlapp
8 Bit	12 Bit	4 Bit	13 Bit	3 Bit
10 Bit	14 Bit	6 Bit	15 Bit	5 Bit
10.5 Bit	14.5 Bit	6.5 Bit	15.5 Bit	5.5 Bit
12 Bit	16 Bit	8 Bit	17 Bit	7 Bit

Required dynamic range: 13.3 Bits



PASA output signal



PASA output spectrum

- 99.9 % of signal in the spectrum below 3.17 MHz
  ⇒ Minimum sampling frequency: ≈ 7 MS/s
  ⇒ 7 samples to cover full pulse
  ⇒ 8 sample mode would cover full pulse, but no sufficient base line coverage!

Required Number of ADCs per Chip

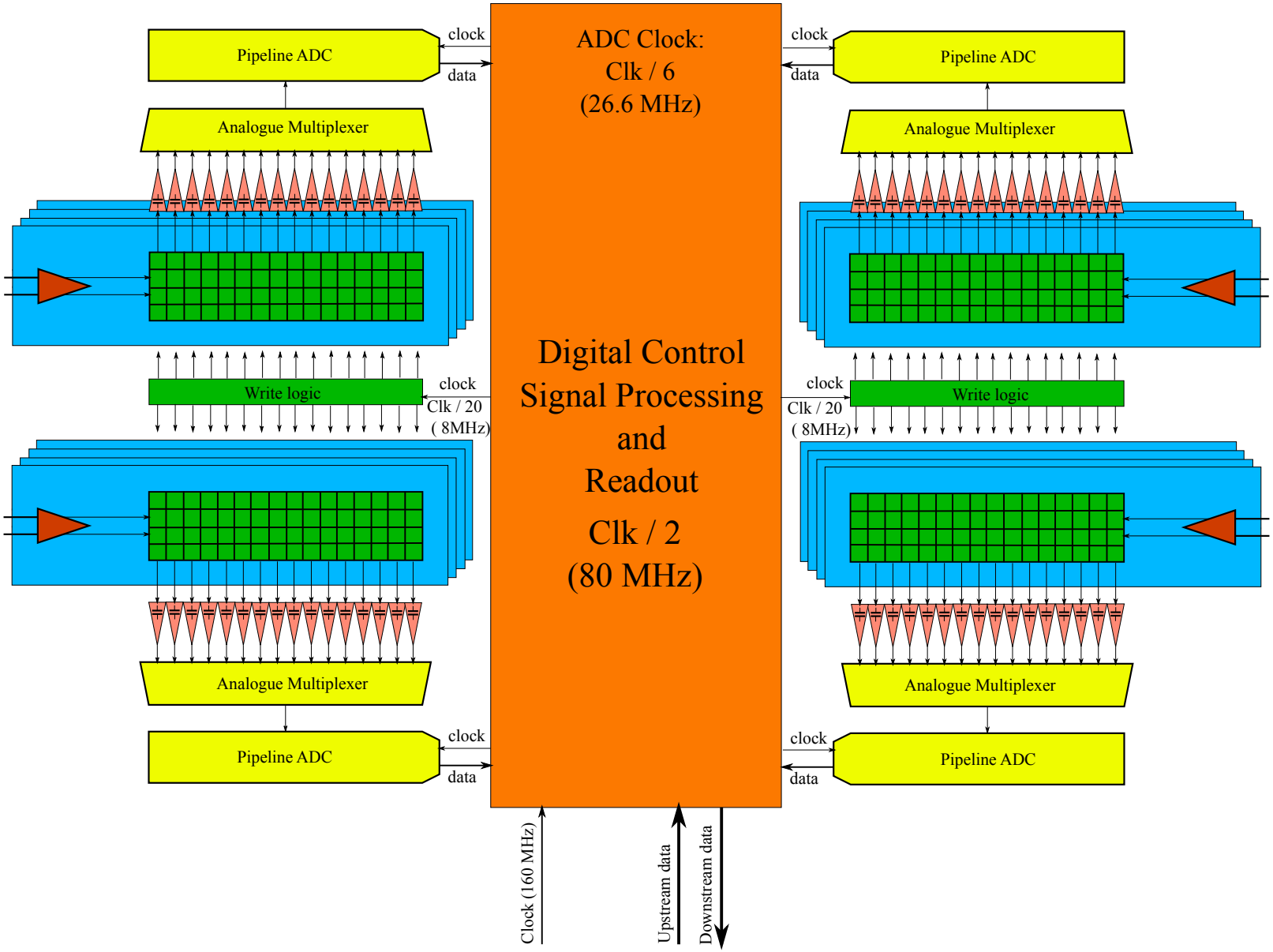
- ADC sampling rate: 33 MS/s
- Number of channels: $n_{ch} = 16$
- Estimated mean hit rate: $f_{hit} = 300$ kHz / channel
- $n_S = 8$ Sample mode
  - $\Rightarrow$ Required sampling rate: $f_{Samp} = n_{ch} \cdot n_S \cdot f_{hit} = 38.4$ MS/s
  - $\Rightarrow$ 2 ADCs / chip
- $n_S = 16$ Sample mode
  - $\Rightarrow$ Required sampling rate: $f_{Samp} = n_{ch} \cdot n_S \cdot f_{hit} = 76.8$ MS/s
  - $\Rightarrow$ 3 / 4 ADCs / chip

Data rate Estimation

- Bits per Event for raw data:

information	8 Sampl. mode		16 Sampl. mode	
channel		4		4
time stamp		12		12
samples	$8 \cdot 12$	96	$16 \cdot 12$	192
		112		208

- For 300 kHz event rate and 16 channels:
  $\Rightarrow$ Data rate: $\approx$ 540 MBit/s resp. 1 GBit/s
- With on-chip feature extraction: data reduction to
  $\approx$ 180 MBit/s


Pipeline ADC
clock
data
Analogue Multiplexer
Write logic
clock
Clk / 20
(8MHz)
ADC Clock:
Clk / 6
(26.6 MHz)
Digital Control
Signal Processing
and
Readout
Clk / 2
(80 MHz)
Clock (160 MHz)
Upstream data
Downstream data

I would like to thank

- Luigi Capozza
- Oliver Noll
- Phillip Grasemann

from Helmholtz institute Mainz / University of Mainz for their strong support during testing and characterisation of HitDetection V2.00

Thank you