Test of the frontend electronics of the CBM Silicon Tracking System

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The Compressed Baryonic Matter (CBM) experiment & the Silicon Tracking System (STS)

The CBM experiment:
- QCD phase-diagram at moderate temperature and high density.
- Au + Au @ 2-11 AGeV (SIS100) at 10^5-10^7 interactions/s.
- Fast self-triggering electronics and time-stamped readout.
- High speed data processing and acquisition system.
- 4D event reconstruction and fast selection algorithms.
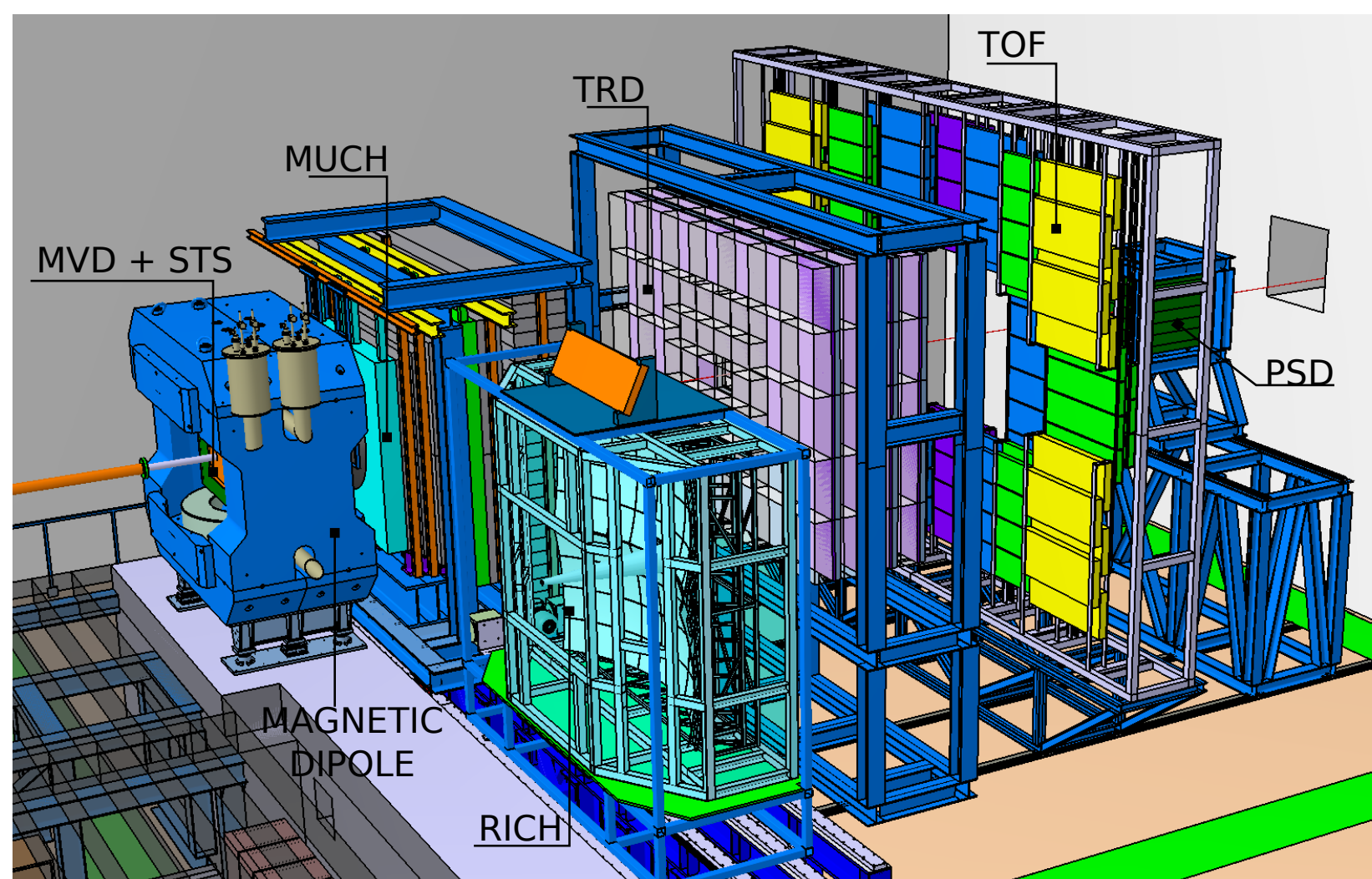
STS requirements:
- High efficiency.
- Tracking up to 1000 charged particles/collision.
- Radiation hardness: 10^{14} 1 MeV n_{eq}/cm^2.
- Low mass: material budget per station in the range $0.3 - 1.5\%$ X_0.

STS features:
- 8 tracking stations inside 1 T field.
- Double-sided Si micro-strip sensors ~ 300 μm thickness and $7.5°$ stereo-angle between front and back side strips.

The STS Readout chain
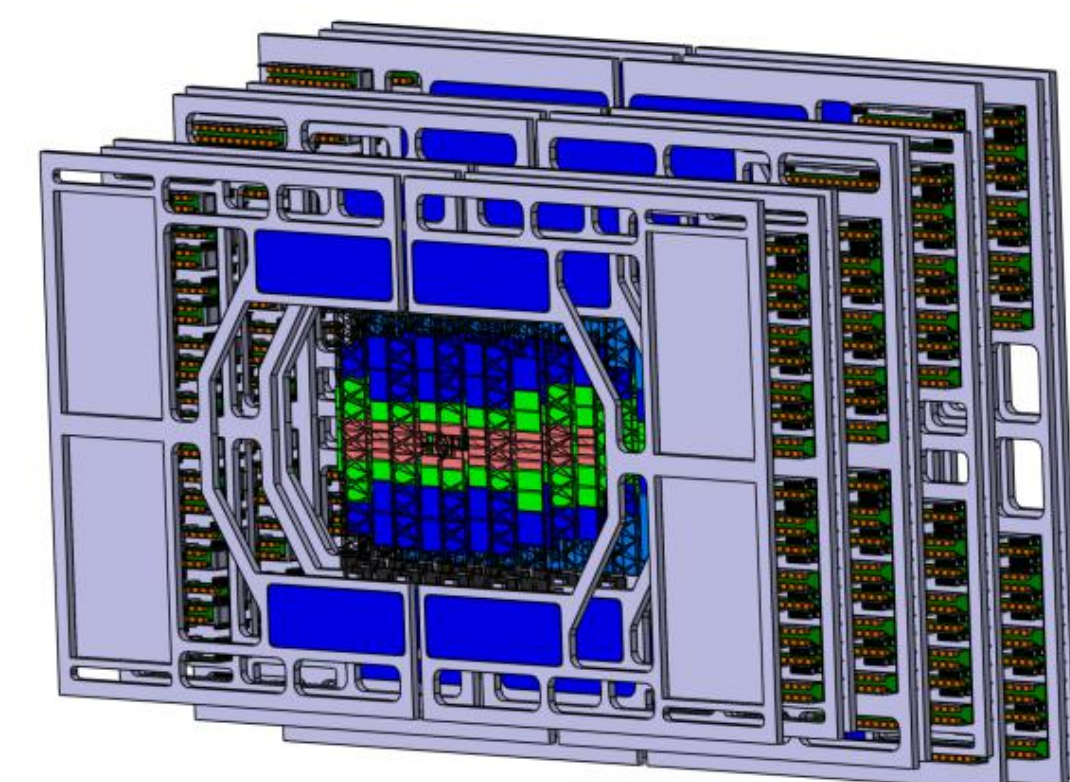
Block diagram of the STS Readout chain
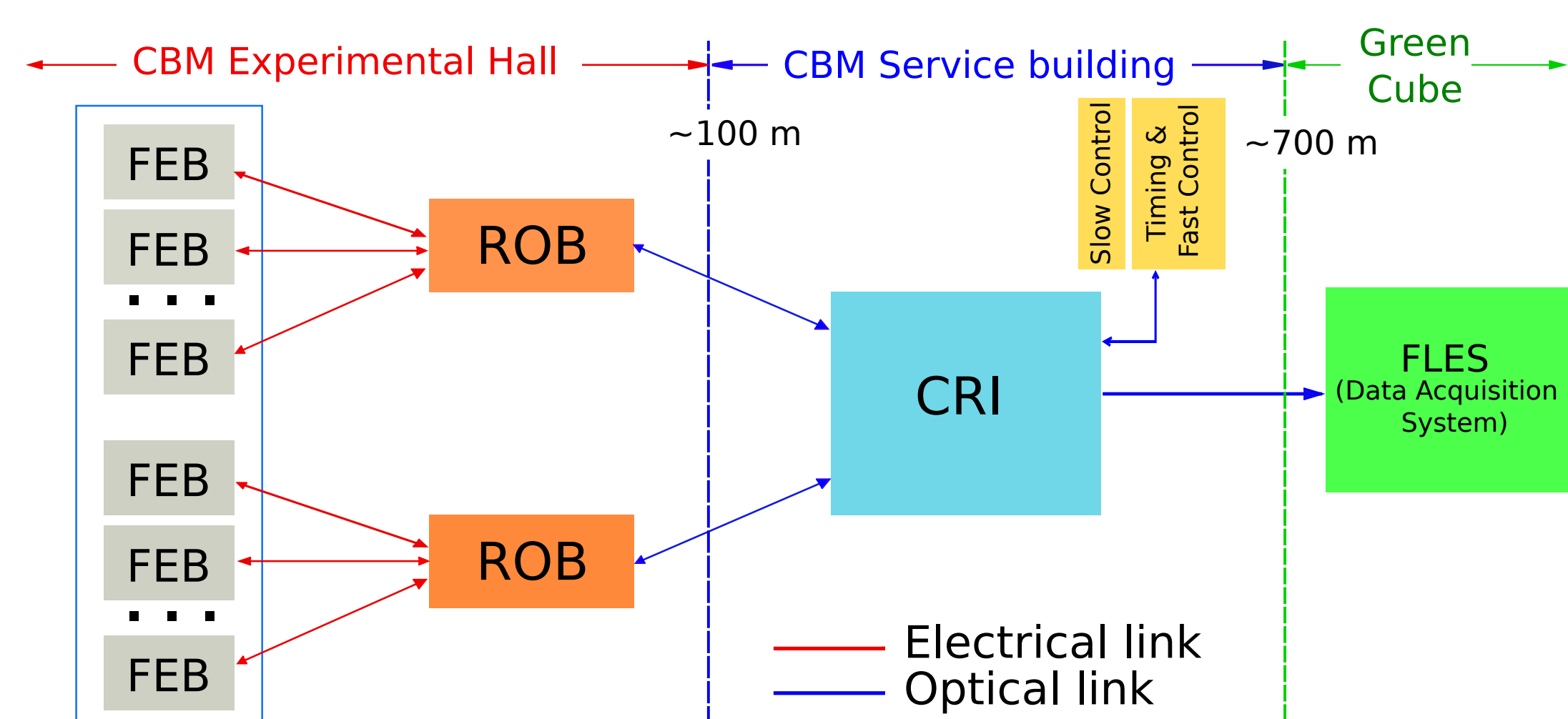
Front End Board (FEB)
- Part of a functional module, where 2 FEB with custom designed ASIC are connected via microcables to a Si sensor.
- Every FEB contains 8 STS-XYTER ASICs for reading out 1024 channels.
- Provides digitized hits.
- Located close to the Si sensors.

Read out Board (ROB)
- Data aggregation from several ASICs.
- Optical readout interface.
- Control and clock distribution.
- Based on CERN GBTx and Versatile Link components.
- Located inside STS box.
 - → Limited space.
  - → Radiation hardness.

Common Readout Interface (CRI)

CBM DAQ layer with common hardware platform.
- FPGA based.
- Timing and control interfaces.
- Data preprocessing.

First Level Event Selection (FLES)
- Time slice building & full event reconstruction.
- Online event selection.

The STS-XYTERv2 test setup at GSI

**STS-XYTER** → **STS** + **X,Y** coordinates + **T**ime and **E**nergy **R**esolution
Low power, self-triggering ASIC dedicated for reading out the double-sided Si sensors.

STS-XYTER functional blocks.
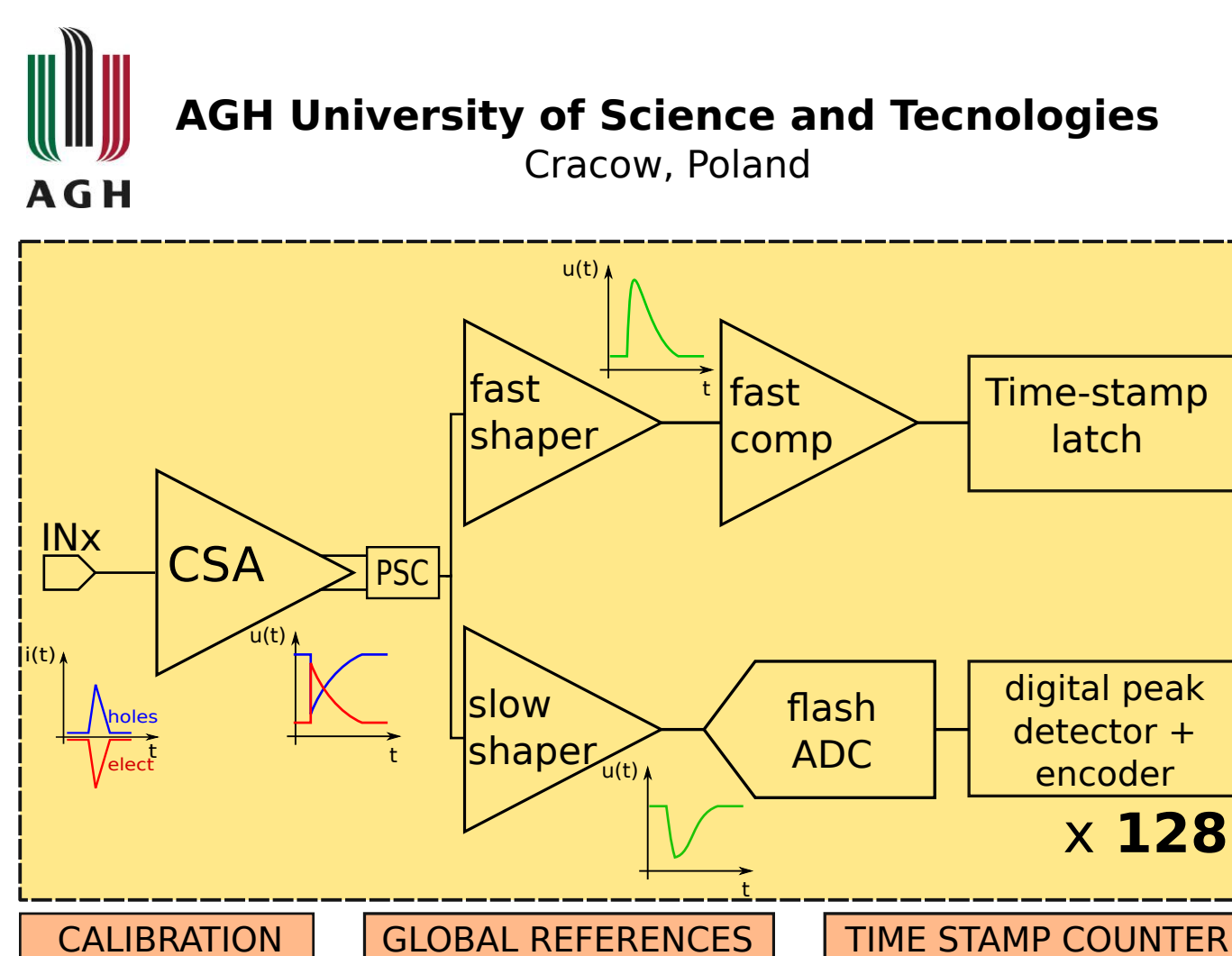
STS-XYTER features:
- 128 readout channels + 2 test channels.
- Time resolution: ~ 5 ns.
- 14 bit time stamp.
- 5 bit flash ADC/channel.
- 15 fC dynamic range.
- Radiation hard layout.
- Digital backend compatible with the CERN GBTx data concentrator.

Prototype STS-XYTERv2 FEB controlled via dedicated protocol backend in Kintex7-FPGA board. Flexible and modular platform for ASIC and sensor testing, software and firmware development.
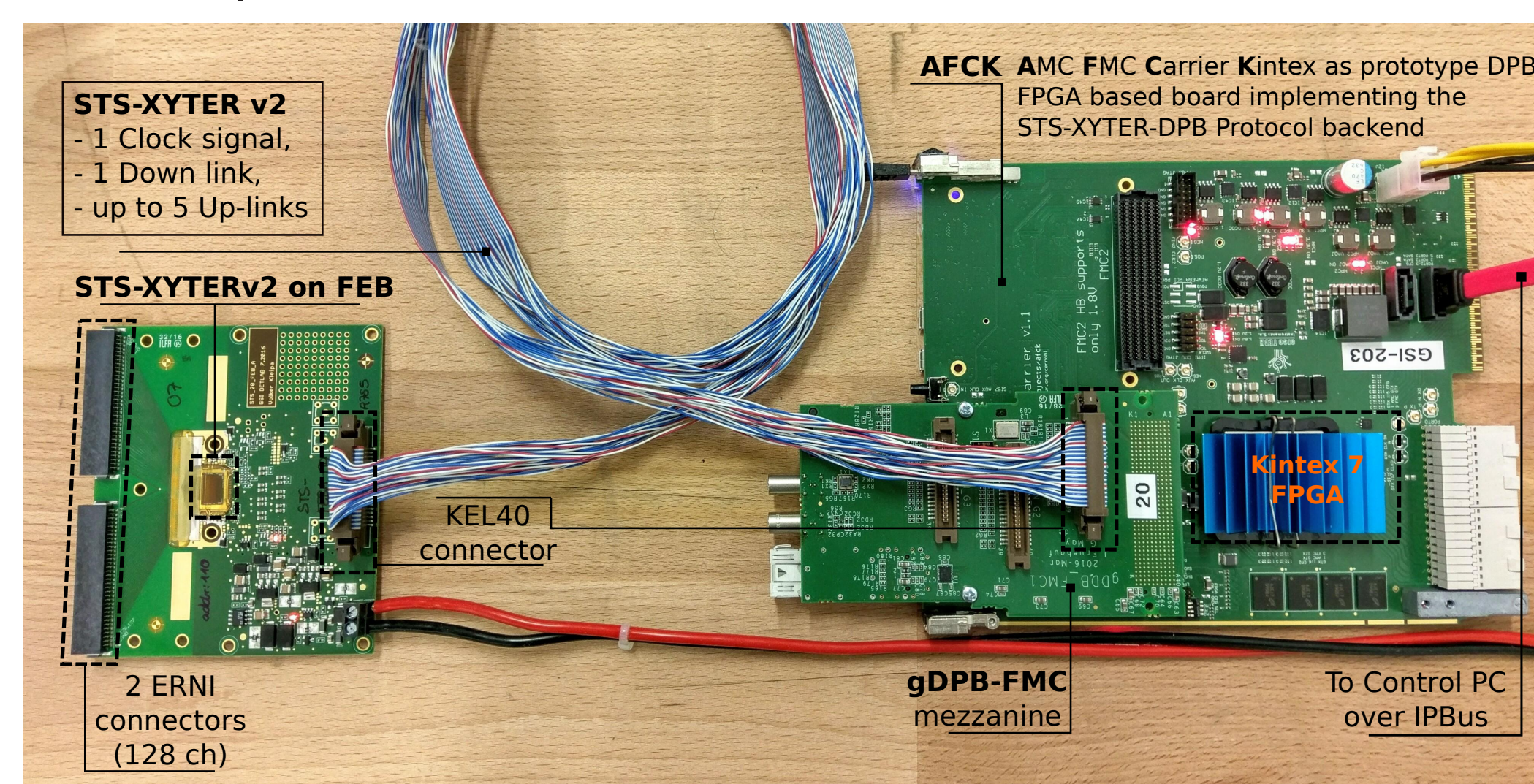

ADC tests

Calibration:
Development and test procedures to evaluate and calibrate in-channel ADCs.

ADCs linearity for 128 channels.

Features:
- Internal pulse generator (range up to 15 fC)
- Global registers sets ADCs range.
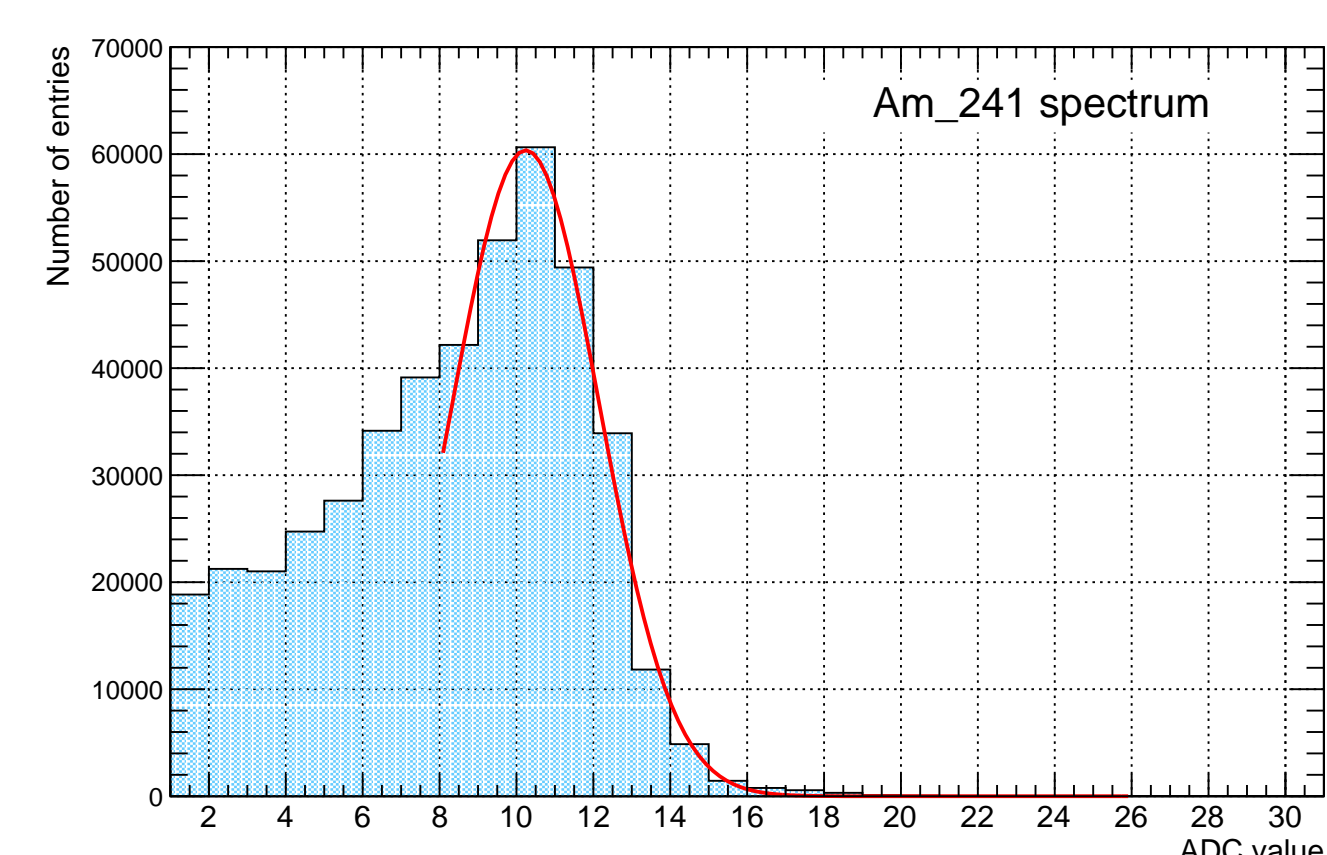- Every ADC has 31 discriminators with adjustable individual threshold (8 bit).

Table 1: Deviation across discriminators in all channels.

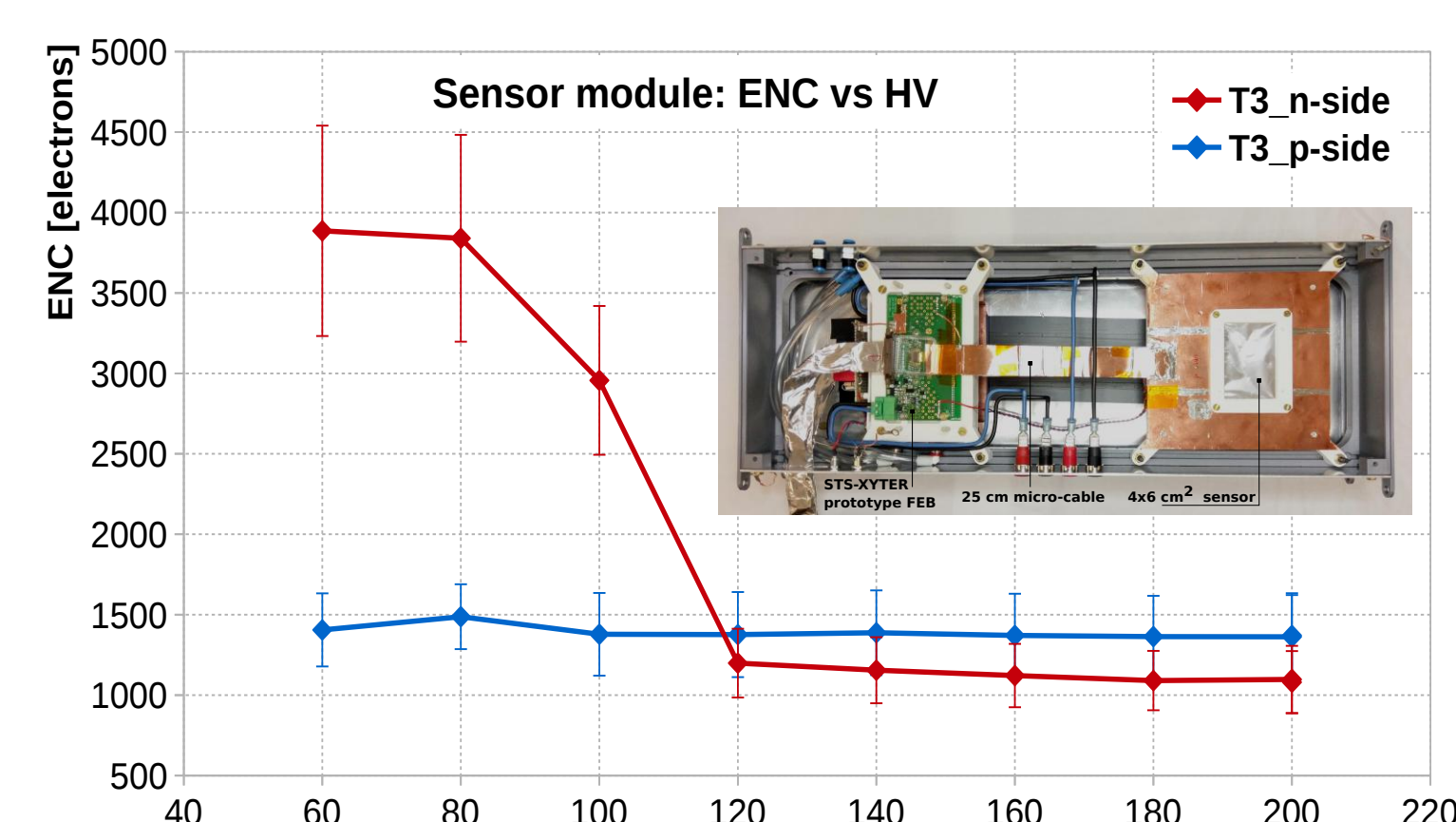|	Bef[fC]	Aft[fC]
holes	0.08	0.02
elect	0.09	0.02
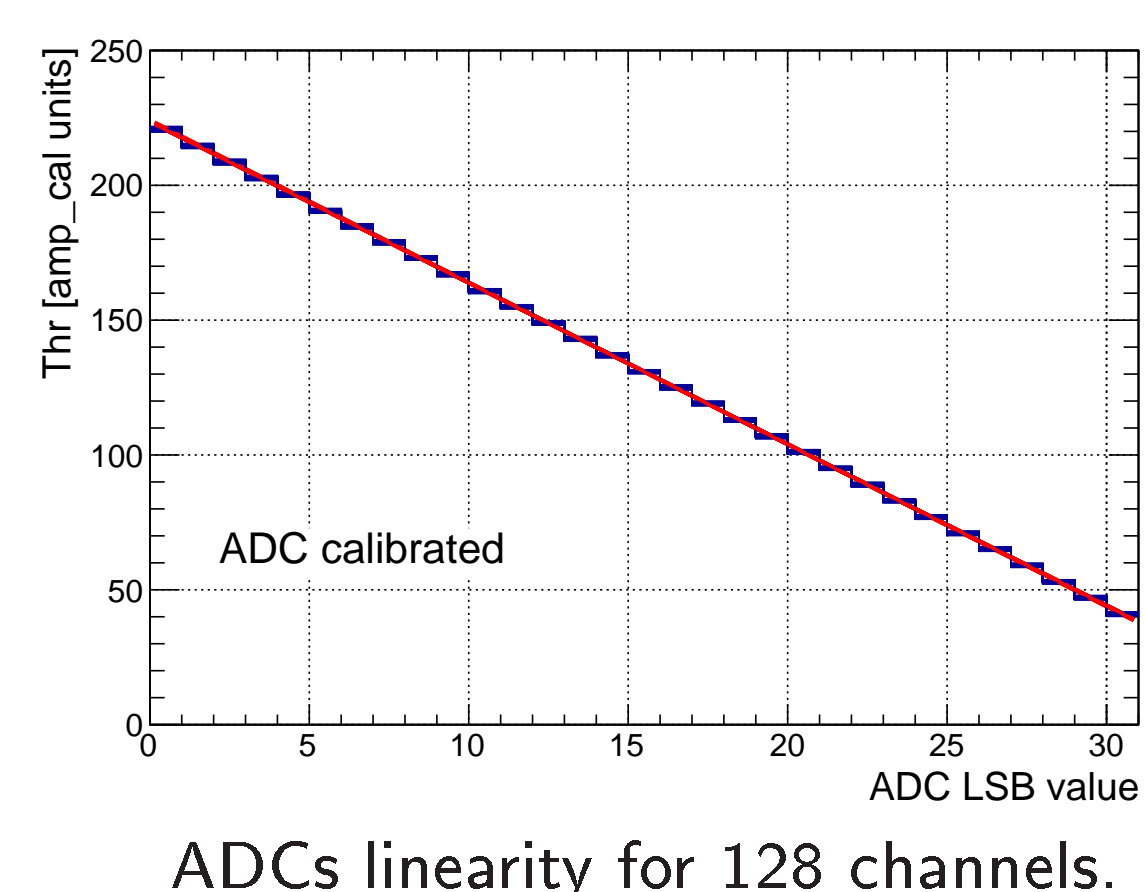
Sensor readout & Equivalent Noise Charge (ENC):

Example of a signal from ^{241}Am source, readout with a 4×6 cm^2 sensor and the STS-XYTERv2 ASIC.
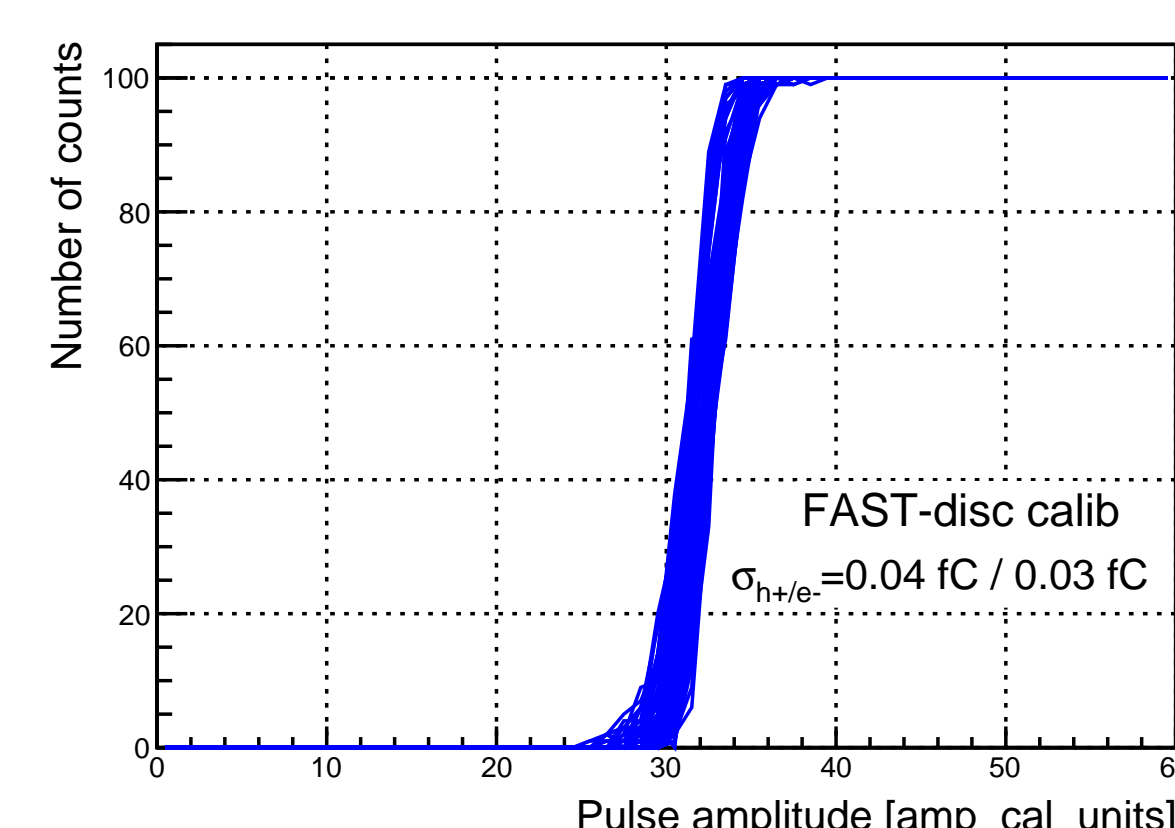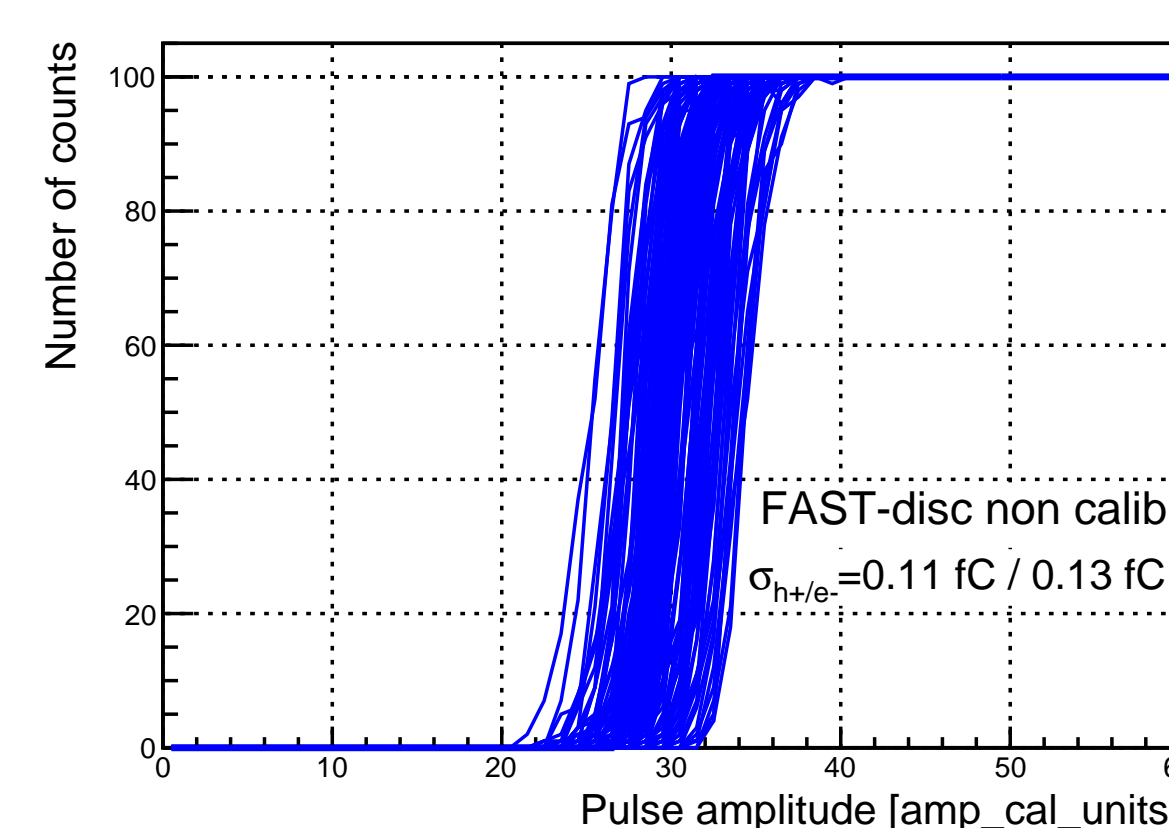
Noise as function of the detector HV measured in a module with 4×6 cm^2 sensor, connected via 25 cm microcable to the STS-XYTERv2.


FAST discriminator tests

Calibration:
The calibration procedure is similar to the one implemented for the ADCs. Every channel possesses a FAST discriminator with adjustable individual threshold (6 bit).

FAST disc. S-curves for 128 channels before and after calibration.

Time-walk and ENC vs load capacitance:

Measured FAST discriminator time walk as function of the signal amplitude. Reference signals set to 100 mV $\sim$ 10 fC with 1 kHz frequency.
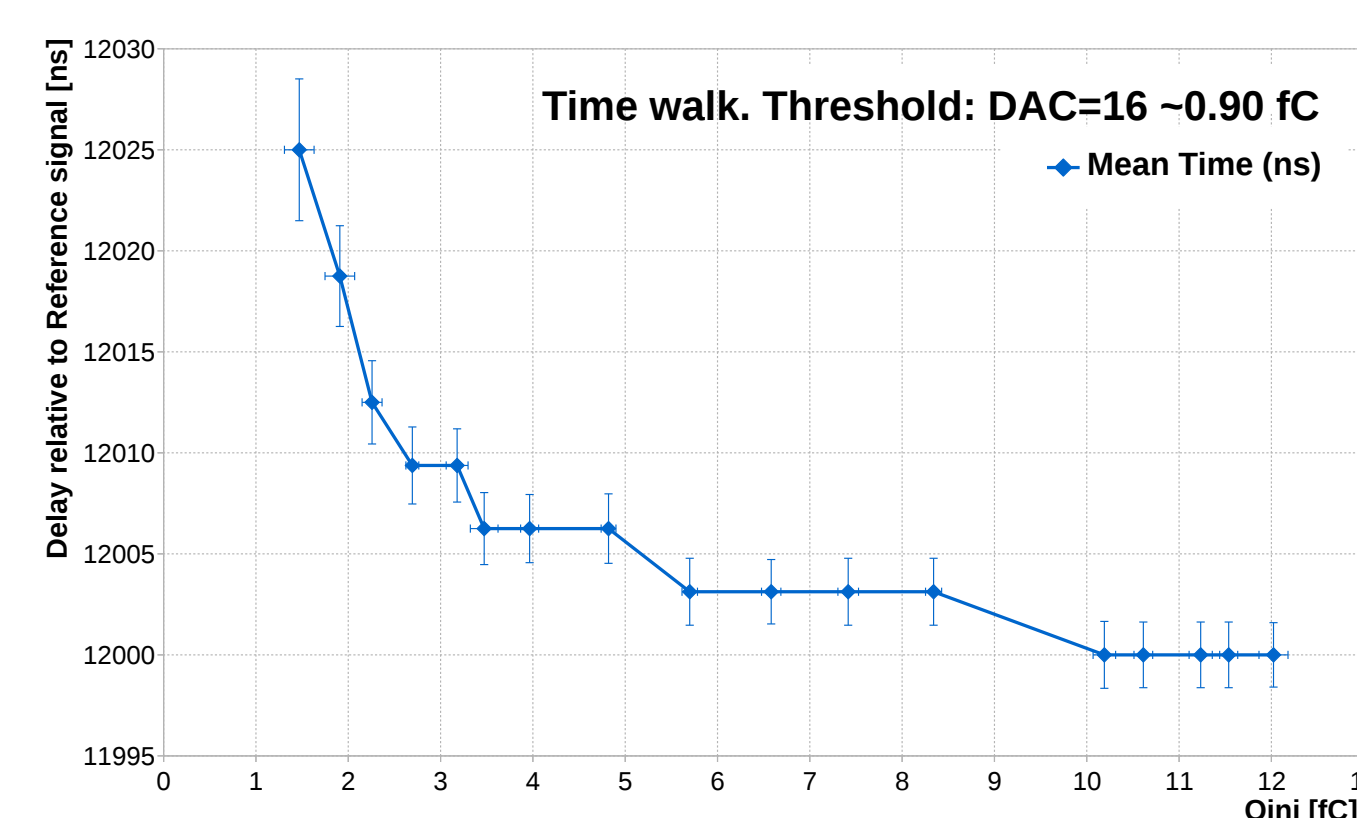
Using a phantom board, where a set of low leakage capacitors were placed, the contribution to the noise was estimated for different load capacitances.