ADC based DAQ for PANDA STT, technical report

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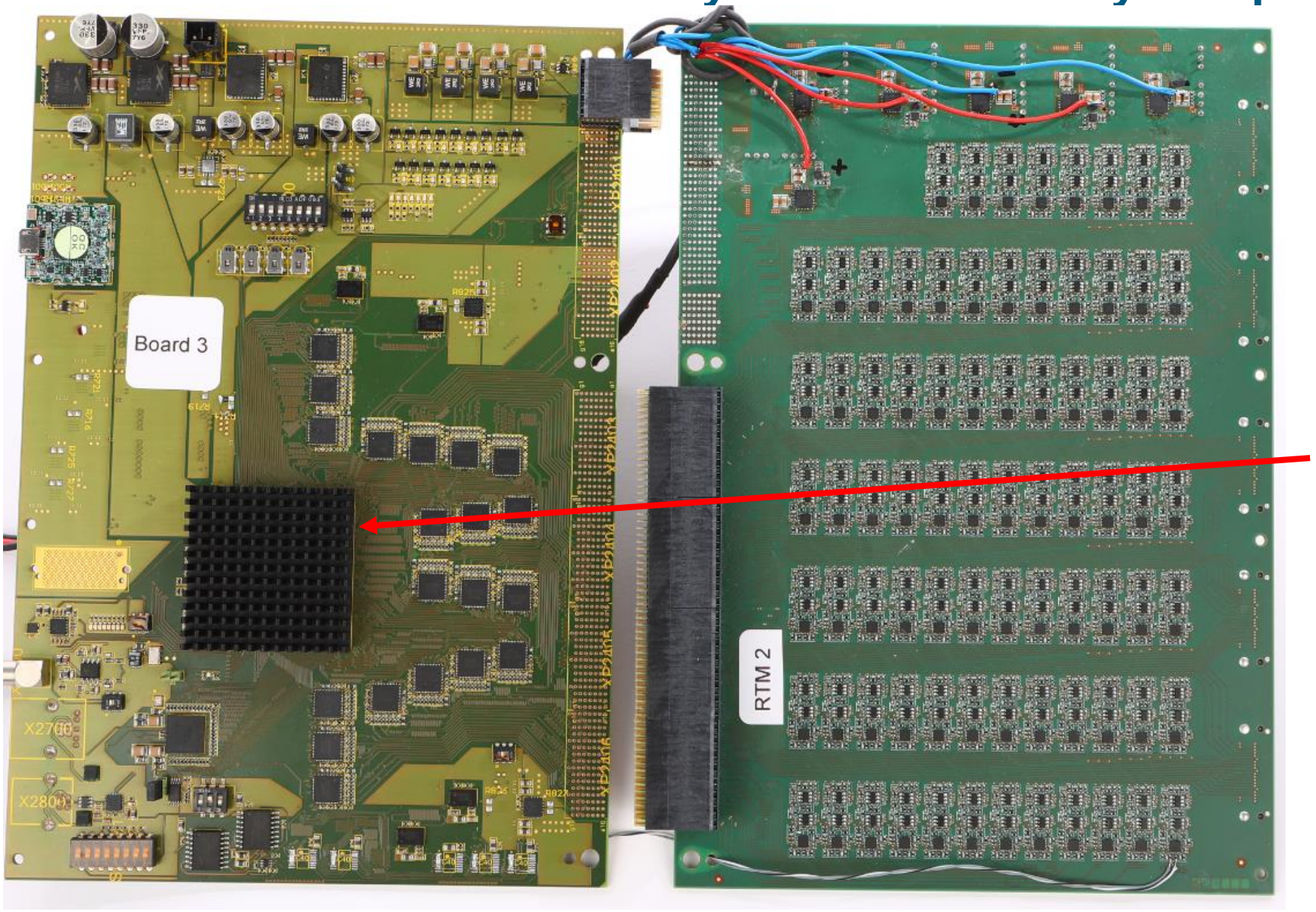
Boards overview.

Motivation: processing of all 160 Channels as single one.

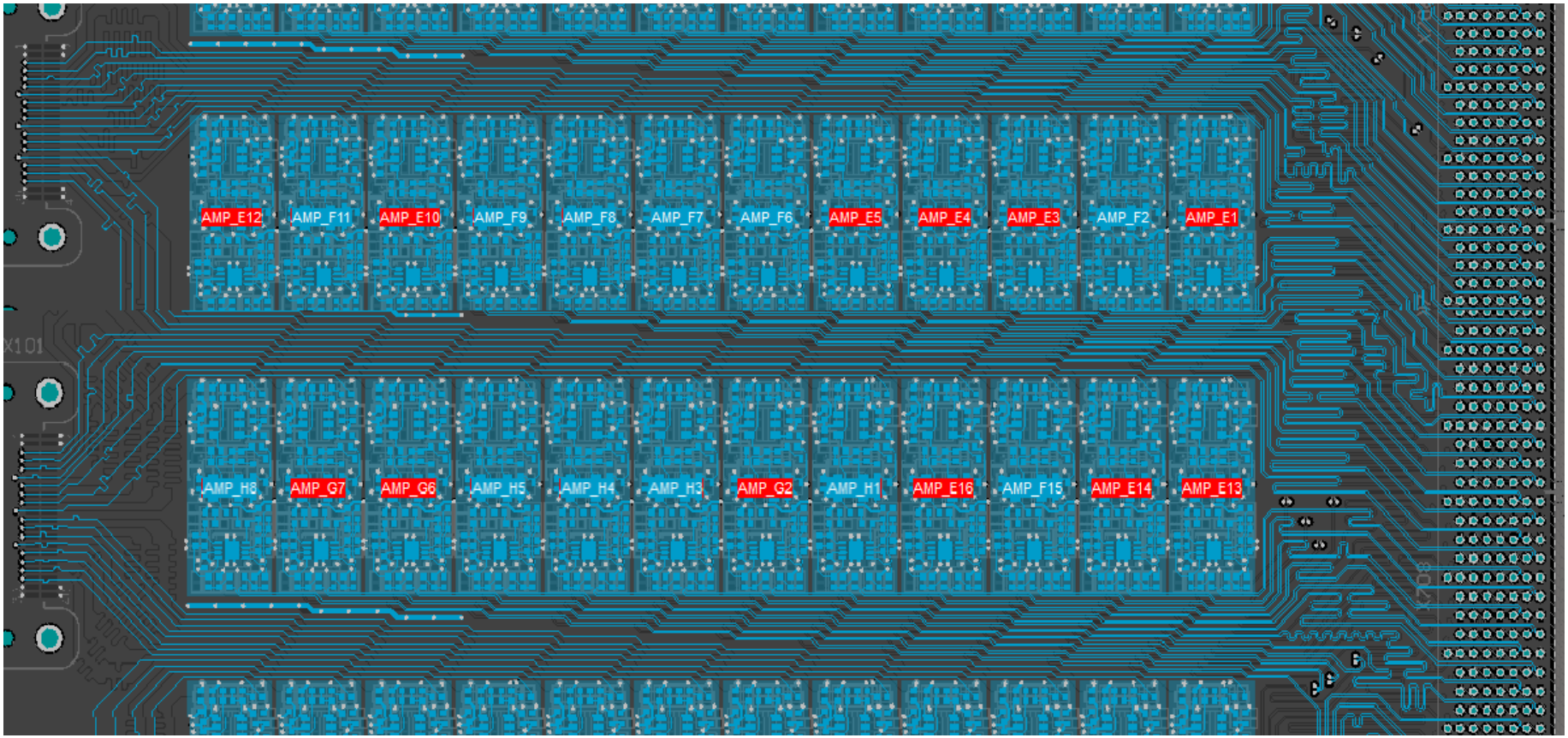
This instrument do not need any calibration/ delay setup.



A fully synchronous design, proposes 3 aspects:

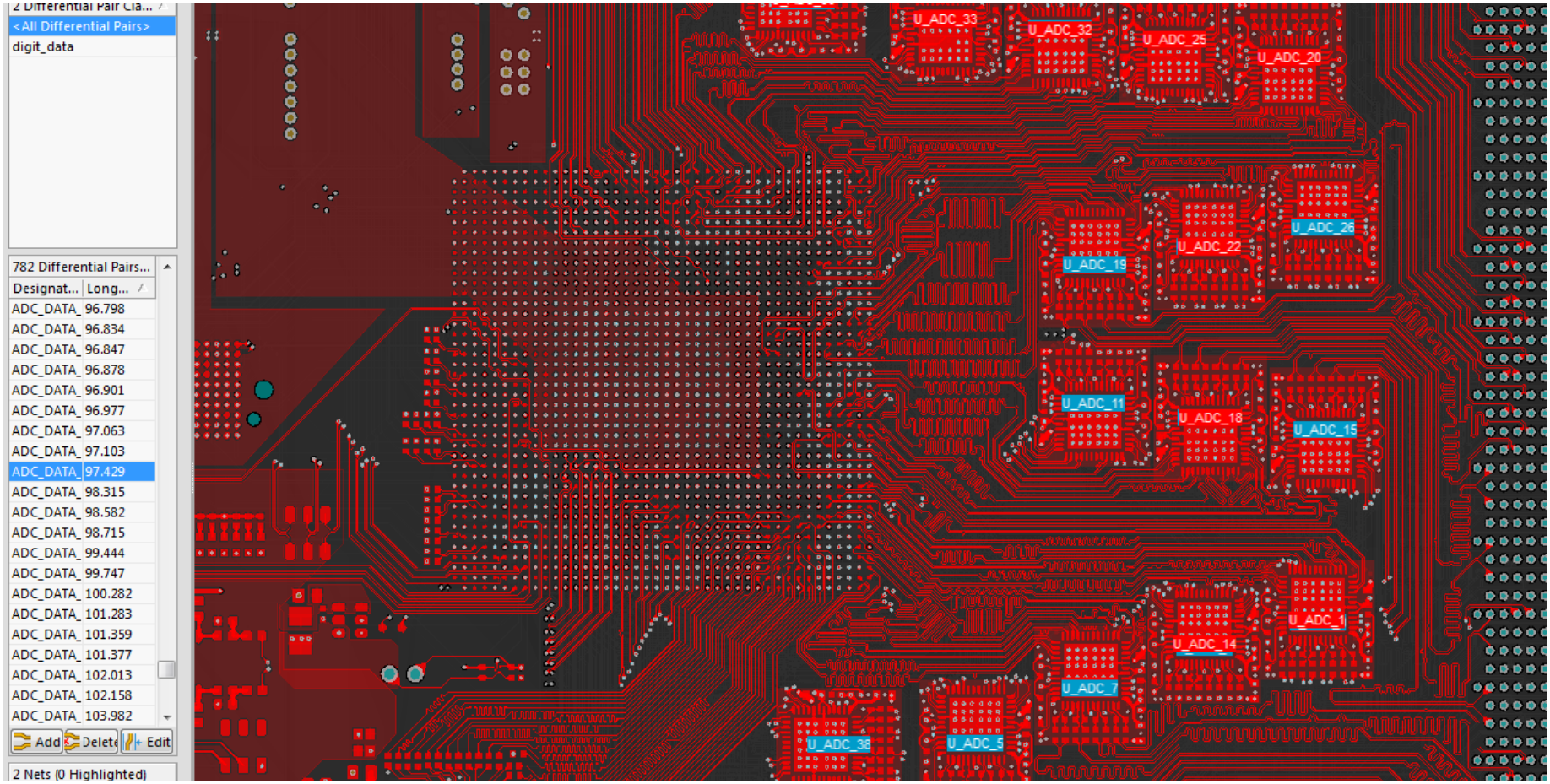
1. **Equal data propagation delay in analog path;**
2. **Synchronous data capture on FPGA;**
3. **Minimal sampling clock skew (~10 ps)**

1. Length matching on RTM, tolerance of 0.1 mm



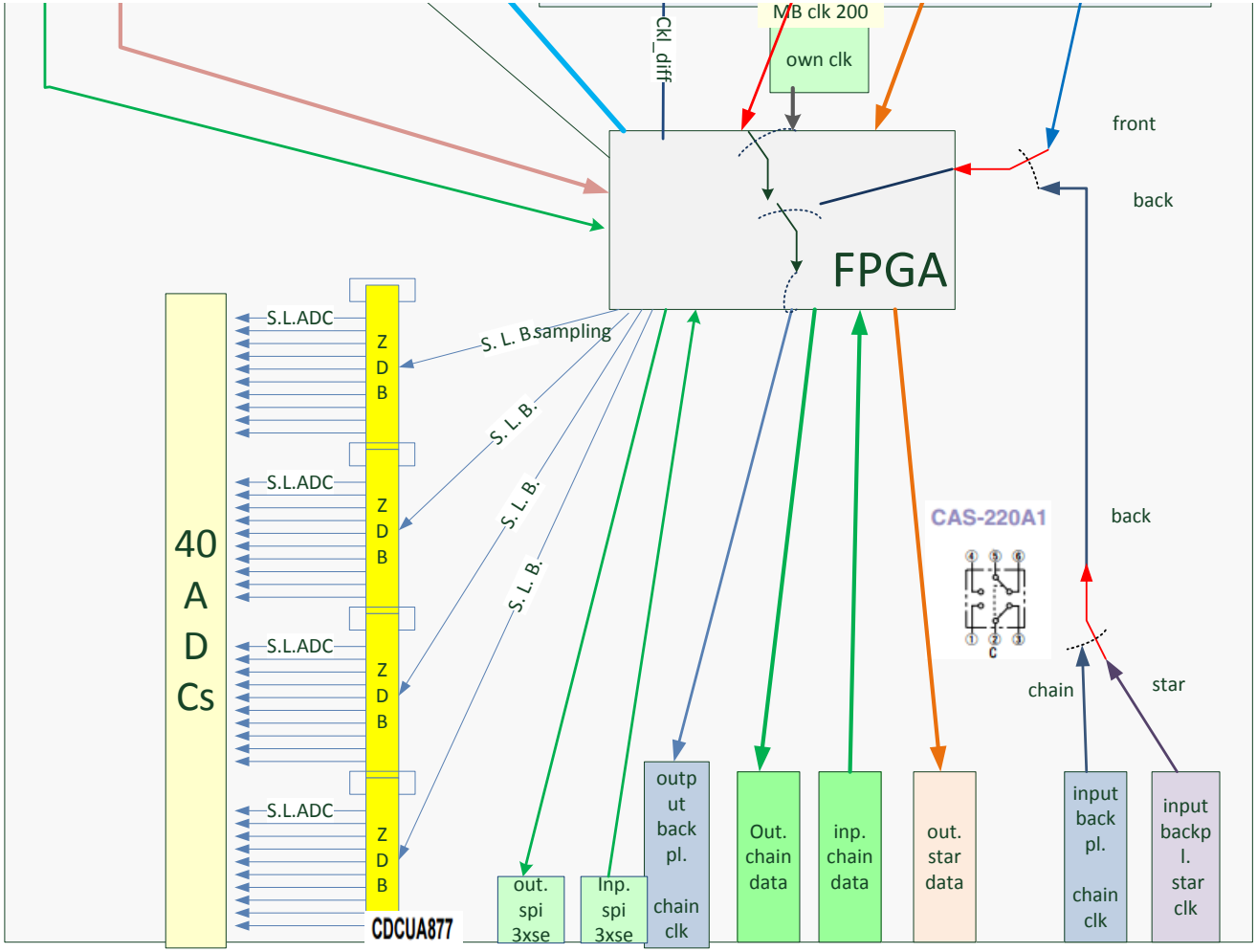
All channels on boards have the same signal propagation delay: no calibration for boards itself is needed.

2. Length matching FB: digital lines length matching of 10 mm, including on FPGA signal propagation (in FPGA package deskew)



All digital 1 GHz lines matched provided propagation difference only +45 ps,
On FPGA signal capture do not require separate delay setup for each channel.

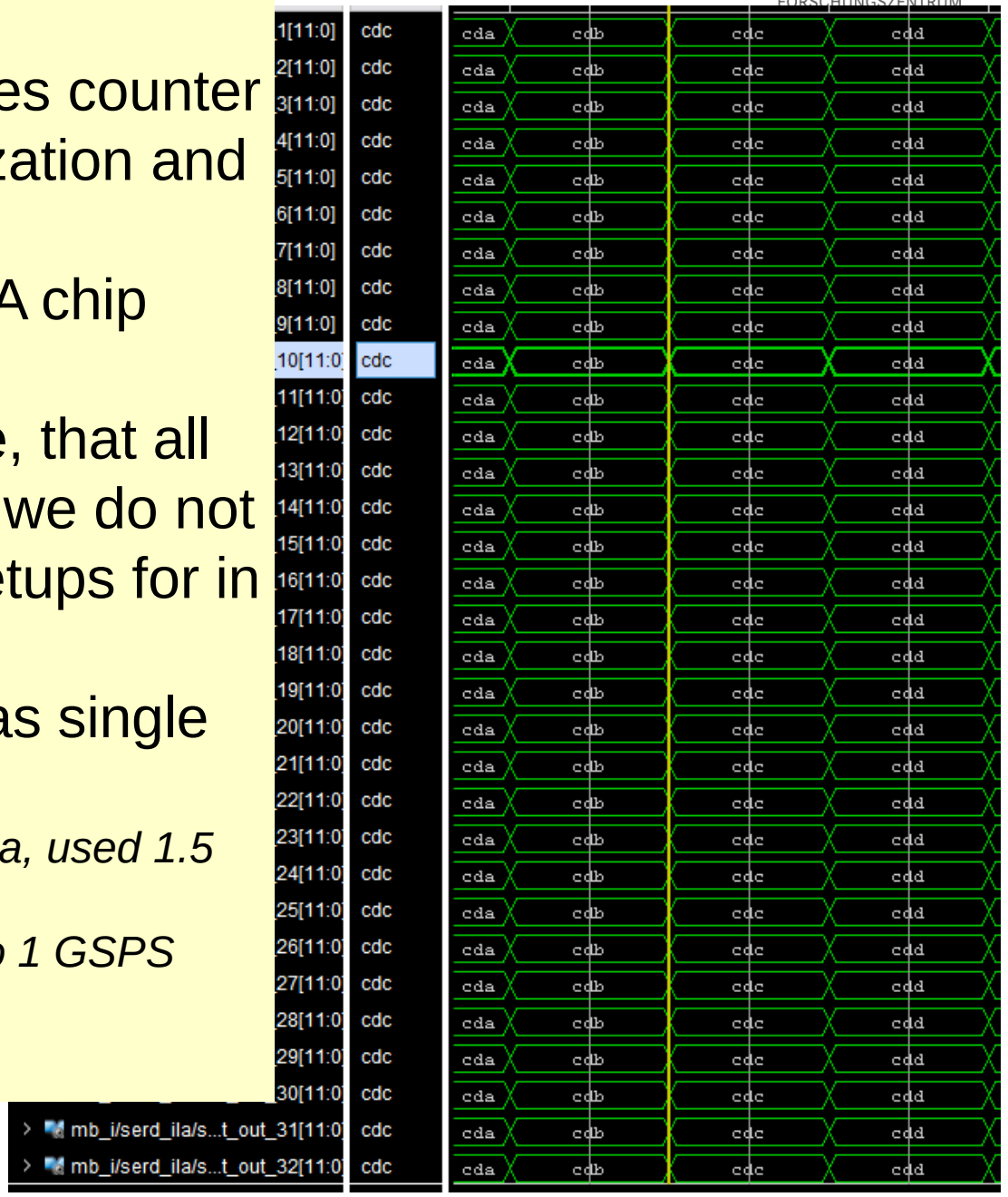
3. ADCs Clock distribution using Zero Delay clock Buffers and length matched design (incl. package deskew) provides sampling clock skew < 15-20 ps) for all 160 Sampling channels.



Test of front board:

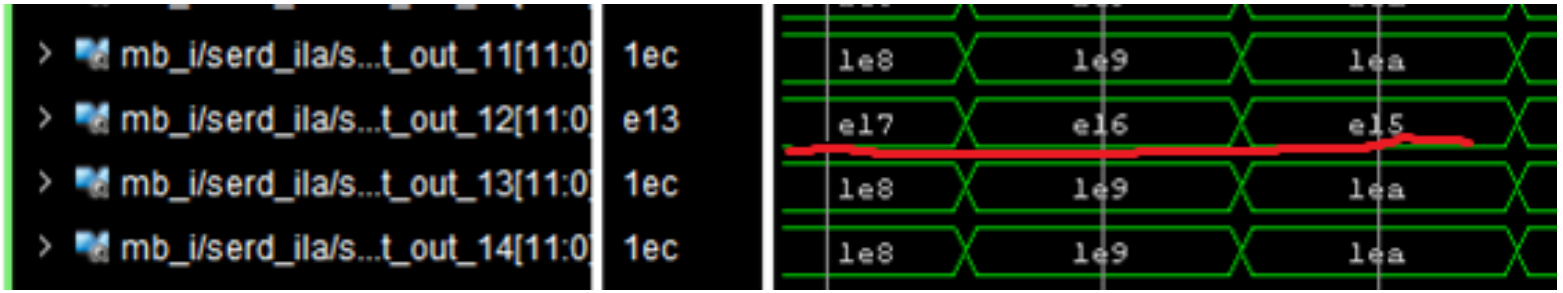
ADC -HMCAD1520 provides counter muster for easy synchronization and test,
Signals got using on FPGA chip scope replays this muster
We could immediately see, that all channels are running and we do not need perform 160 delay setups for in FPGA capture,
all channels are captured as single one.

- *adjustable LVDS current 0.5-7 ma, used 1.5 ma.*
- *sampling rates of 80 MSPS up to 1 GSPS*

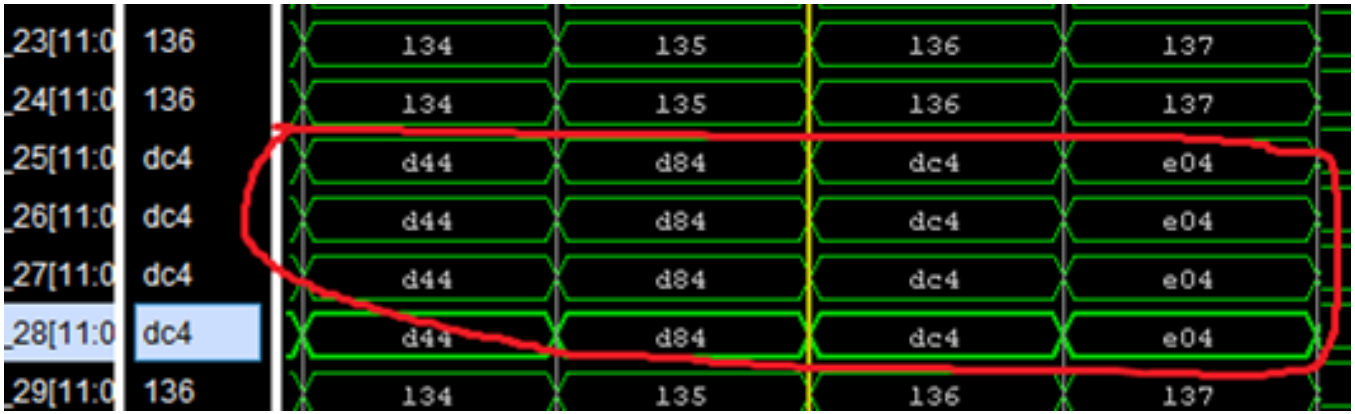


Detected errors:

1. in 2 channels p and n lines exchange

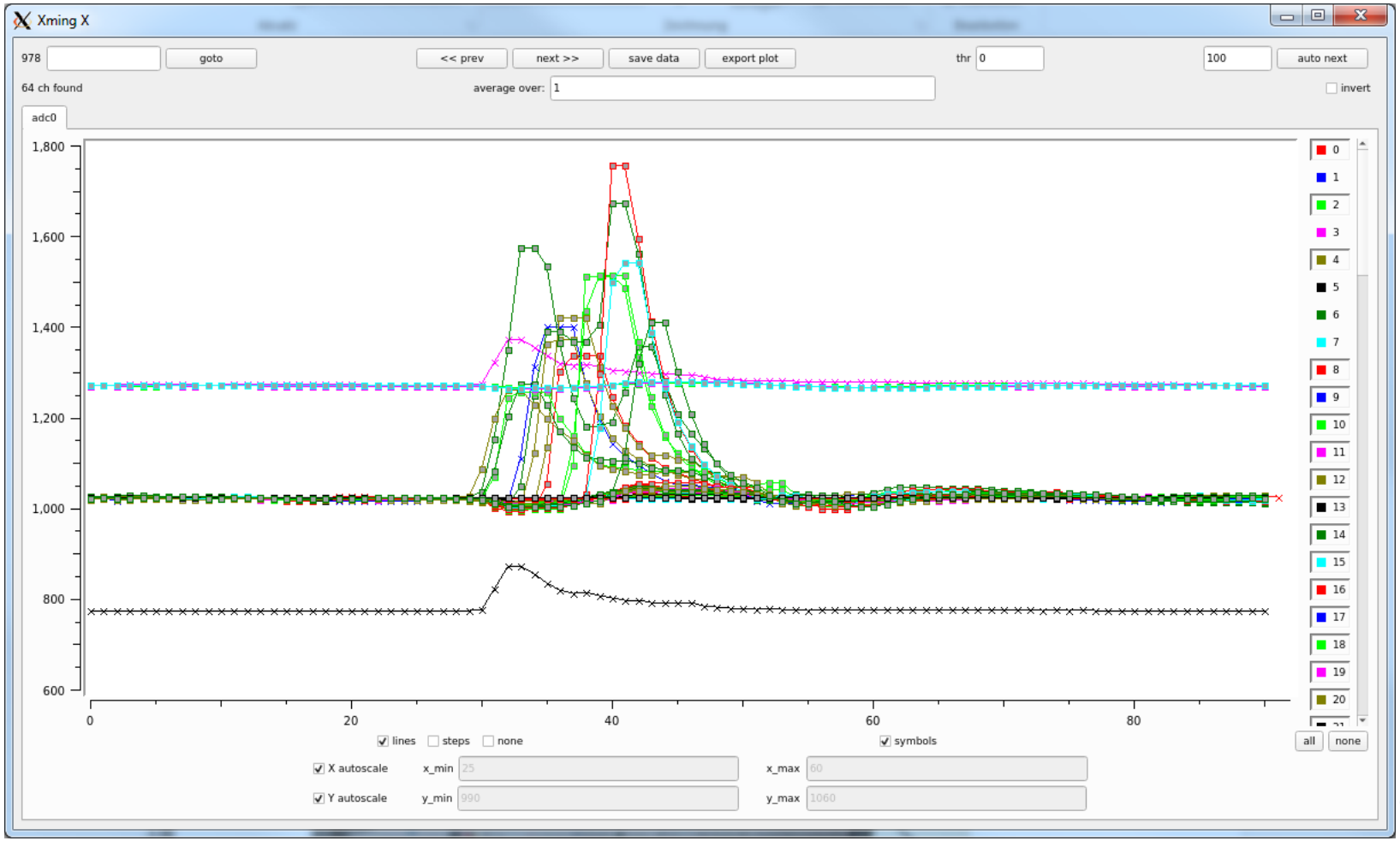


2. The longest (~107 mm digital ADC lines offers not a stable signals)

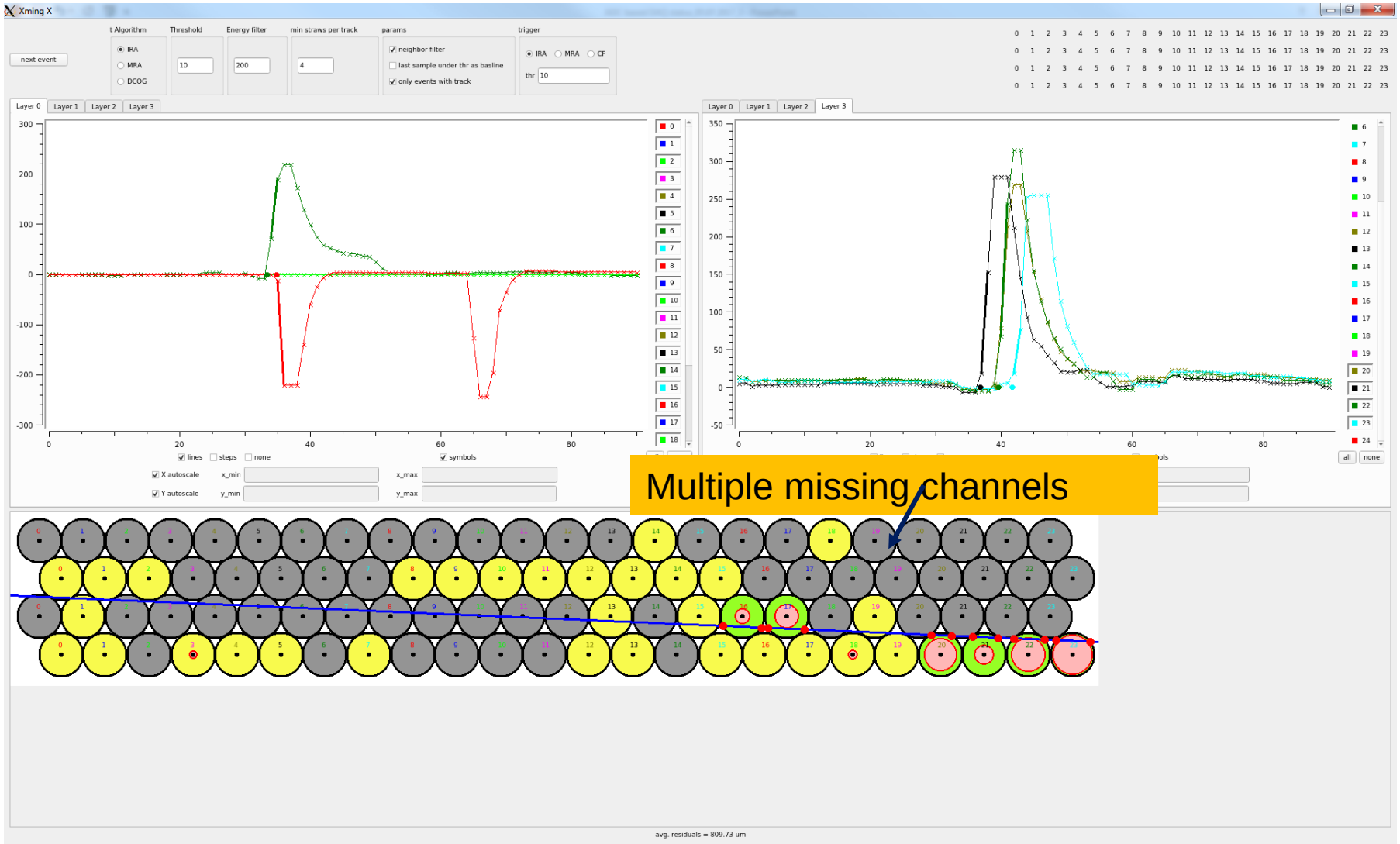


Errors detected during test beam.

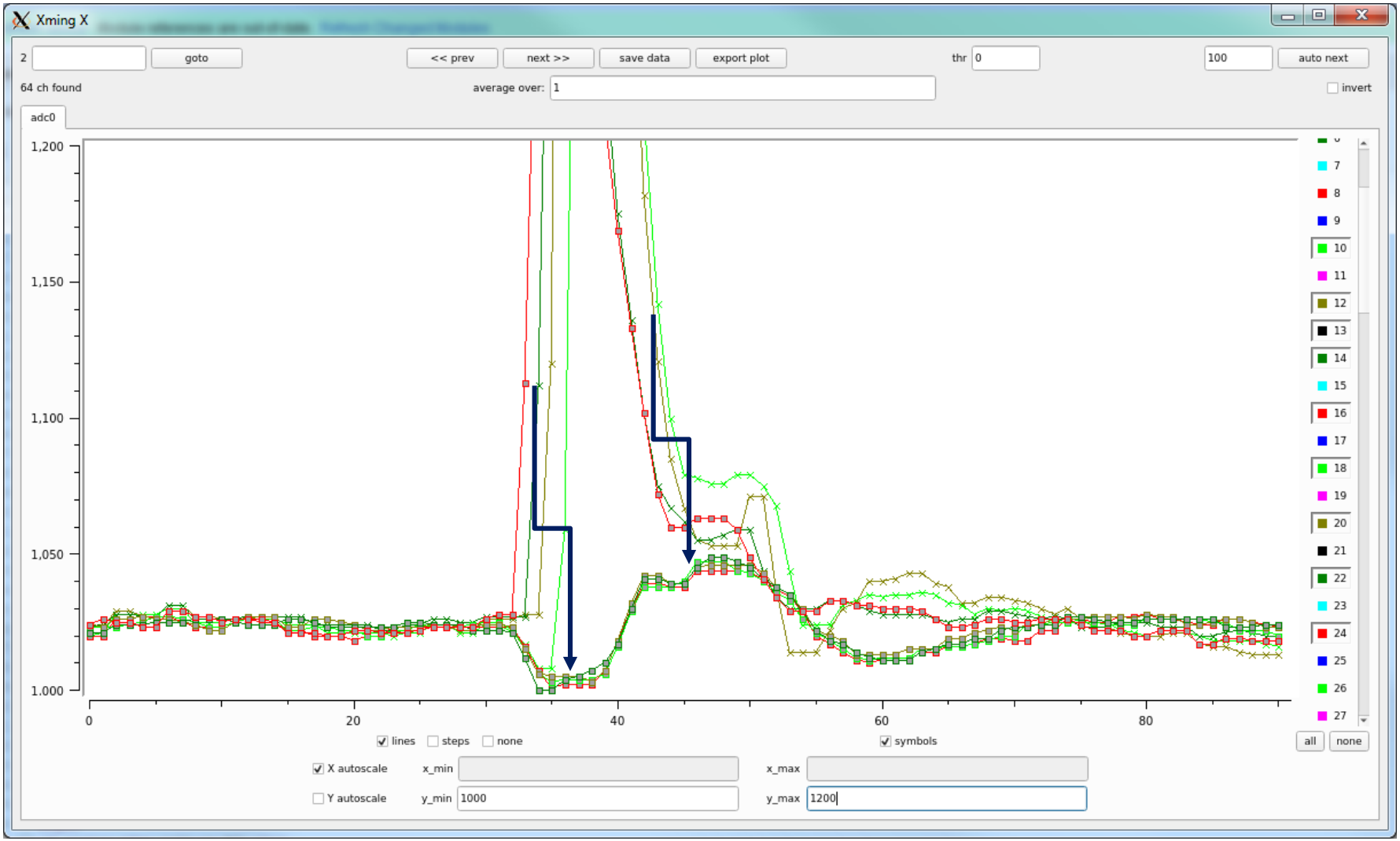
Positive and negative shifted baselines, providing reasonable signals?? The answer is simple: the backplane connector has a pressed technology and provided a bad contact. Dependent on either p or n lines are not connected the baseline is shifted in one or other direction. If the both lines are not connected→ missing channels→ ca 20 +8 s.e. (RTM error).



First tracking using a new DAQ



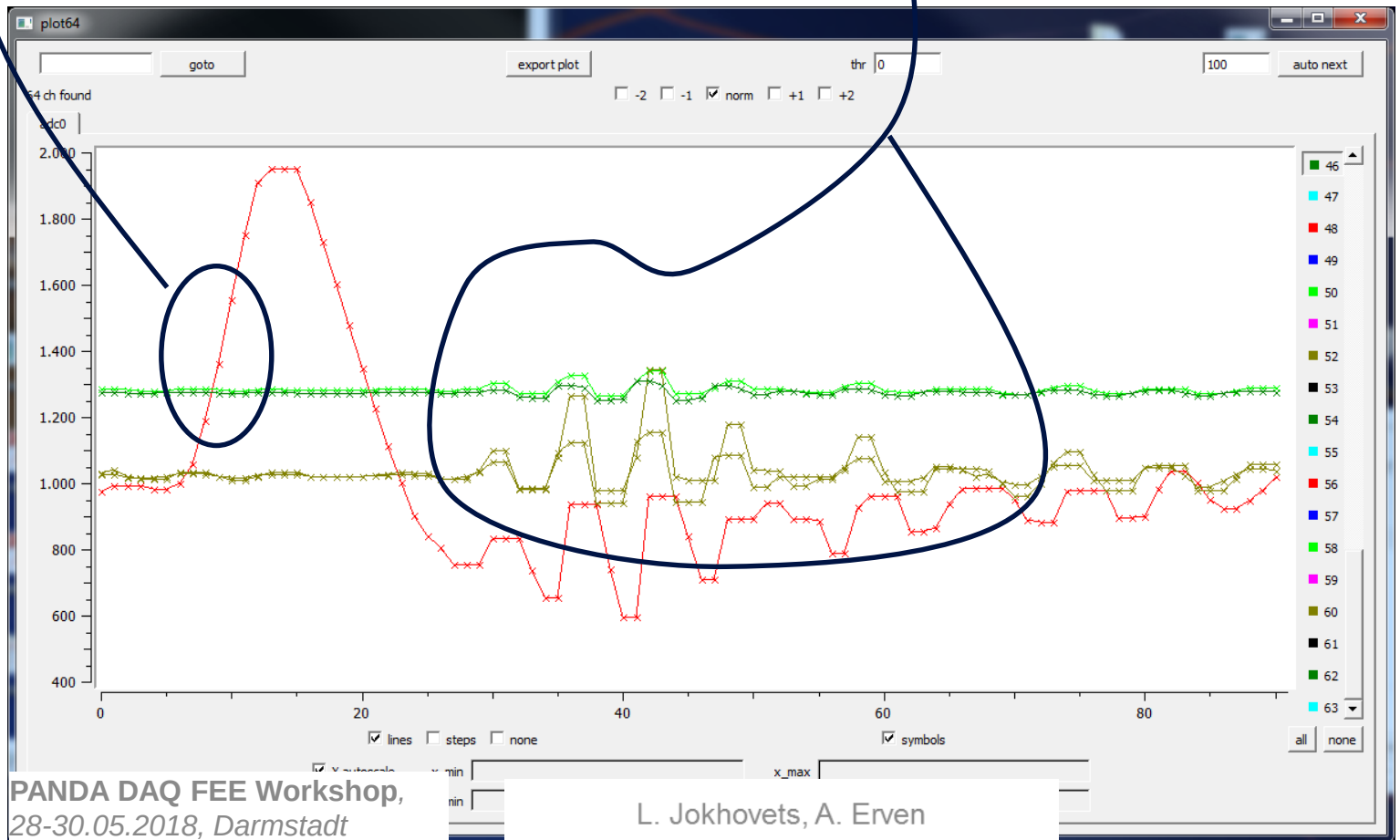
Expected undesired effects:
1. Crosstalk ~ 5%



Cross Talk verification (on amplifier board and on Samtec cable connecting HV coupling crate and Processing crate)

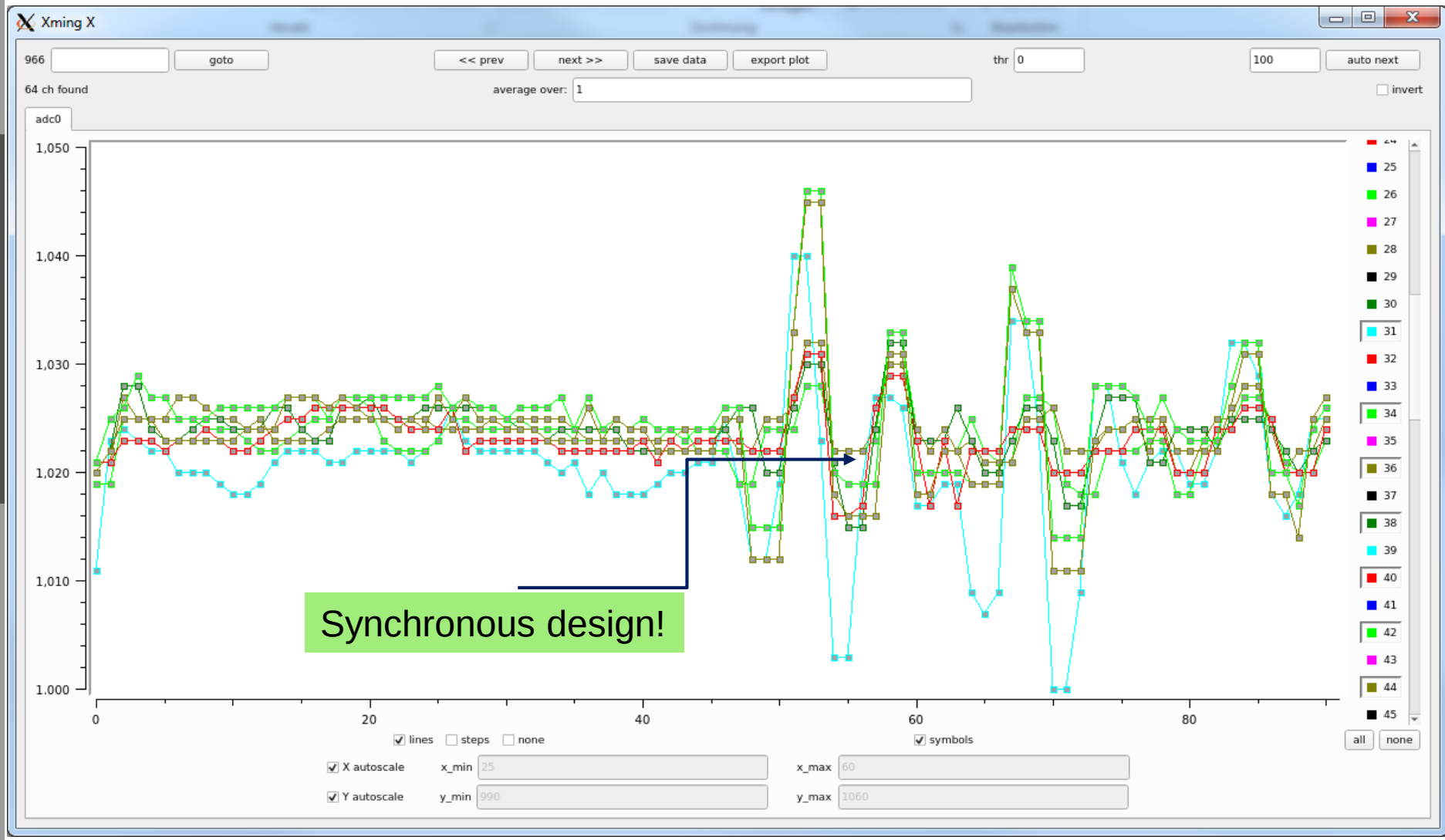
FORSCHUNGSZENTRUM

1. The crosstalk effect is not observed. Is the reason for this effect STTs or other cabling??→ feather investigation is necessary.
2. However, the resolution in our design is not strong affected by a crosstalk, moreover, we can detect and resolve it.
3. We see a noisy signals in not shielded setup. Attention- also without 8 m long micro coax !



Expected undesired effects:

2. Coherent noise, be proposed coming mostly from Samtec cable. Comparing to the previous picture the shielding reduces the noise factor ca 4-5.



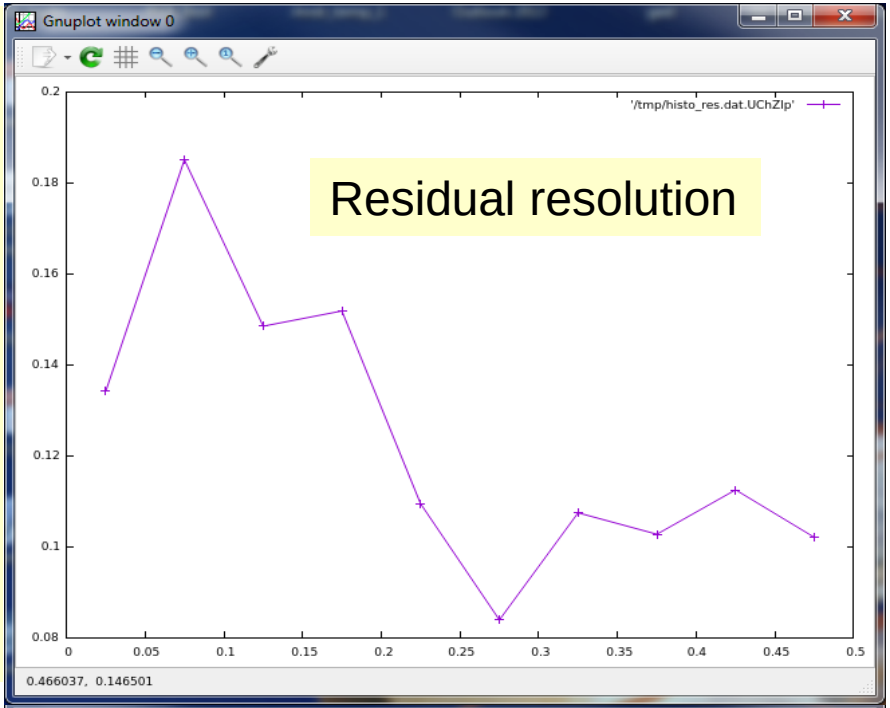
Spatial resolution leading edge discriminator , 100 MSPS

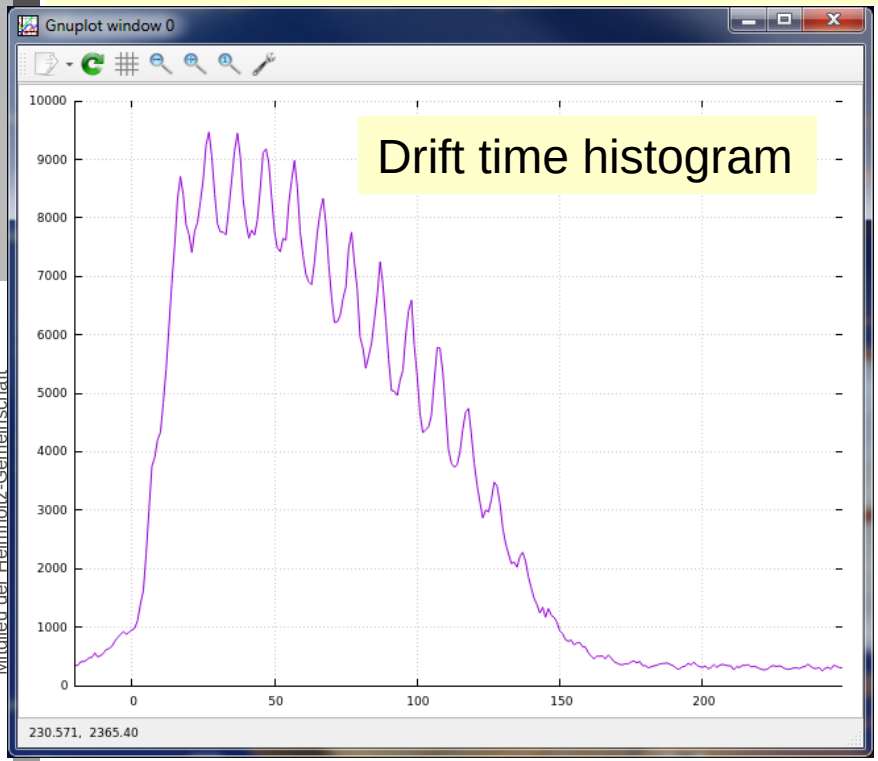
Parameters:

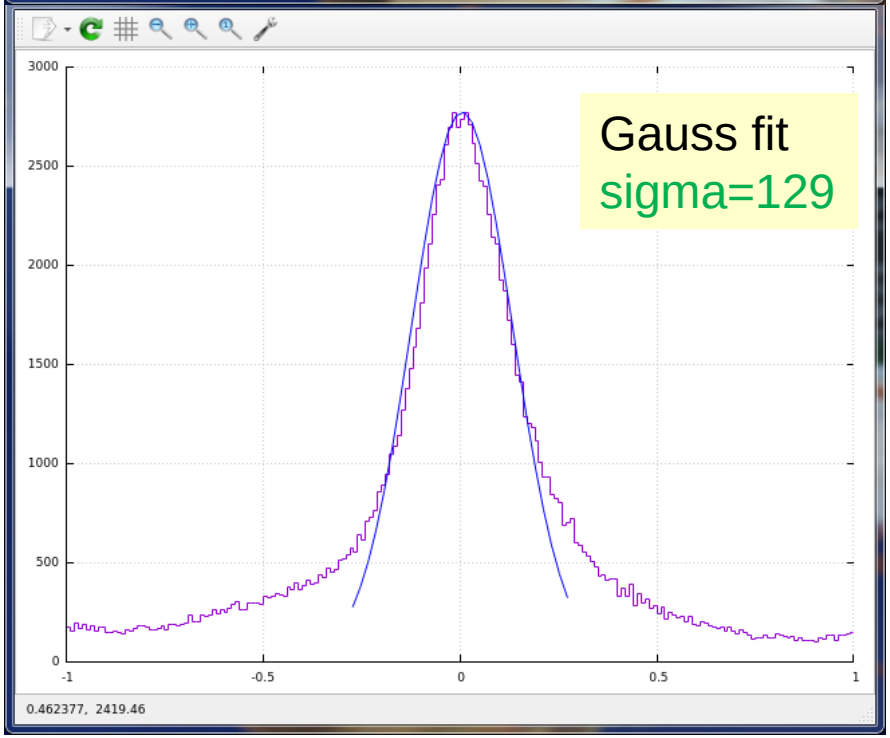
Threshold =20 (noisy design);

Energy filter=250

>6 STTs on track





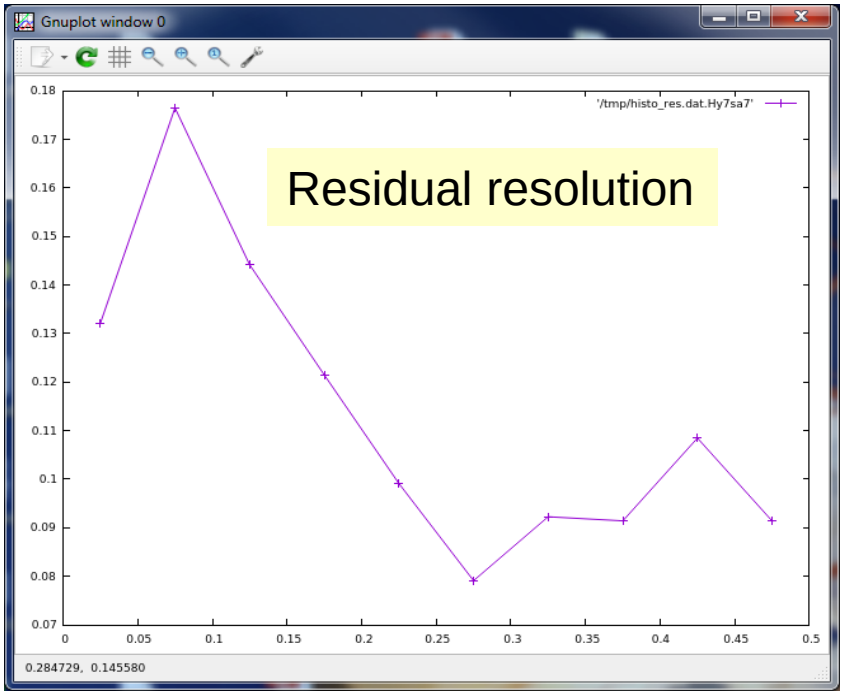


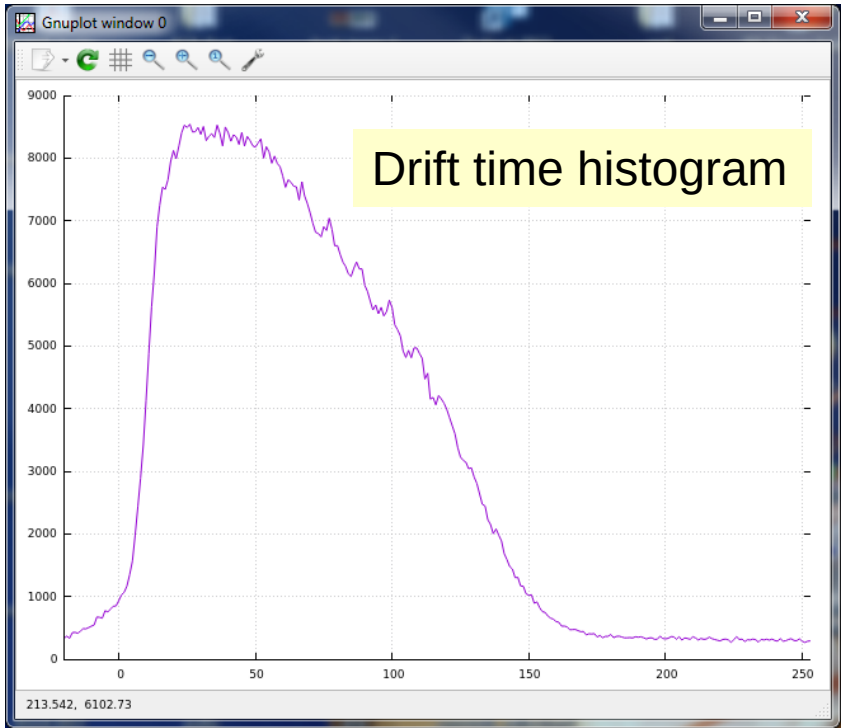
Spatial resolution leading edge discriminator technique (our method), 100 MSPS

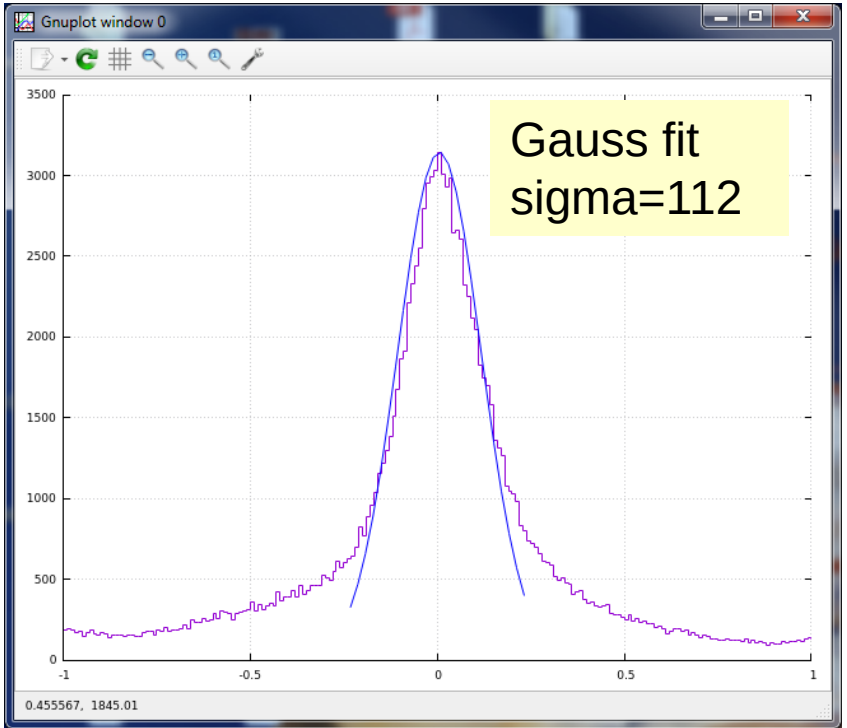
Parameters:

Threshold =20 (noisy design);

Energy filter=250







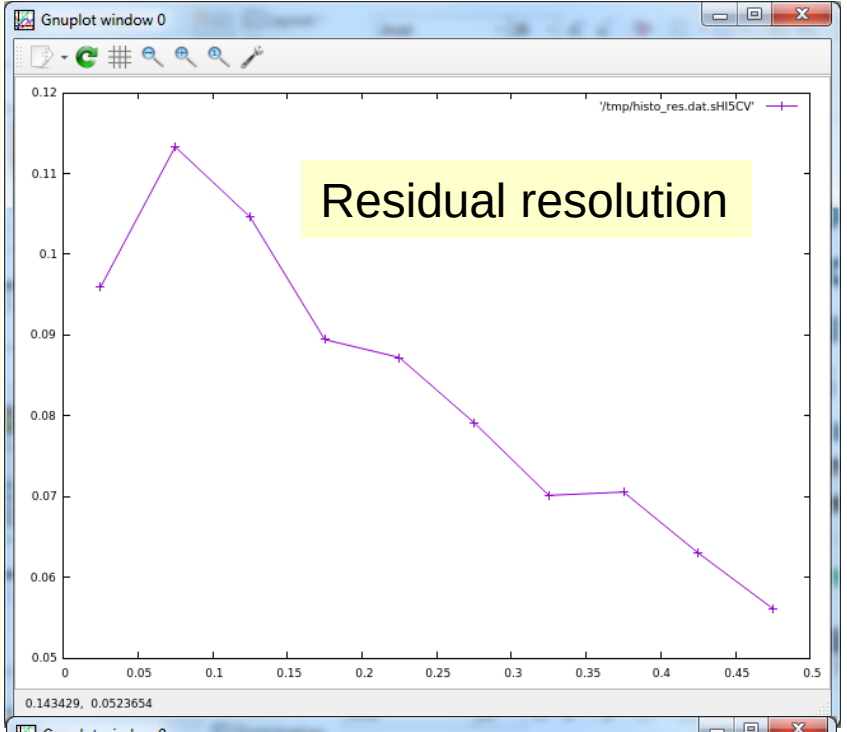
Spatial resolution leading edge discriminator technique (our method), April 2016, 16 channels

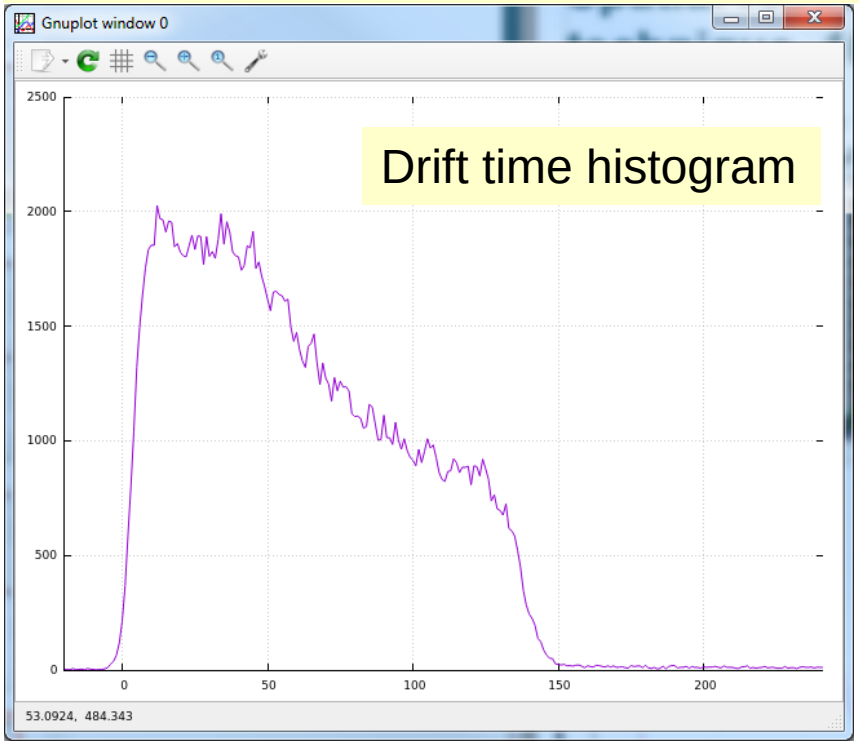
Parameters:

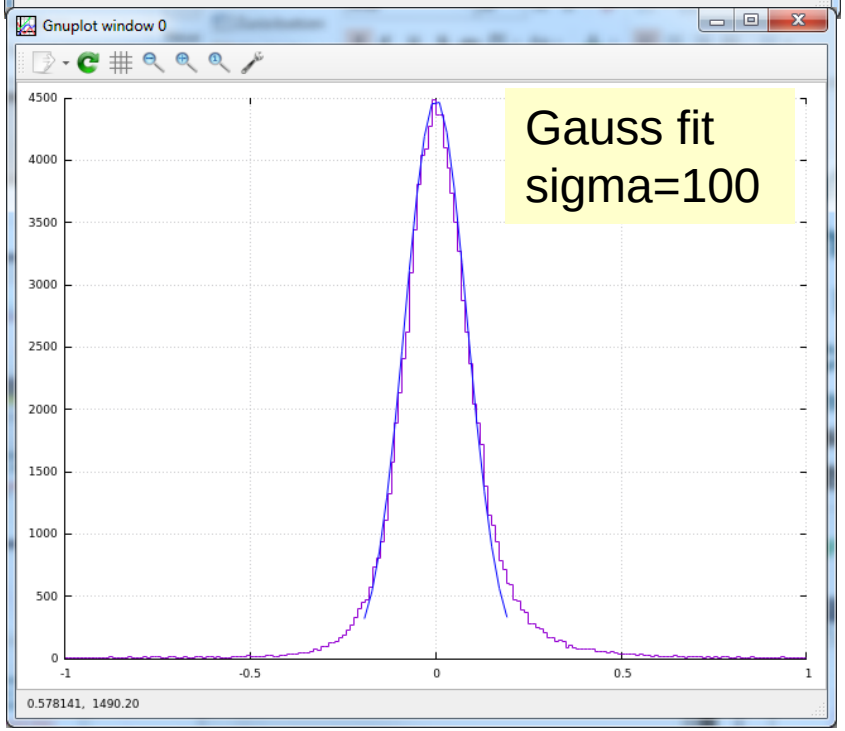
Threshold =5

Energy filter=200

>10 STTs on Track







Processing Firmware,

For 160 channels FW takes only 20% from Virtex XC7V585T resource.
Failed by test beam, delivering high amount of low energy hits, proposed coming from coherent noise.
Should be corrected. During test beam we have got raw data.
They will be used as simulation input for FW debugging.

The very first version of new developed ADC based DAQ (new HV coupling, new open VPX crate with new amplifier/shaper board, as well as sampling processing board) is able to provide a reasonable tracking data.

We have some debugging / improving issues. They will be performed without HW- redesign. Cosmics tracking will be used to verify this process.

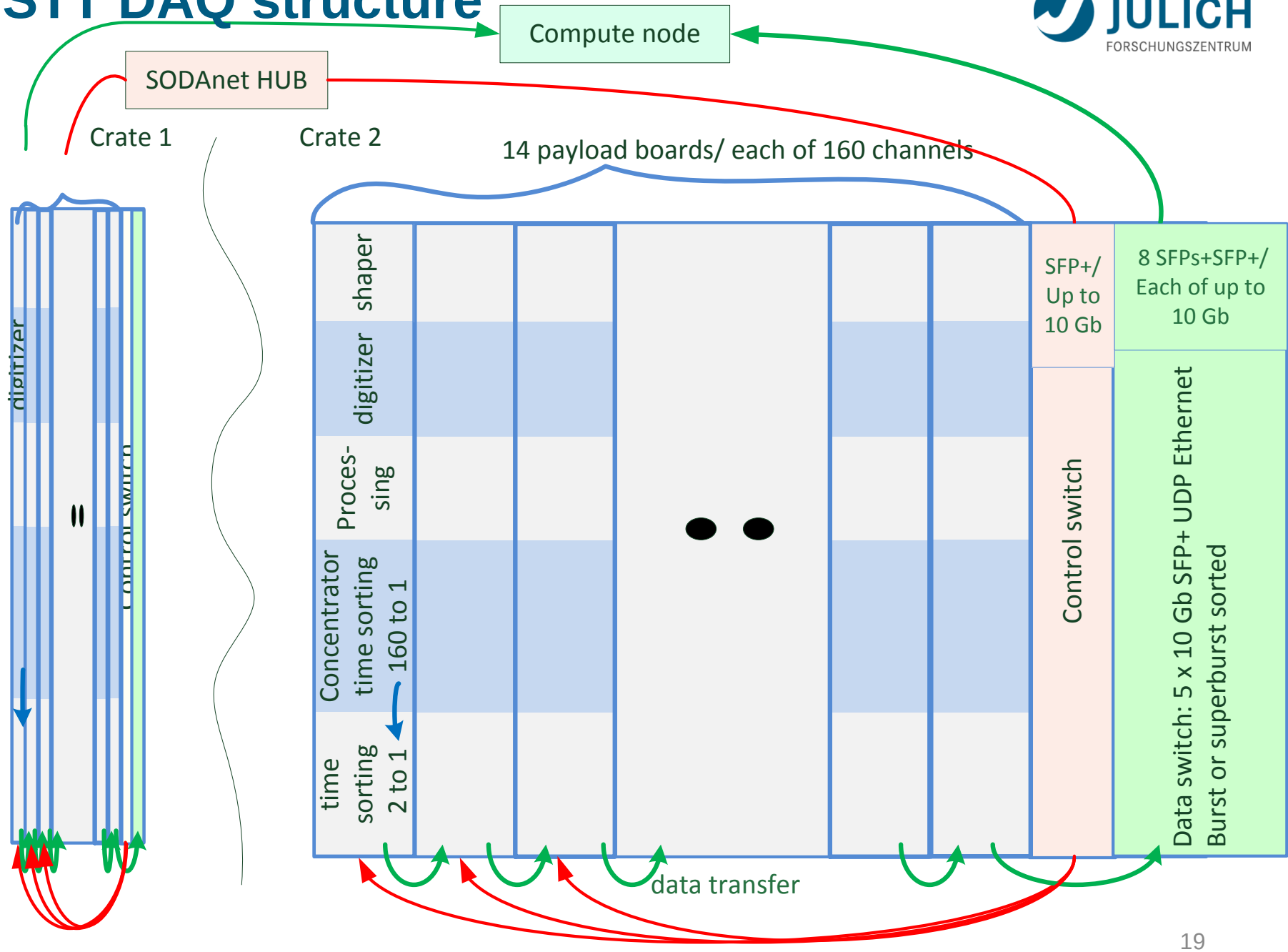
4 Years ago we have proposed a new high integrated DAQ system.

And now we are here: insides of only two crates

- Amplifiers/shapers
- sampling
- And processing for all 4200 channels are implemented

More over these crates will include also Data Concentrator and Controller for SODAnet communication and clock distribution.

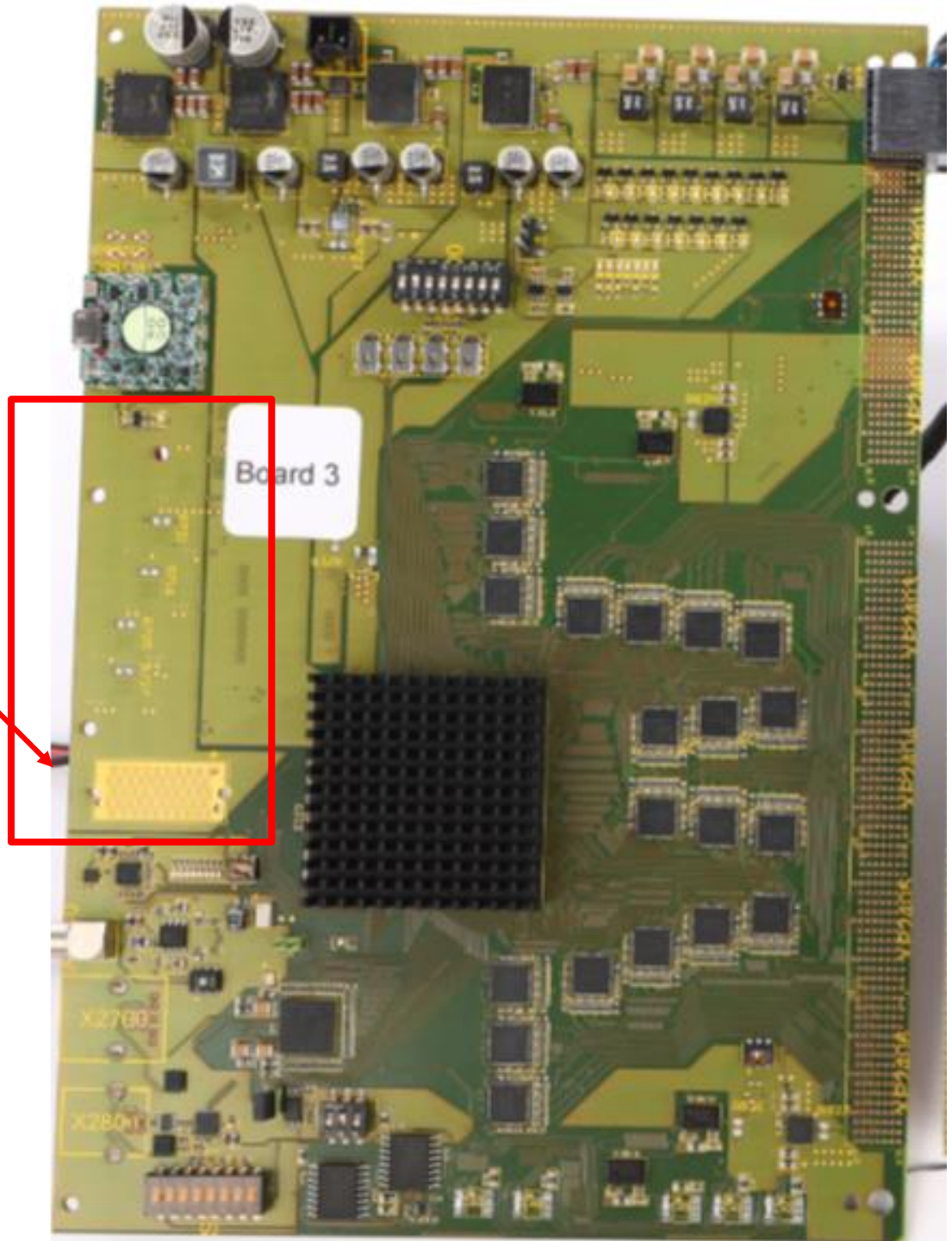
STT DAQ structure



Two steps to reuse our payload boards for control switch and data concentrator development

1. Easy evaluation of 10 Gbit GTX on Virtex 7 using our payload board

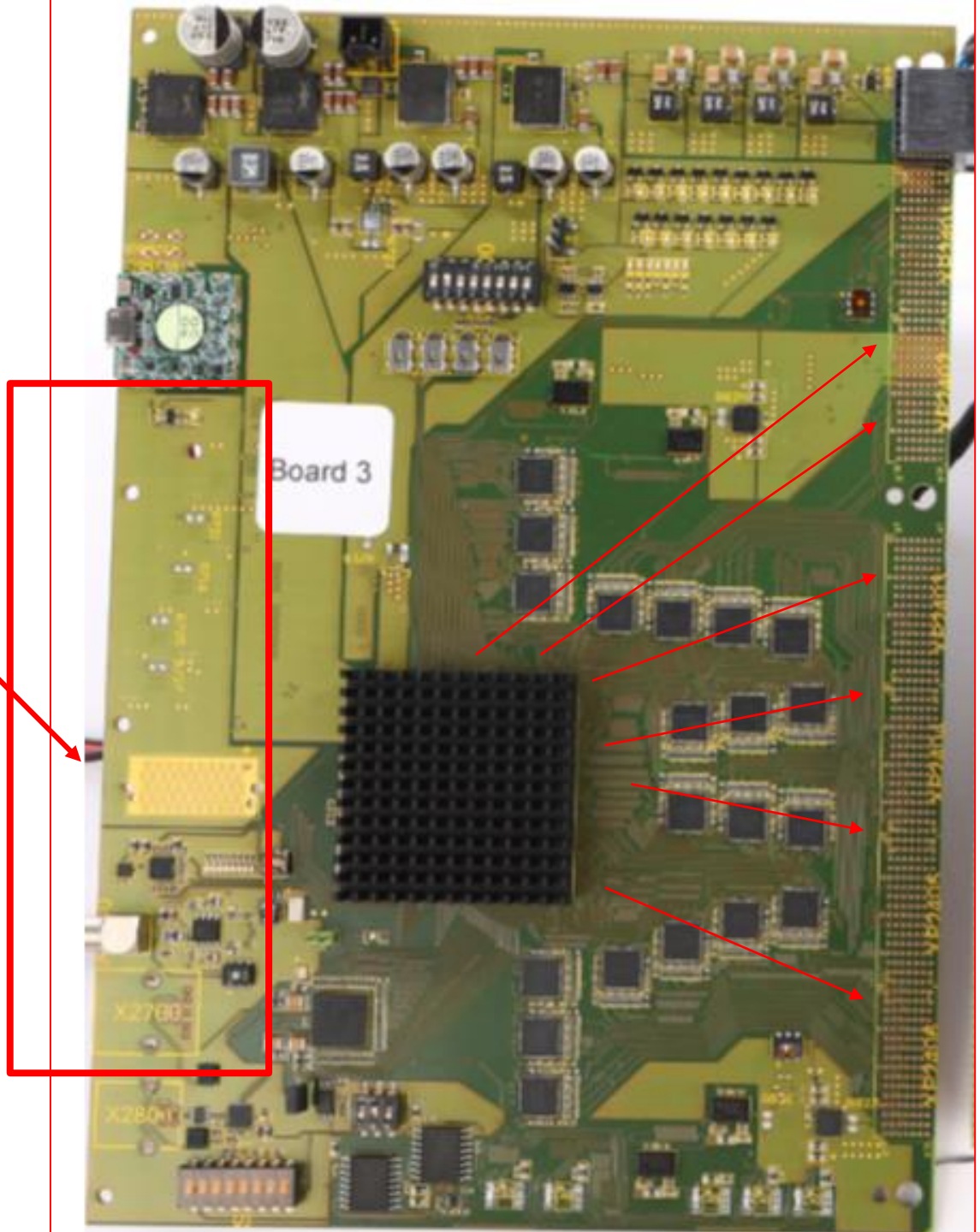
- There are all Power supply also for MGT Transceivers.
- Add-on board is foreseen with available connections to GTX-Banks.



2. Using design of the same payload board,

we integrate SFP connectors and instead of ADC, route serial links to backplane providing clock distribution to payload boards and data acquisition from these.

We benefit from ready to use power supply, slow control, and programming circuits.



We are making a progress.

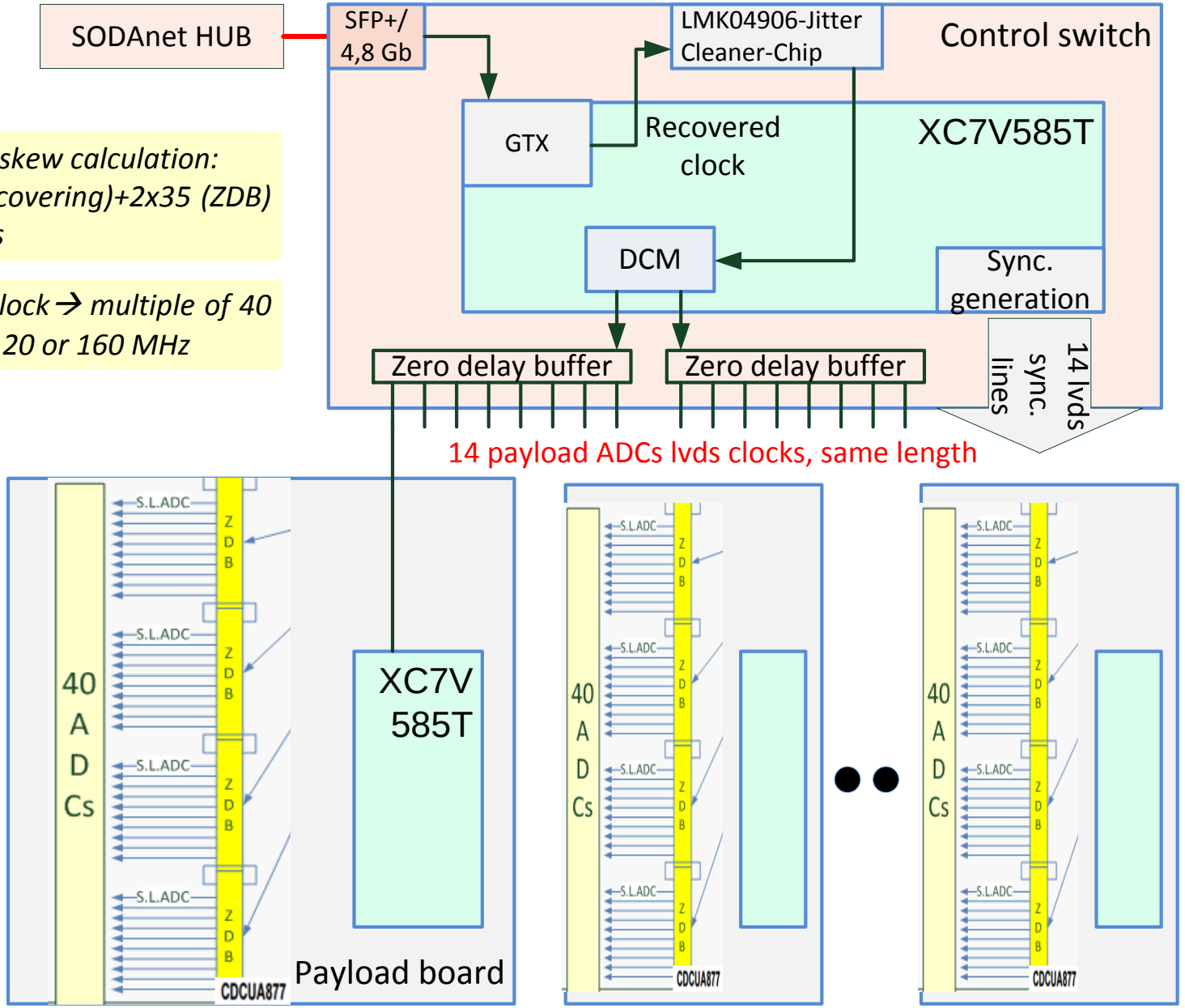
In one year the whole configuration should be ready.

One year more is required for debugging and test.

Thank You very much!

1. clock skew calculation:
70 ps(recovering)+2x35 (ZDB) =<145 ps

2. ADC clock → multiple of 40 MHz → 120 or 160 MHz



2.7 Test beam results 28.03.2016

1 GeV/c, Ar- CO_2 80/20, 1800 V