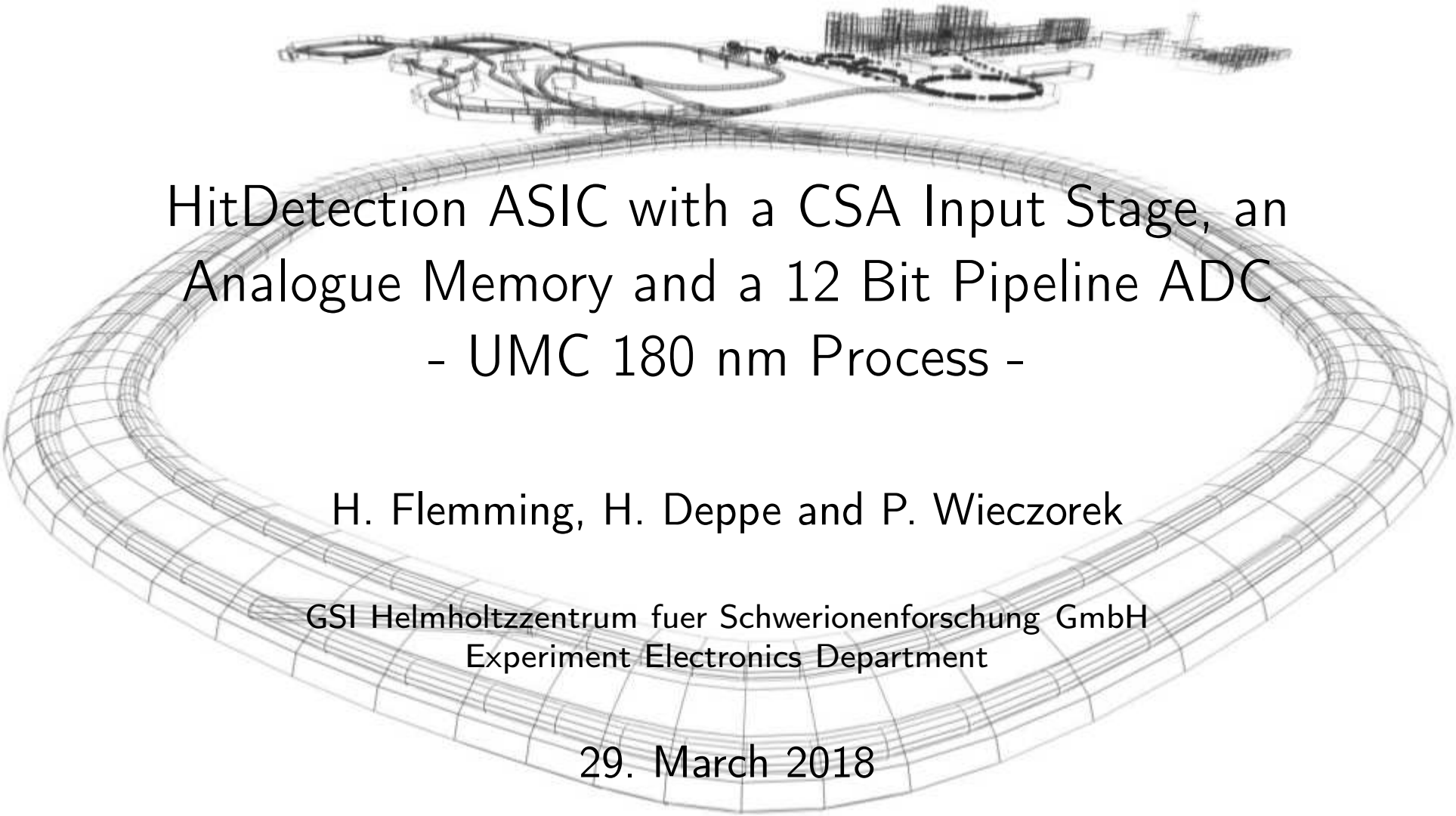


HitDetection ASIC with a CSA Input Stage, an Analogue Memory and a 12 Bit Pipeline ADC - UMC 180 nm Process -

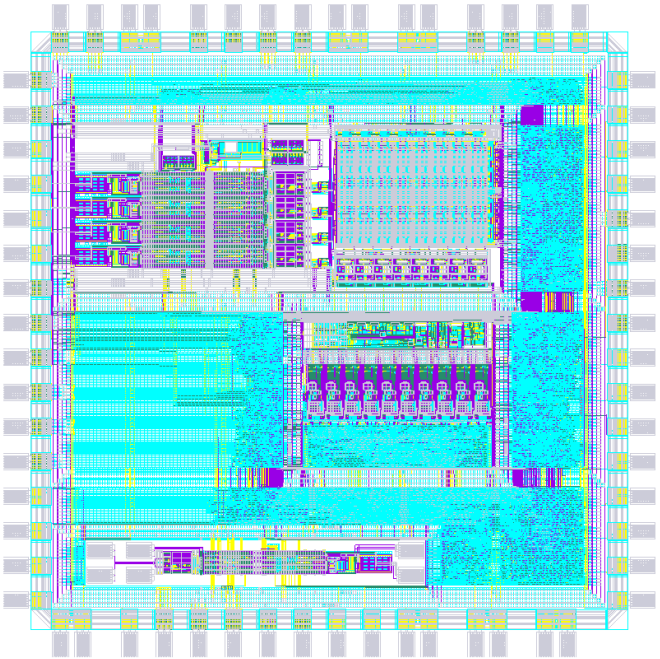
H. Flemming, H. Deppe and P. Wieczorek

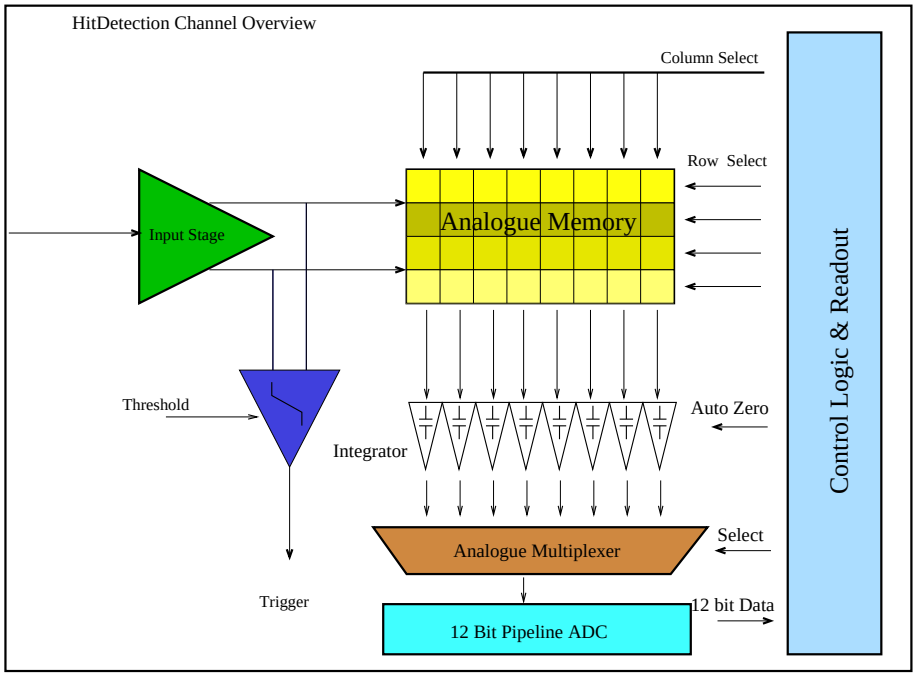
GSI Helmholtzzentrum fuer Schwerionenforschung GmbH
Experiment Electronics Department

29. March 2018

Outline

Outline

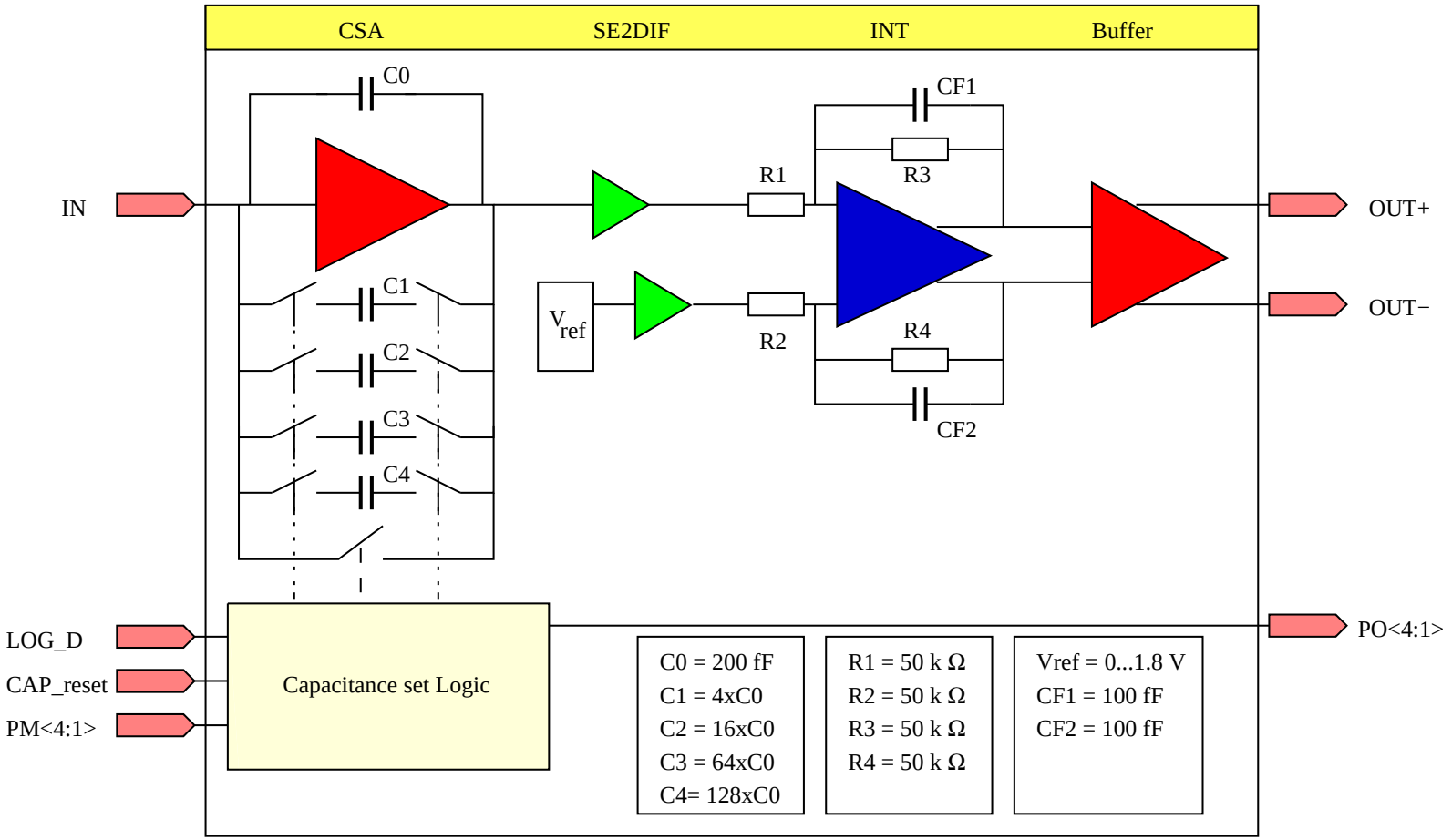




- Chip area (4 channels): $3250\,\mu\mathrm{m} \times 3250\,\mu\mathrm{m}$
- Mode of operation

- HitDetection ASIC: Self-triggered analogue transient recorder and a 12 bit pipeline ADC
  - Input stage: differential input buffer or a charge-sensitive amplifier
  - Discriminator as trigger and a differential analogue memory for signal storage
  - On-chip 12 bit pipeline ADC for signal digitalisation

Outline



- Input stage consists of a CSA, single-end to differential stage and differential output

- Noise calculations for the input transistor as dominant noise source

$$ENC_{th}^2[e^2] = \frac{10 \cdot k_B \cdot T}{8 \cdot q^2} \frac{C_T^2}{\tau_s \cdot \sqrt{(k_x \cdot W/L \cdot I_{ds})}} \quad (1)$$

$$ENC_{1/f}^2[e^2] = \frac{4 \cdot K_f}{C_{ox}^2 \cdot q^2} \frac{C_T^2}{W \cdot L} \quad (2)$$

$$ENC_{DET}^2[e^2] = \frac{2}{q} \cdot I_{det} \cdot \tau_s \quad (3)$$

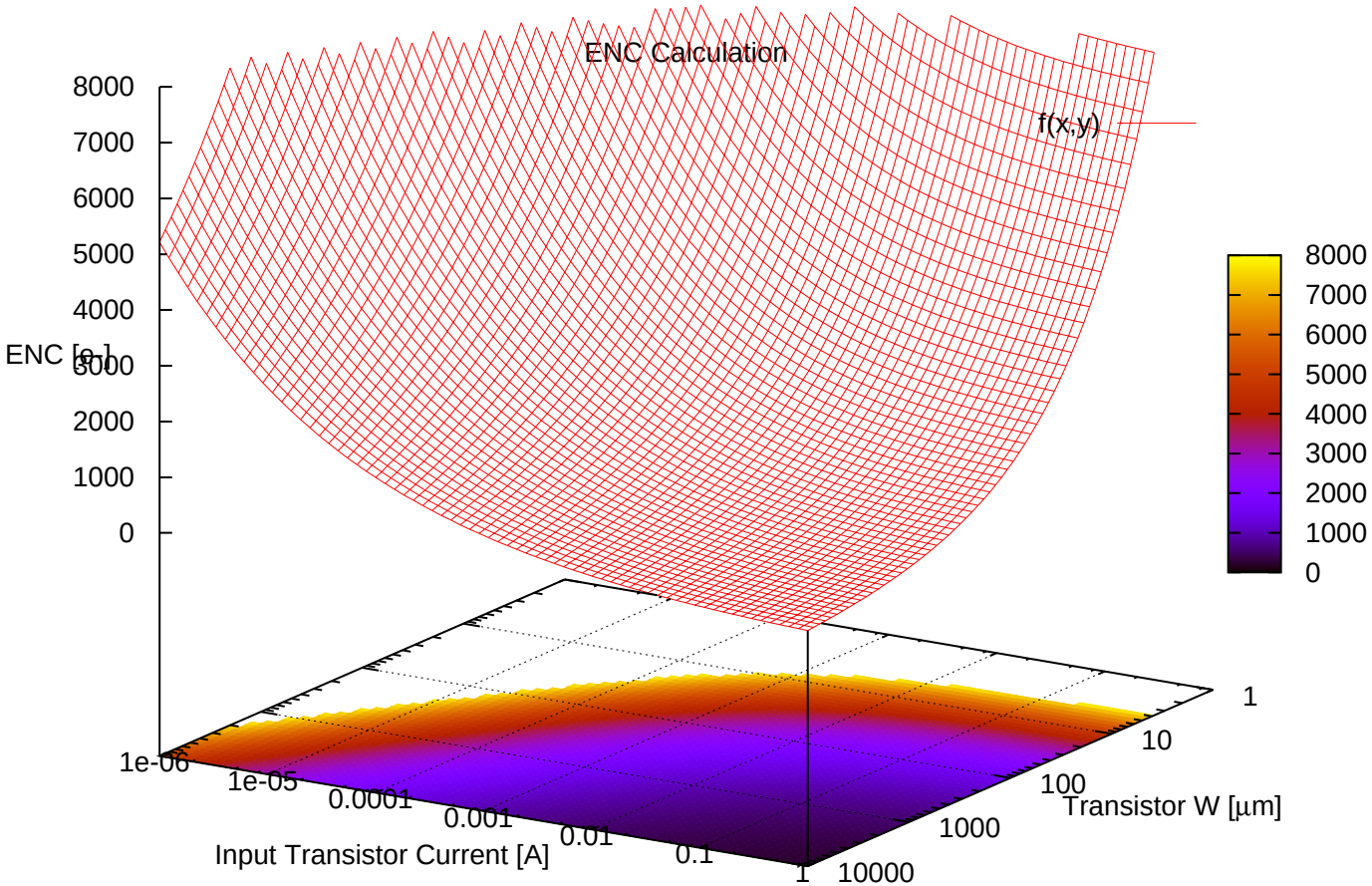
$$ENC_{tot}^2 = ENC_{th}^2 + ENC_{1/f}^2 + ENC_{DET}^2 \quad (4)$$

Const.	Value	Unit
k_B	1.38E-023	J/K
C_{ox}	8.22E-003	F/m^2
q	1.60E-019	C
T	300	K
K_f	5E-027	C^2/m^2
k_x	129E-006	F/Vs

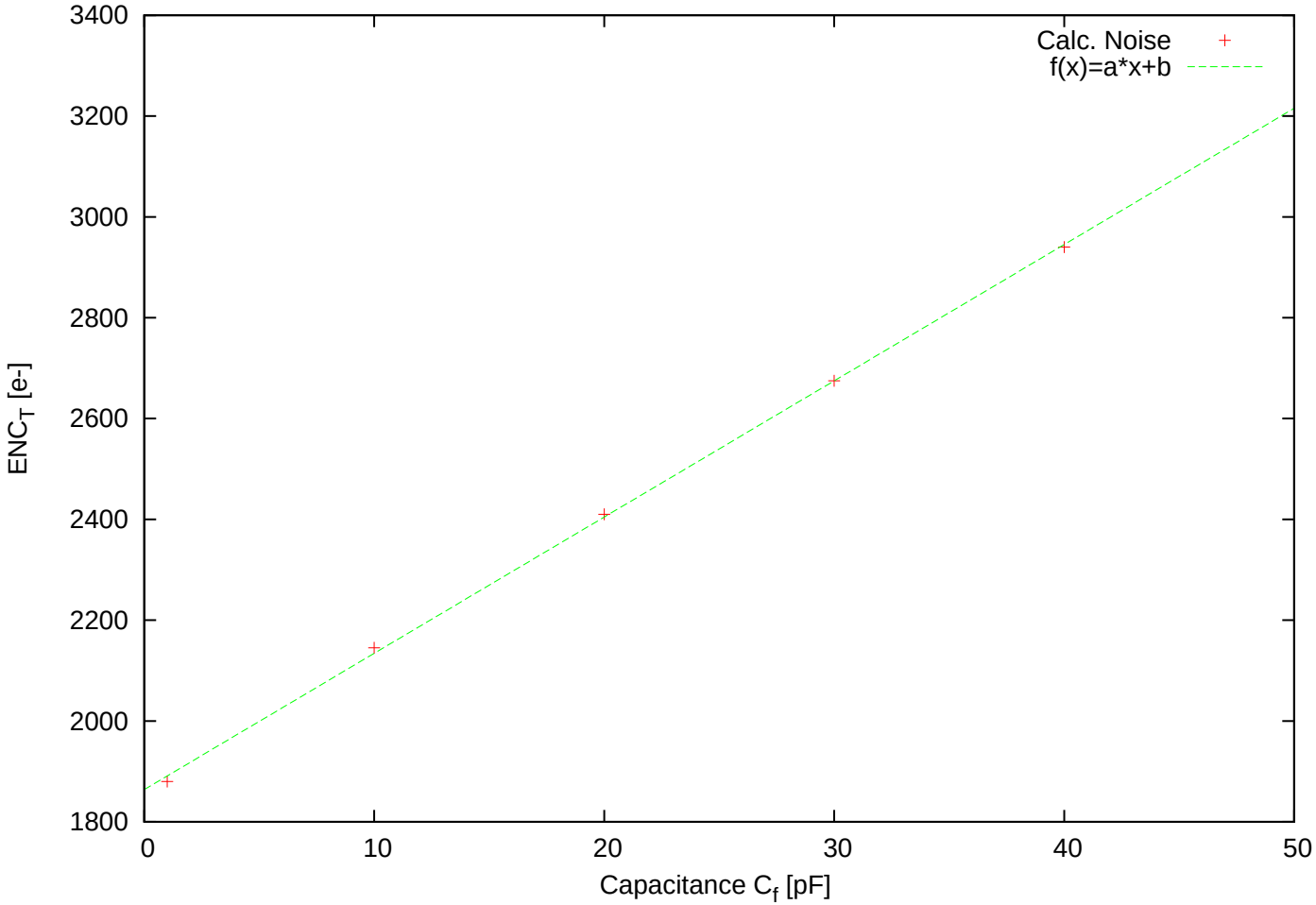
Variable	Description
C_T	sum of all Cs at the input
W	transistor width
L	transistor length
I_{ds}	current through transistor
τ_s	shaping time
I_{det}	detector leakage current

- Set parameters for current design
  - Implement small capacitance for stability in differential OTA
    $\Rightarrow$ integration time $\tau_s = 10\,\text{ns}$
  - Detector leakage current: $I_{det} = 10\,\text{nA}$ ... $100\,\text{nA}$

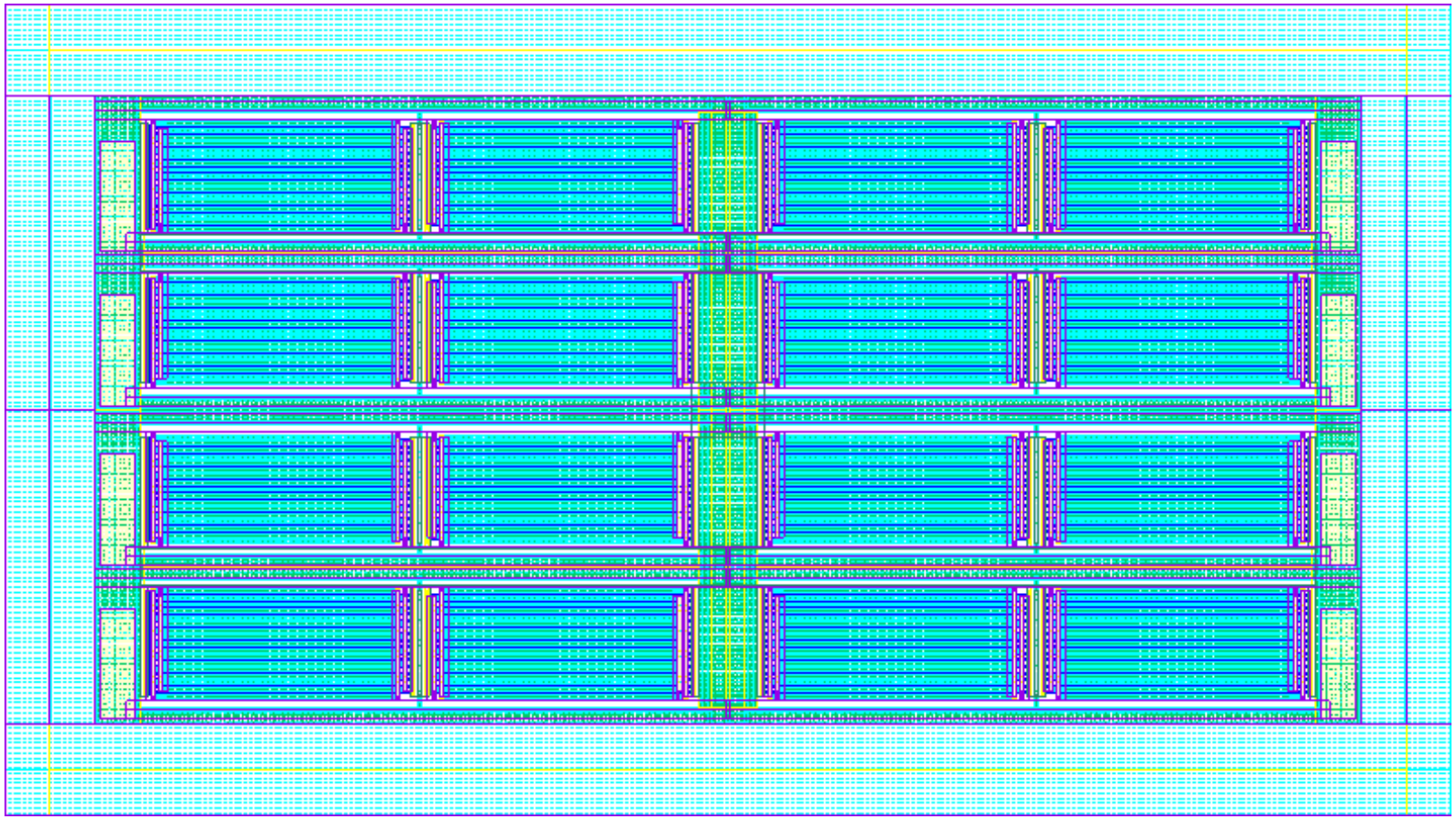
- Optimise transistor parameter W/L and I_{ds}
  - Input transistor ratio W/L high $\Rightarrow$ large input capacitance
  - Current through input transistor large $\Rightarrow$ high power consump.



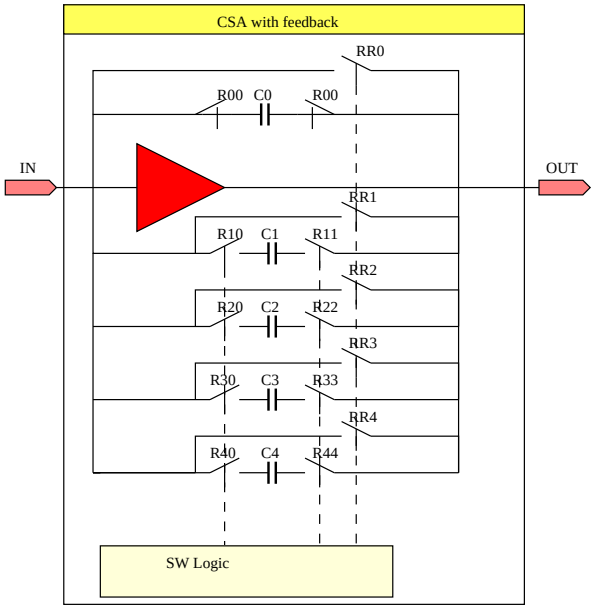
- Optimise parameter $C_T = C_{gs} + C_{det} + C_f$
  - Low noise contribution $\Rightarrow$ C_T as small as possible
    - Detector capacitance C_{det}: is fix
    - C_{gs} increase with the transistor geometrie
      $\Rightarrow$ trade off between transistor width and capacitance
    - Feedback capacitance C_f: $\Rightarrow$ trade off between noise and dynamic range
- C_{gs}=20 pF; C_{det}=50 pF; C_f=1 pF .... 30 pF
  $\Rightarrow$ C_T= 71...100 pF

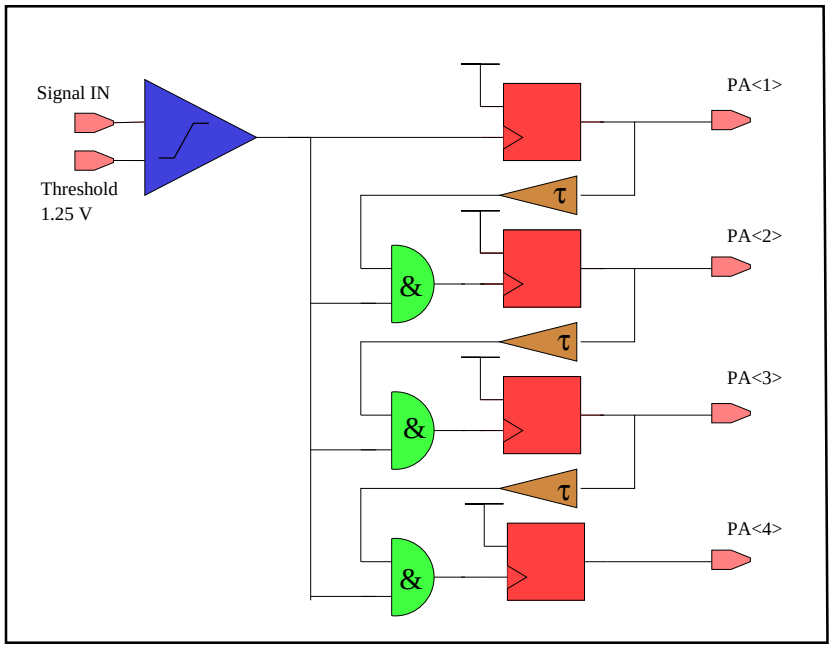


- Small capacitance for small signals $\Rightarrow$ better SNR



- Layout input transistor with W/L: 35 556 ($256 \times 25/0.18$)
- Input transistor area on chip: 330 µm $\times$ 95 µm

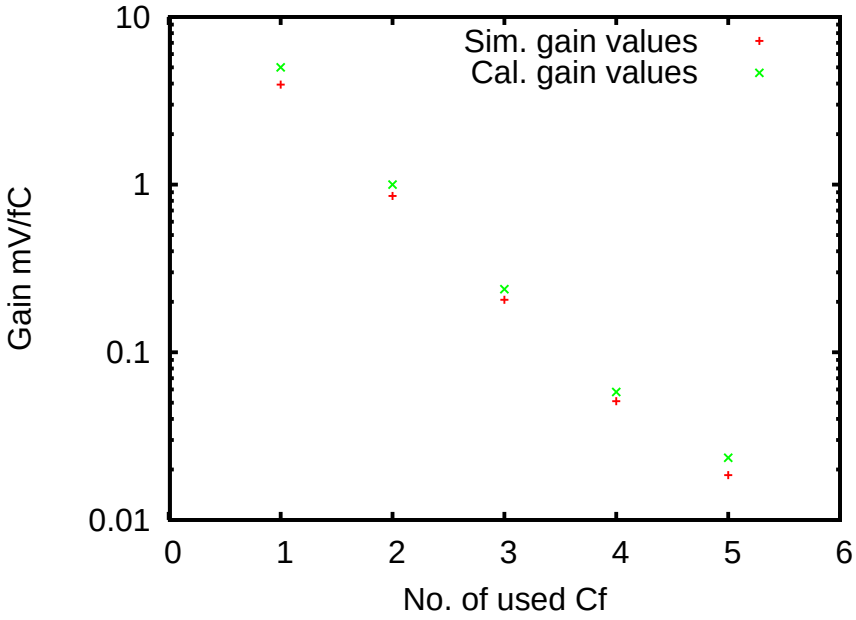


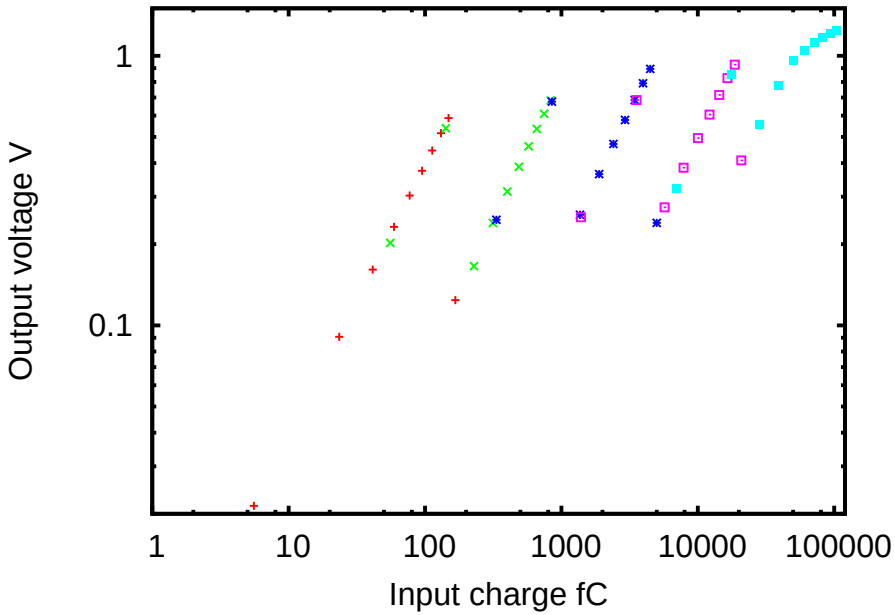


- Architecture of the programmable feedback
- Design of the self switching - logic with one comparator
  - Option: Automatic or manual setting of feedback capacitance C_0 to C_4

No.		Unit	Area	Unit
C_0	200	fF	220	μm^2
C_1	$4 \times C_0$	fF	880	μm^2
C_2	$16 \times C_0$	fF	3523	μm^2
C_3	$64 \times C_0$	fF	14080	μm^2
C_4	$128 \times C_0$	fF	28160	μm^2

- Symmetrical layout for small capacitances
- Multiple of a unit $C_0 = 200\,fF$
- Max. input capacitance is 42.4 pF
  (Output 1 V $\Rightarrow$ max. input charge is 42.4 pC)
- Capacitances placed over active area of the amplifier

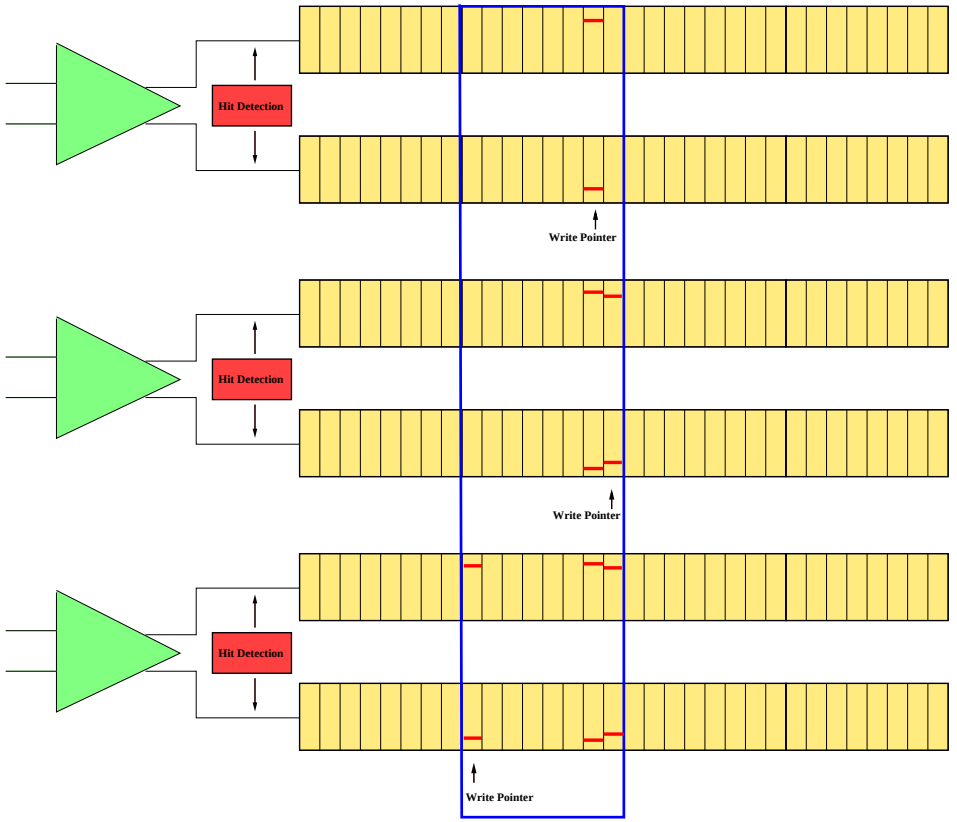




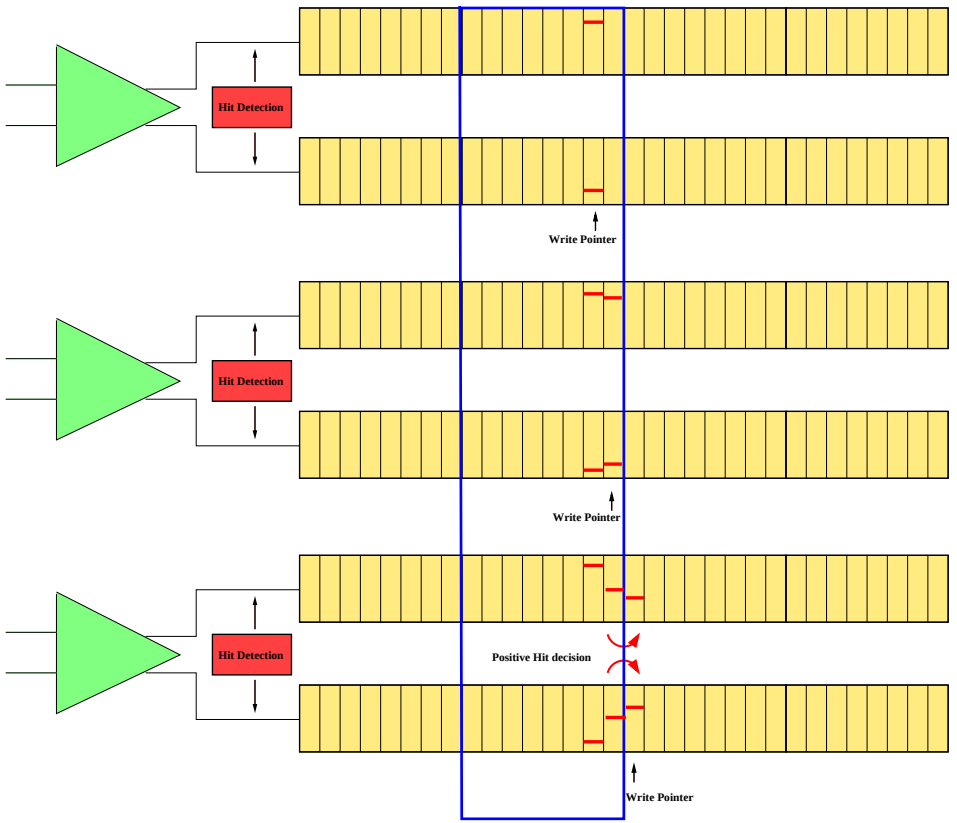
- Gain: 5mV/fC and 0.024 mV/fC
- Lin. output range up to 42 pC

Outline

- Capacitor array used as analogue memory
- Analogue memory is divided into blocks with configurable size
- Signals from input receiver are sampled and stored at the position of write pointer
- Write pointer rotates inside of one block

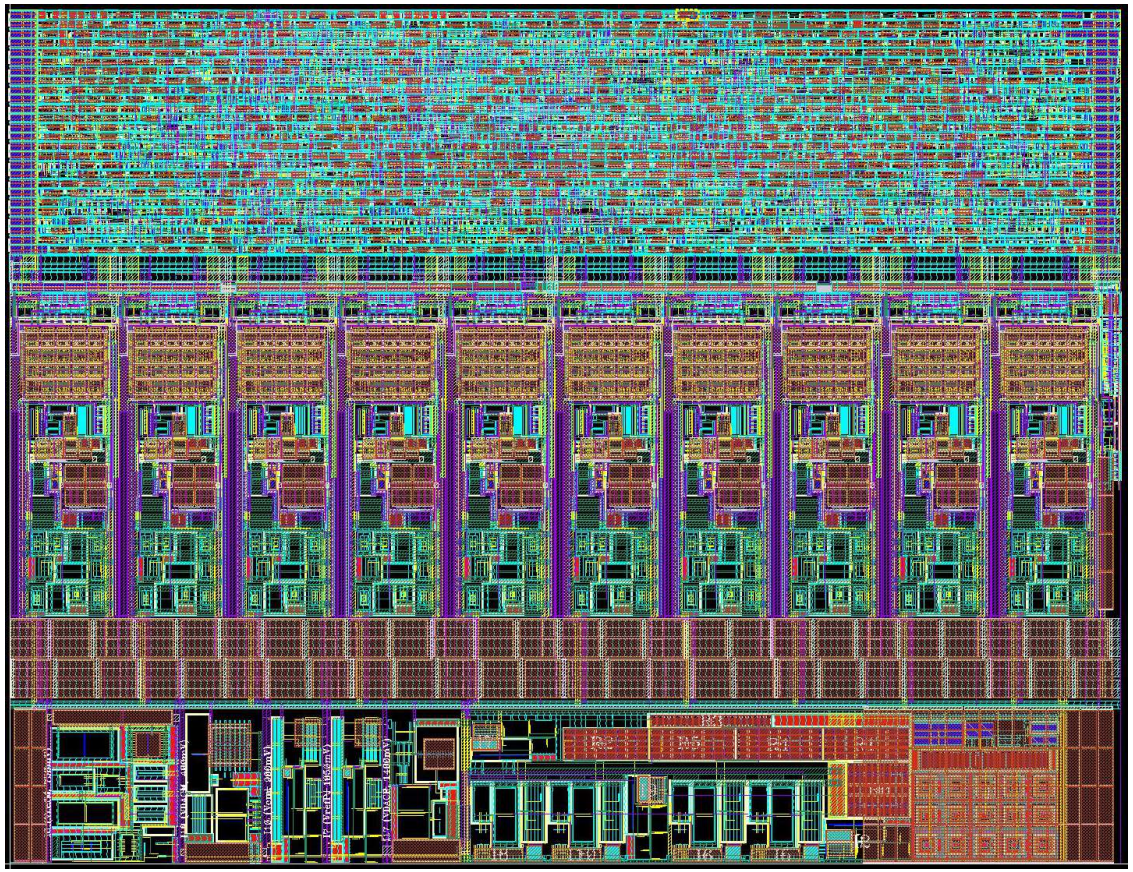


- Signals from particle energy deposits are detected by the hit detection unit
- Write pointer switches to the next memory block
- Signal transient is stored in previous block
- Analogue readout when shared ADC is available
- Block is available again for signal storage

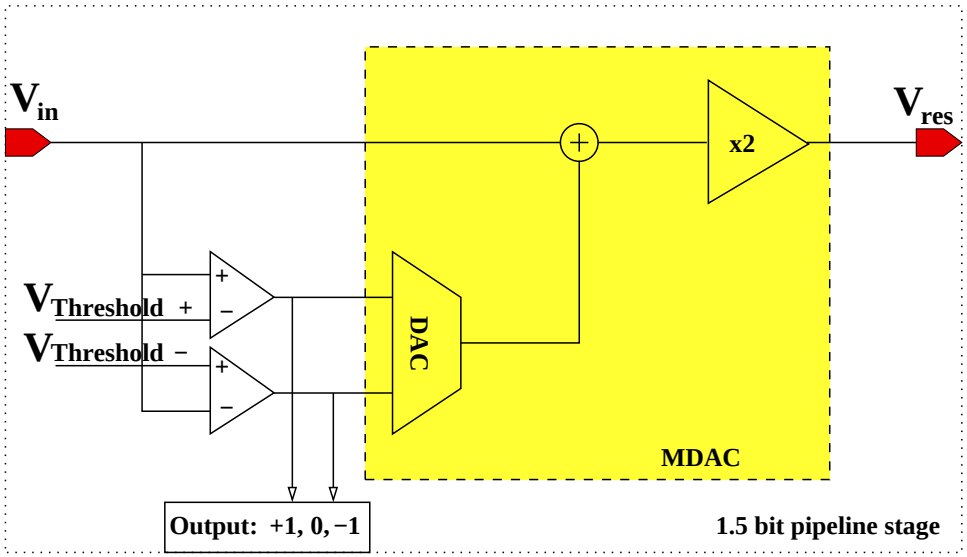


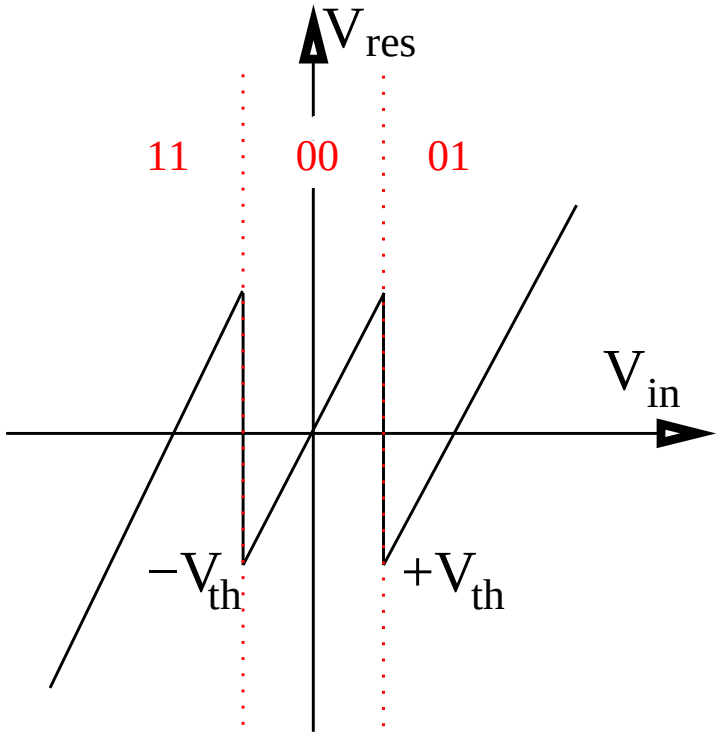
- Requirements for the integrator stage:
  - Fully differential operation
  - Input DC range: 0 - 1.5V
  - Pulse amplitude: $\pm$ 1V
  - High linearity
  - High slew rate
- Use a fast integrator architecture without CMFB
  - Differential input
  - Auto zero circuit
  - Output buffer

Outline

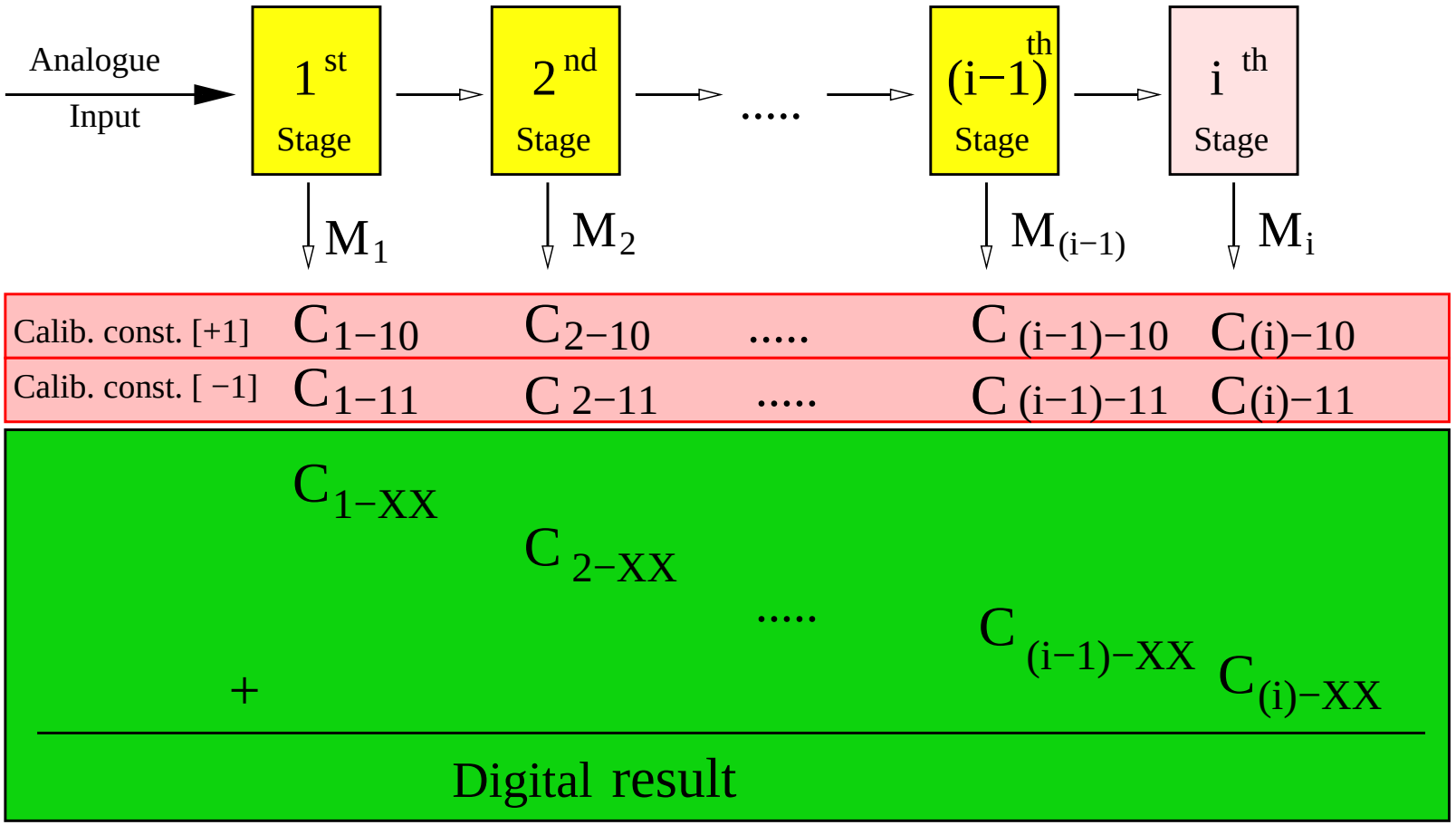


- Layout of the 12 bit pipeline ADC ($715\,\mu m \times 930\,\mu m$)
- Central: 1.5 bit stage (total 10 stages); last stage only comparator
- Voltage references below the pipeline stages
- On top: Digital logic (includes calibration)

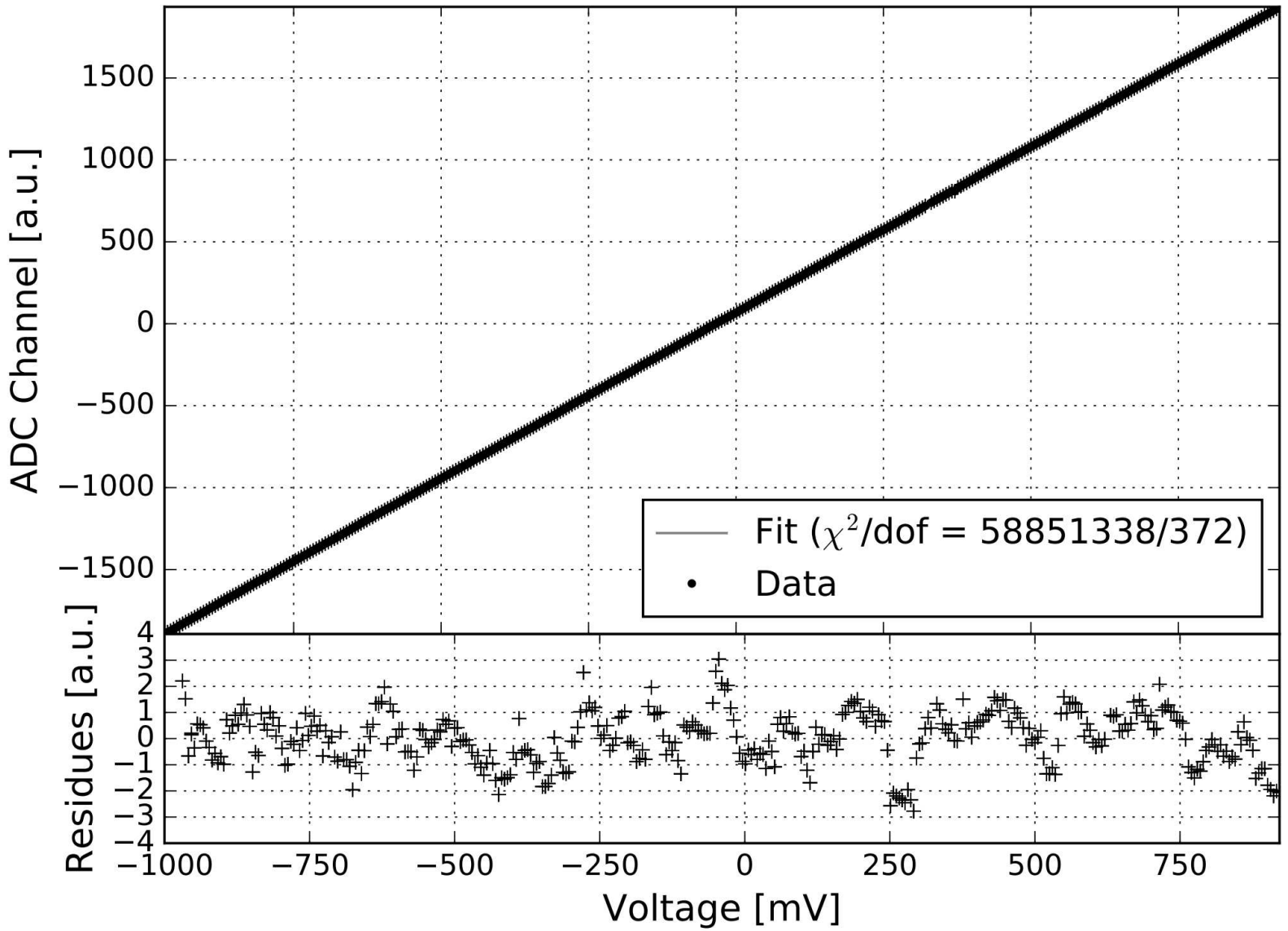


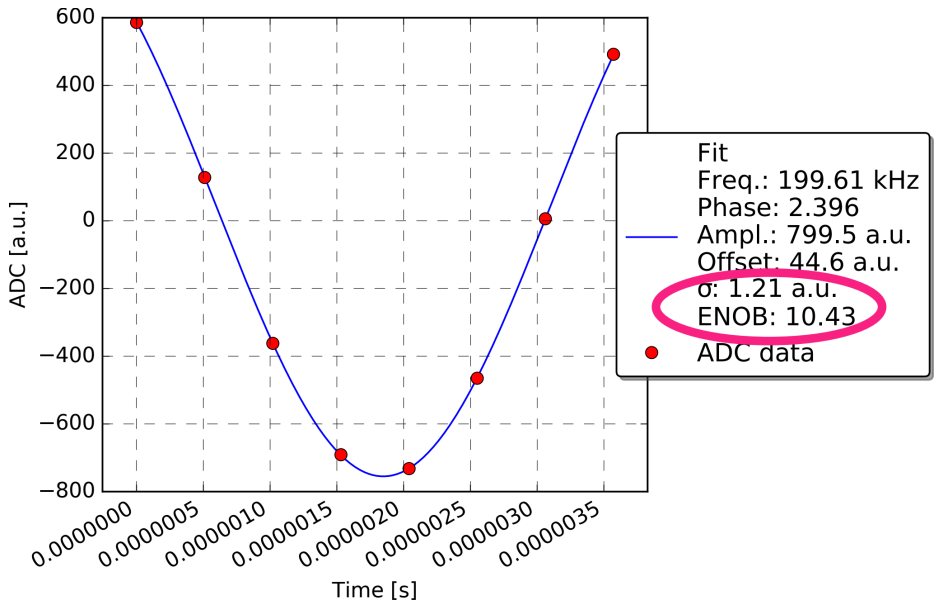


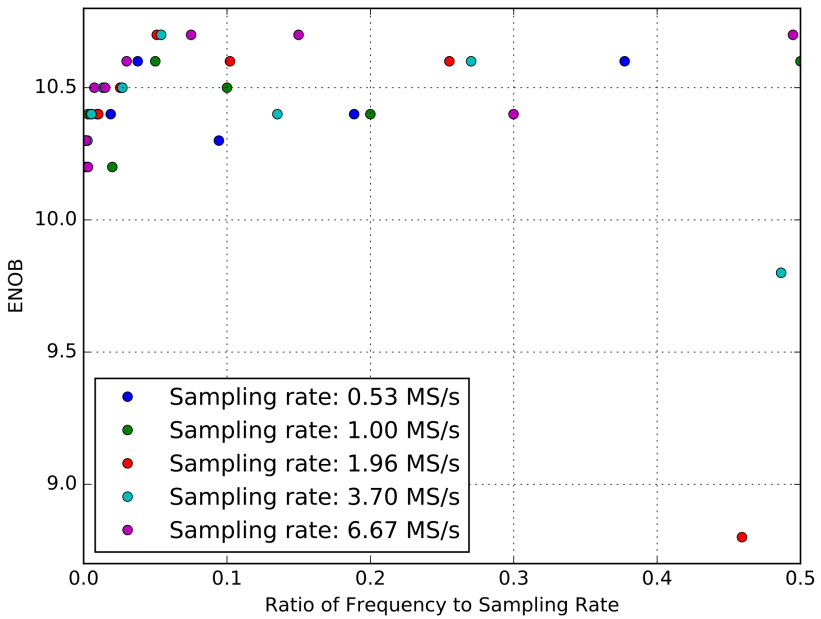
- MDAC works with 3 clock phases (reset/charge/readout)
- Amplifier: fast, stable, precise ⇒ switched design



- ADC measurements and analysis are done by Mainz colleagues


ADC Channel [a.u.]
1500
1000
500
0
−500
−1000
−1500
Fit (χ^2/dof = 58851338/372)
Data
Residues [a.u.]
4
3
2
1
0
−1
−2
−3
−4
−1000
−750
−500
−250
0
250
500
750
Voltage [mV]


ADC [a.u.]
Time [s]
Fit
Freq.: 199.61 kHz
Phase: 2.396
Ampl.: 799.5 a.u.
Offset: 44.6 a.u.
σ: 1.21 a.u.
ENOB: 10.43
ADC data


ENOB
Ratio of Frequency to Sampling Rate
Sampling rate: 0.53 MS/s
Sampling rate: 1.00 MS/s
Sampling rate: 1.96 MS/s
Sampling rate: 3.70 MS/s
Sampling rate: 6.67 MS/s

- Results of ADC measurements and analysis (carried out by colleagues from Mainz)
  - ADC has an INL of 2.26 LSB
  - ENOB of the ADC: 10
- Results of CSA measurements and analysis
  - ASIC is bonded and will be measured in June
- Results of memory measurements and analysis
  - Measurements and analysis are/will be done by colleagues from Mainz