Single Event Upsets in the PANDA EMC

Results from neutron and proton irradiations of the digitiser board

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Front-end electronics in the Electromagnetic Calorimeter

$\sim$ 600 front-end digitiser boards in the EMC

375 in Barrel   225 in Forward Endcap

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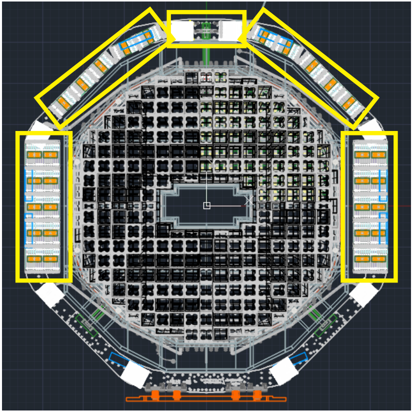

Figure courtesy of C. Schnier.

- Distributed over several crates placed around the detector perimeter.
- Two Xilinx Kintex-7 FPGAs per board.
- Of interest here: **SEUs** caused by neutrons and protons in FPGA.
- Interesting also for other subdetectors.

Proton irradiation

- In November 2016 at the AGOR cyclotron at KVI.

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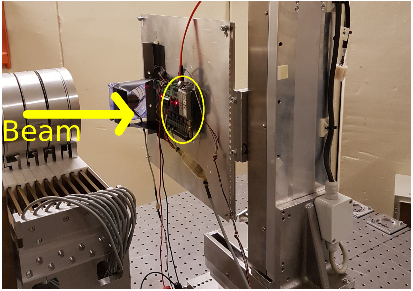
- Board perpendicular to the beam (covering half of the board). **One** FPGA read out.



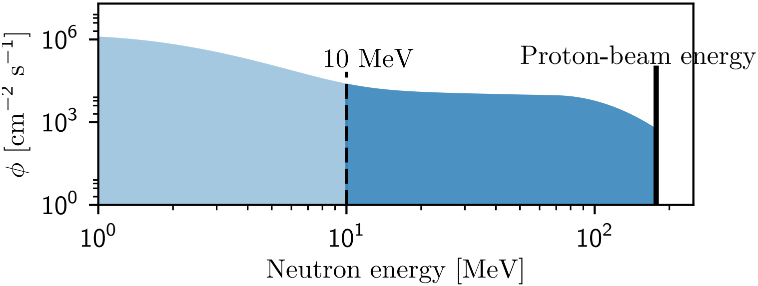
- Three proton energies:
  - 184 MeV (primary beam energy)
  - 80 and 100 MeV (with degrader)
- Total proton fluence: $\sim 4 \cdot 10^9$ cm^{-2}.

High-energy neutron irradiation

- In June 2016 at the The Svedberg Laboratory (TSL) in Uppsala.
- Proton beam (180 MeV) $\rightarrow$ W target $\rightarrow$ Neutron beam. Board perpendicular to the beam. **One** FPGA read out.

High-energy neutron irradiation

- In June 2016 at the The Svedberg Laboratory (TSL) in Uppsala.
- Proton beam (180 MeV) $\rightarrow$ W target $\rightarrow$ Neutron beam. Board perpendicular to the beam. **One** FPGA read out.
- Total neutron fluence: $2 \cdot 10^9$ cm^{-2} (>10 MeV).



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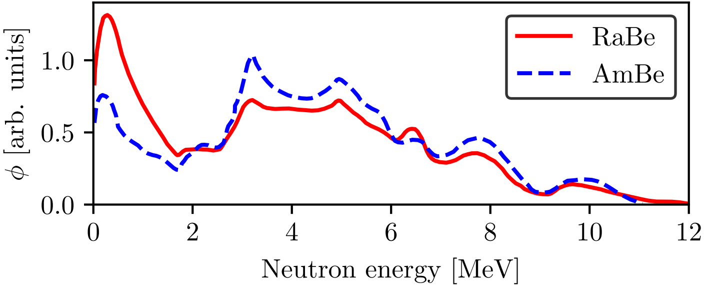
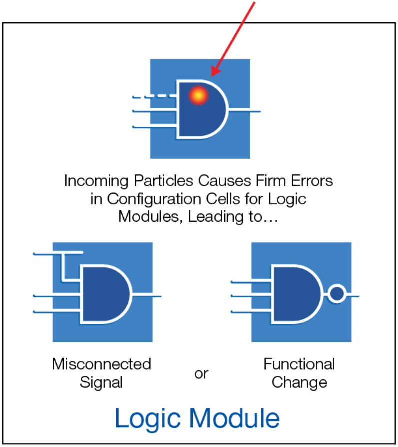
- Separate measurements using RaBe and AmBe neutron sources. **One** FPGA read out.

Low-energy neutron irradiation

- In December 2017 - January 2018 at Stockholm University.
- Separate measurements using RaBe and AmBe neutron sources. **One** FPGA read out.
- Total neutron fluence: $1 \cdot 10^{10}$ cm^{-2}.



Single Event Upsets (SEUs) in FPGAs



Figures from *Single Event Effects (SEE)*, Microsemi website.

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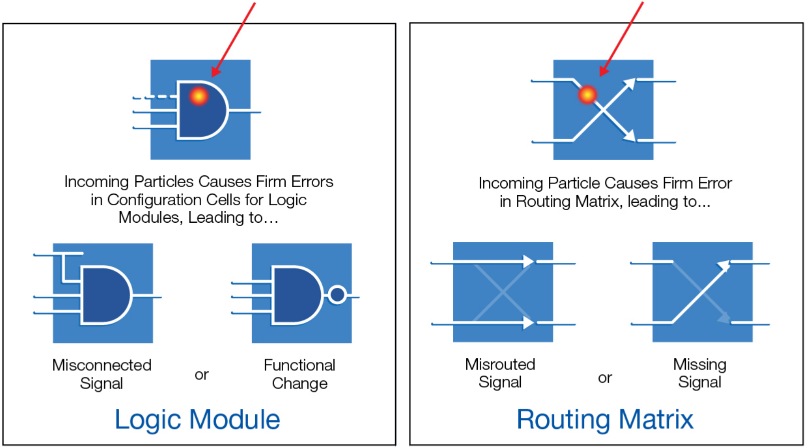

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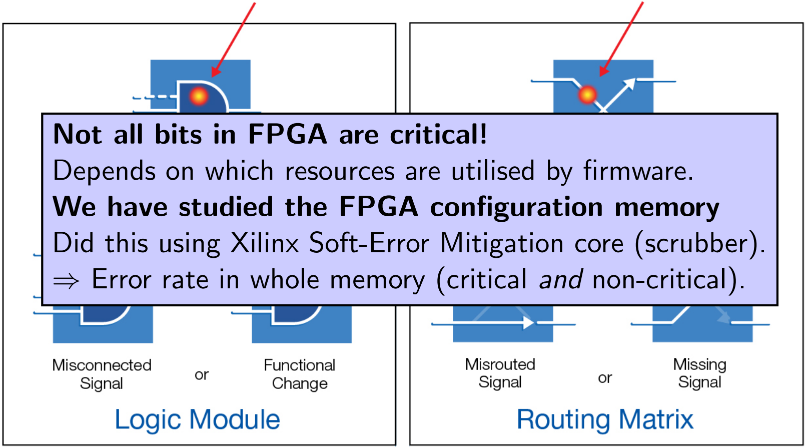

Not all bits in FPGA are critical!
Depends on which resources are utilised by firmware.
We have studied the FPGA configuration memory
Did this using Xilinx Soft-Error Mitigation core (scrubber).
$\Rightarrow$ Error rate in whole memory (critical *and* non-critical).

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Results

SEU cross section

The cross section (per bit) for an SEU in the FPGA is given by

$$\sigma_{\mathrm{SEU}} = \frac{N_{\mathrm{SEU}}}{\Phi_{\mathrm{n}} \cdot N_{\mathrm{bits}}}$$

Number of SEU

Particle fluence

Total number of bits

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Number of SEU (N_{SEU})

Particle fluence (Φ_{n})

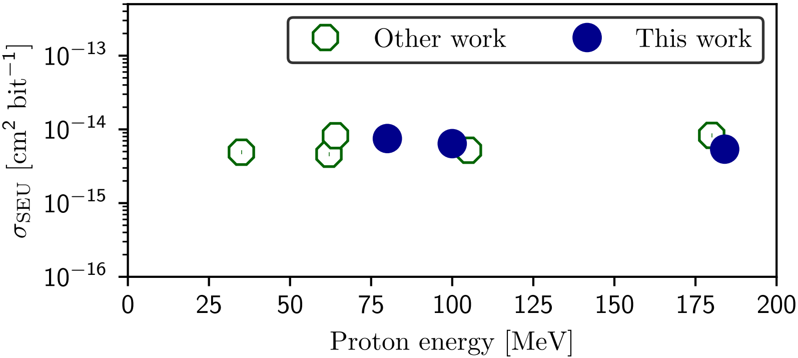
Total number of bits (N_{bits})

Once the cross section and particle flux are known,
the *SEU rate* and *mean time between upsets* may be determined.

Results

Proton irradiation

Good agreement with other measurements on Kintex-7:



Other work from for example ATLAS (LAr) and LHCb (RICH) groups.

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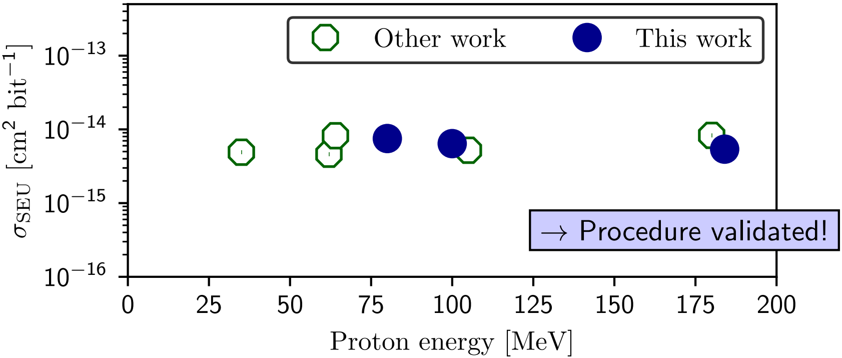

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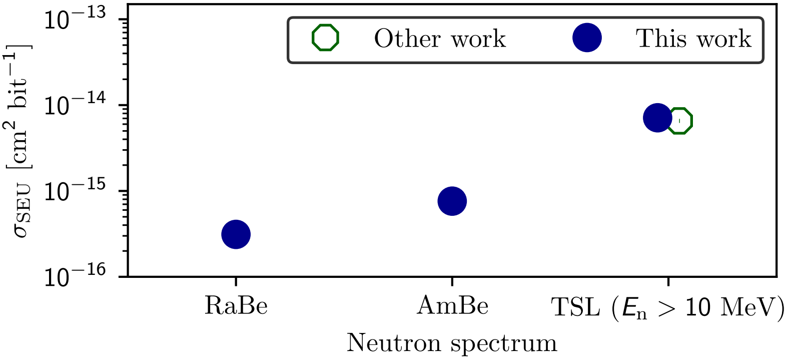
Results

Neutron irradiations

Good agreement with other measurement on Kintex-7:



Other work from ATLAS (LAr) group.

TSL cross section determined from neutron fluence above 10 MeV.

What does this mean for PANDA?

From neutron and proton irradiations
σ_{SEU} determined at specific energies.

Conditions during PANDA operation
Continuous energy spectrum of particles at front-end board location.
SEU rate = ?

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Needed:
Way to predict SEU rate in PANDA, using results from irradiations.

Conditions during PANDA operation
Continuous energy spectrum of particles at front-end board location.
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What does this mean for PANDA?

From neutron and proton irradiations
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Solution: Monte Carlo simulations
1) GEANT4-based model of energy deposits in microelectronics $\Rightarrow \sigma_{\mathsf{SEU}}(E)$
2) pandaROOT simulation $\Rightarrow \Phi(E)$

Conditions during PANDA operation
Continuous energy spectrum of particles at front-end board location.
SEU rate = ?

Developing the SEU model

- Model of energy deposition by protons and neutrons in a memory cell.
- Principle based on standard SEU-modelling tools — constructed to match Kintex-7 feature size.
- In the model, an SEU occurs if the energy deposition in the *sensitive volume* is larger than a *critical energy*.

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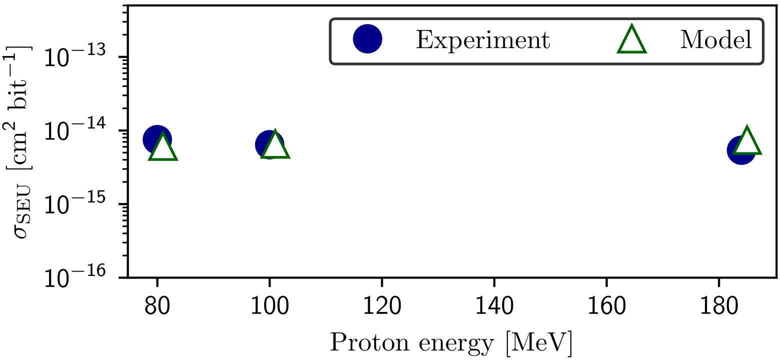
- In the model, an SEU occurs if the energy deposition in the *sensitive volume* is larger than a *critical energy*.
- The values of the model parameters were determined by fitting the model to our experimental data:
  - Simulate proton and neutron beams matching experiments.
  - Fit to all our data using a full likelihood fit.
- When this was done, the model was verified by comparing the resulting cross sections with the experimental data.

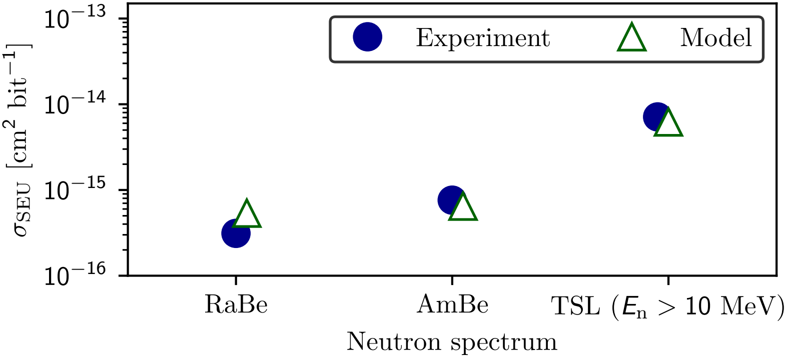
SEU model verification

Protons:



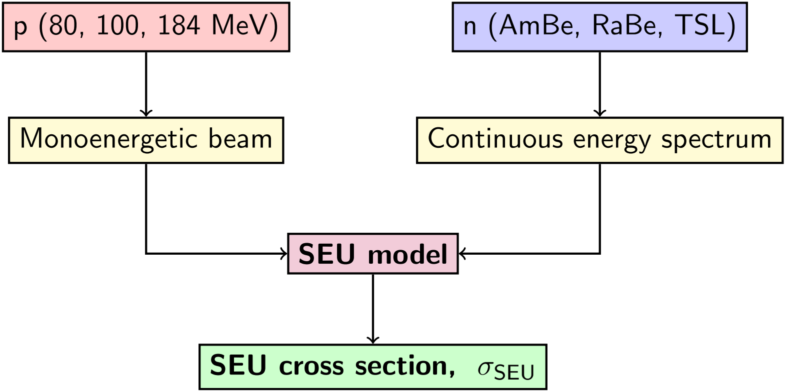
SEU model verification

Neutrons:



Model works for both protons and neutrons.

Using the SEU model



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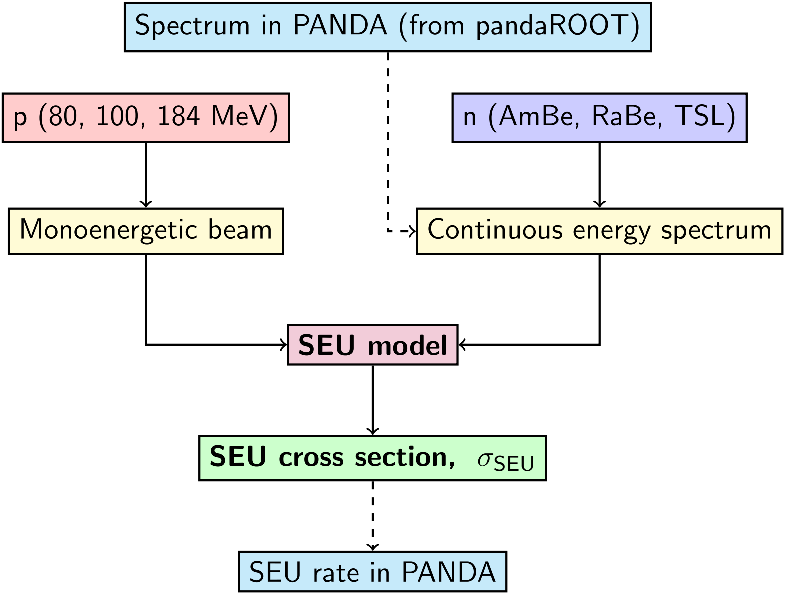

SEU rates in the Electromagnetic Calorimeter

- Simulations performed at antiproton momenta of 1.5, 5.2 and 8.9 GeV/c (to cover the entire phase-1 range) $\rightarrow$ neutron flux at **forward endcap** digitisers.
- All three resulting spectra used as input to the SEU model $\rightarrow$ SEU rates (assuming $\mathcal{L} = 1 \cdot 10^{31}$ cm^{-2} s^{-1}).

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- $p_{\mathrm{pbar}} = 8.9$ GeV/c, $\mathcal{L} = 1 \cdot 10^{31}$ cm^{-2} s^{-1} $\Rightarrow$
  - ϕ_{n} at position of digitisers is ~300 cm^{-2} s^{-1}.
  - MTBU due to neutrons (per FPGA):
    - Any type of SEU: 18 hours.
    - SEUs not correctable by SEM: 180 hours ($\sim$ 10% of all errors).

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- **These values include a safety factor of 10 relative to the results predicted by the model.**

Outlook: Error-mitigation?

- At PANDA startup, triple modular redundancy is probably not necessary when it comes to the FPGA configuration.
- Xilinx SEM protects the configuration (by scrubbing), and can be used in *enhanced* mode — repairs some multi-bit upsets as well $\rightarrow$ decreases uncorrectable-error rate from $\sim 10\% \rightarrow \sim 2\%$ (takes up more resources). Full protection: store copy of bitstream which can replace damaged one.

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- Protection for other parts of the FPGA (like Block Memory) has to be incorporated in design.
- At higher luminosities, TMR might be needed.
- In any case, watch-dog mechanisms have to be included in FPGA design.
- All this should be taken into account when designing the final firmware (mitigation approach depends on which resources are used). $\Rightarrow$ Topic for further discussion.

Thank you!

Extra slide: σ_{SEU} energy dependence