

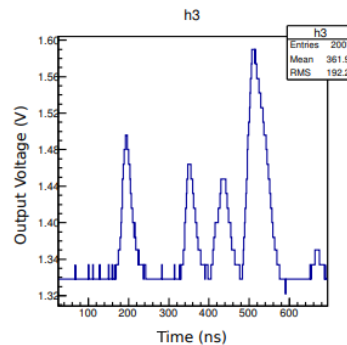
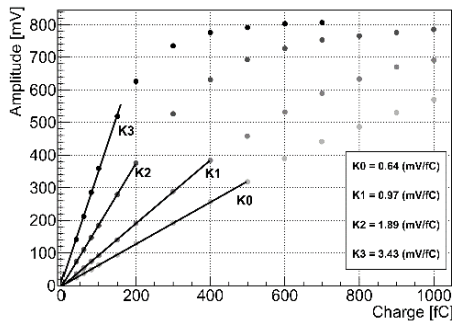
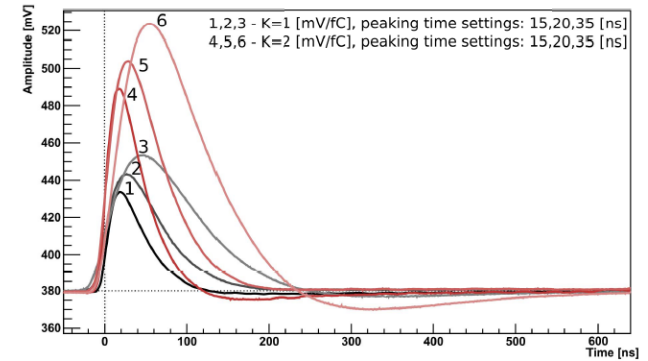
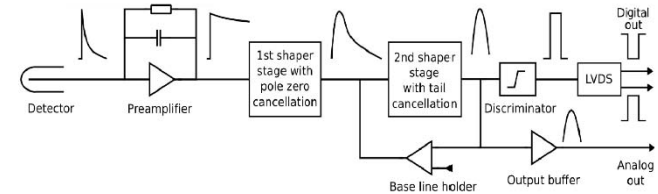
# PASTTREC Status Update

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PANDA DAQ/FEE Workshop 2018

# PASTTREC ASIC

- 8 input channels
- Preamplifier, baseline holder, tail cancellation, discriminator
- Highly configurable
- One common discrimination threshold
- Individual baselines tuning
- 150 ps time resolution (ASIC + FEE + TDC)
- High-rates capabilities



Register <sup>channel</sup> <sub>bits</sub>	Setting	Values
K <sub>1:0</sub>	Gain	4, 2, 1, 0.67 mV/fC
Tp <sub>1:0</sub>	Peaking time	10, 15, 20, 35 ns
TC1C <sub>2:0</sub>	1 <sup>st</sup> stage tail cancellation constant capacitance	6 - 16.5 pF step 1.5 pF
TC1R <sub>2:0</sub>	1 <sup>st</sup> stage tail cancellation constant resistance	3 - 31 kΩ, step 4 kΩ
TC2C <sub>2:0</sub>	2 <sup>nd</sup> stage tail cancellation constant capacitance	0.6 - 1.65 pF, step 0.15 pF
TC2R <sub>2:0</sub>	2 <sup>nd</sup> stage tail cancellation constant resistance	5 - 26 kΩ, step 3 kΩ
Vth <sub>6:0</sub>	Common discrimination threshold	0 - 254 mV, step 2 mV
B <sub>1:0</sub> <sup>4:0</sup>	Baseline fine tuning	0 - 62 mV, step 2 mV
Ch <sub>2:0</sub> <sup>en</sup>	Channel input enable	0 - 7
LVDS <sub>2:0</sub> <sup>en</sup>	Channel LVDS output enable	0 - 7

# PASTTREC FEE

- 16 input channels
  - 2x ASICs
  - Test inputs
  - Digital output connector
    - Discriminated signals to TRB/TDC
    - Registers settings by SPI from TRB
  - Analog outputs
  - +6/-6 V
- 
- Evaluated multiple times under beams with FT and STT prototypes

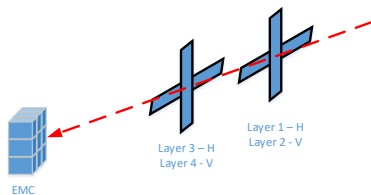


# PASSTREC FEE v2

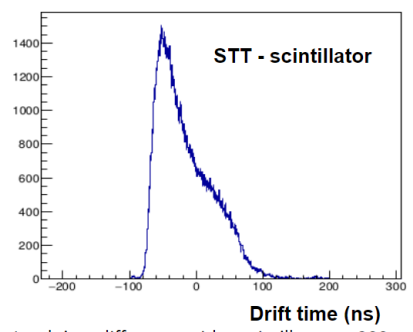
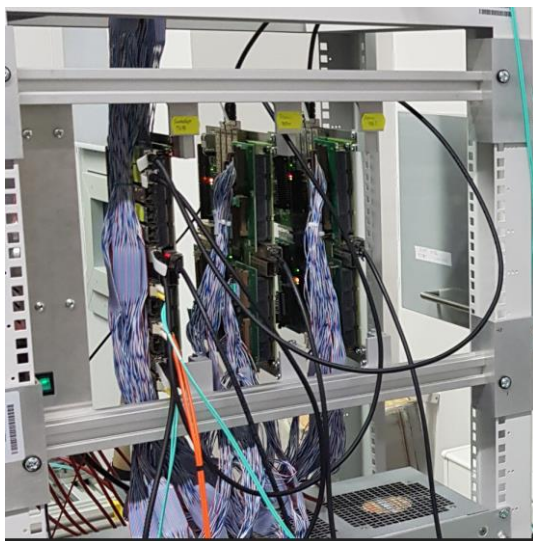
- Analog output removed
- Reduction of size, power consumption, heat
- +5V only



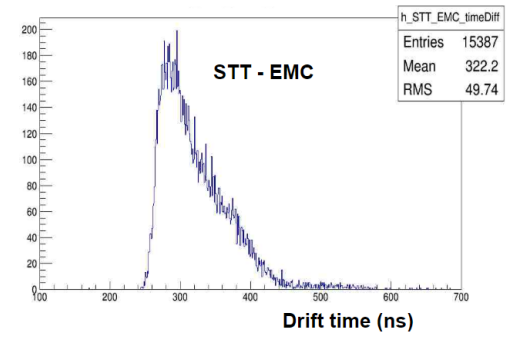
# Last tests



- FT – EMC joint tests
  - 2 TRBs as FEE readout
  - 1 TRB for SODANet synchronization
- Stable operation over couple of weeks
- Analysis and tracking in progress



Lead time difference with a scintillator - ~200 ns  
*Pawel Strzempek-2017*



Cut on time window – (220 – 450) ns