Readout and DAQ interfaces

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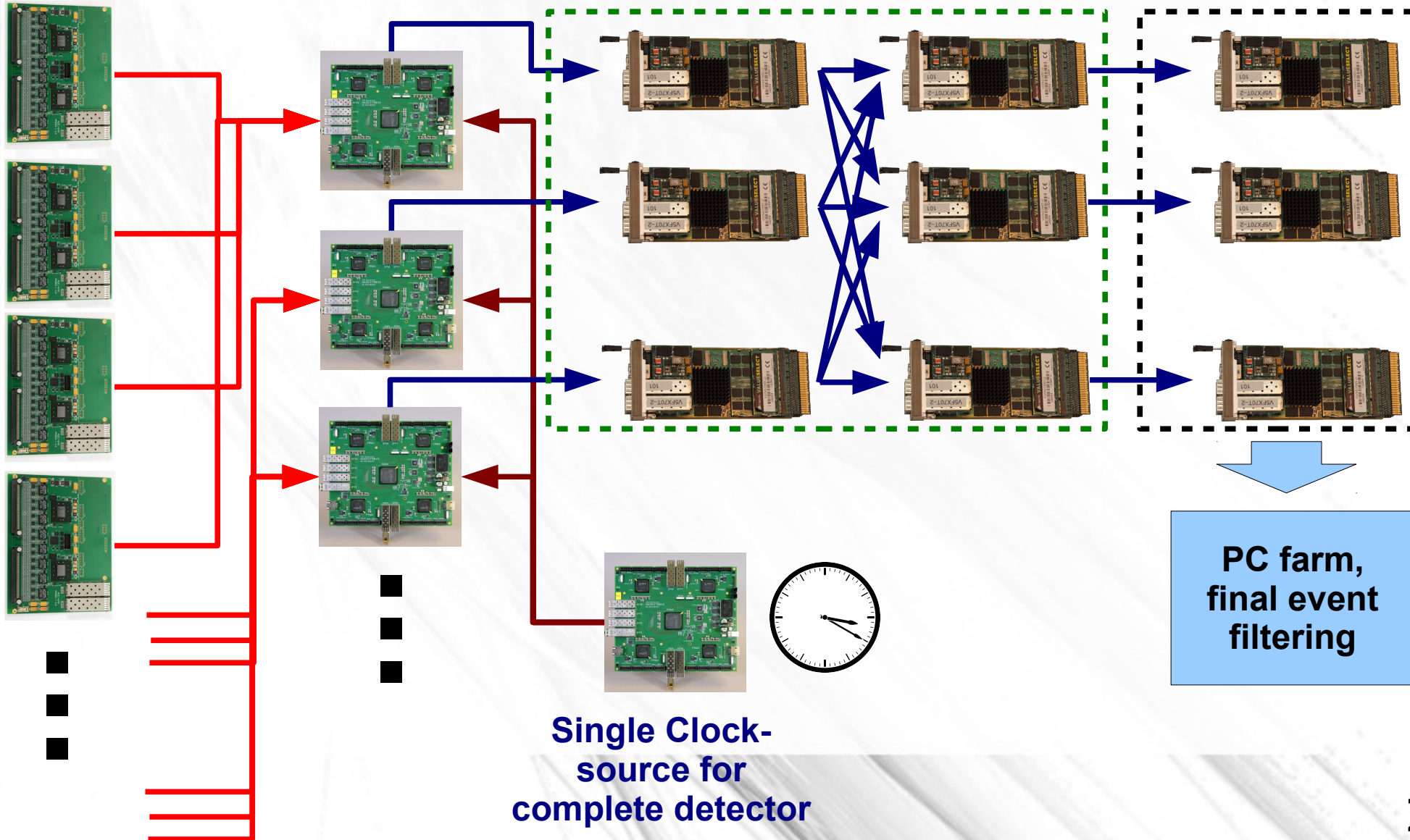
for the PANDA collaboration

Push-Only Readout

Intelligent front-end (Digitizers)

Intelligent front-end (Concentrators)

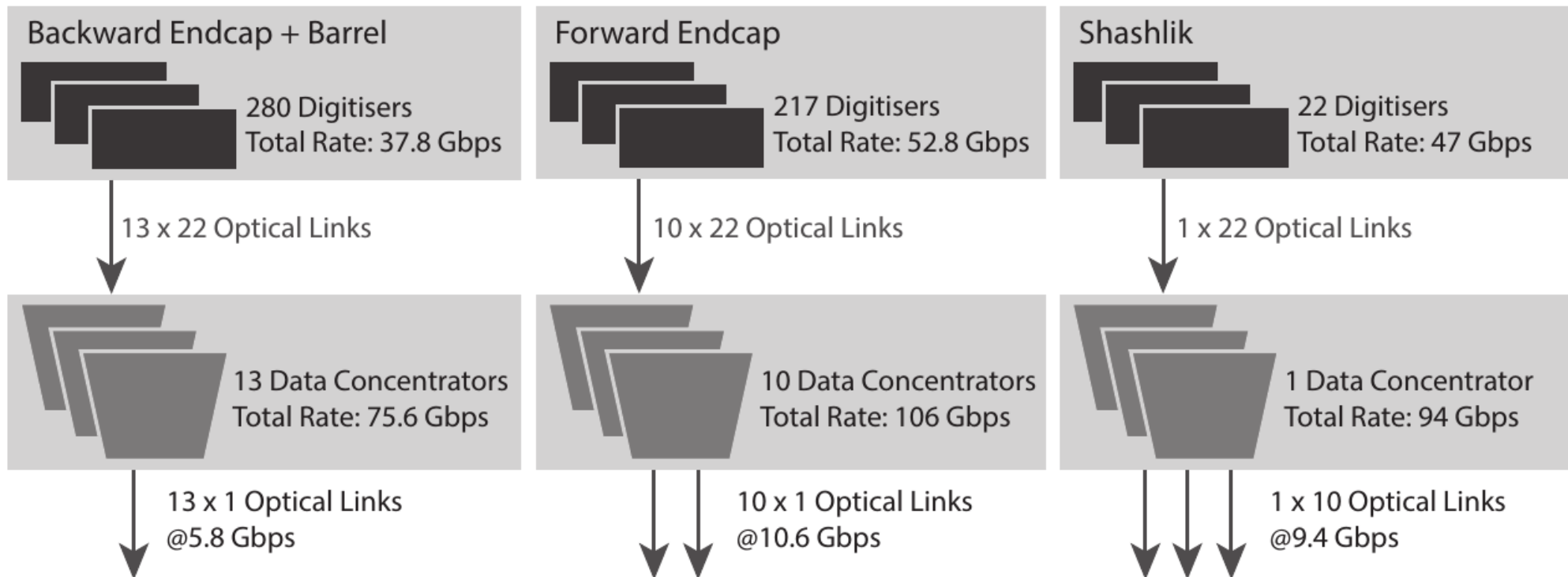**Event-building network with data pre-processing (Concentrators/compute nodes)**

Physics-event reconstruction, filtering

Analogue front-end

Single Clock-source for complete detector

PC farm, final event filtering

EMC data-flow

Worst-case scenario
(20 MHz annihilation rate, mainly single-hit clusters)

Assumption:
- EMC DC has 16 optical fibres
- Available resources: Kintex 7 ultrascale

EMC Burst-building network

Barrel + Backward Endcap | + Forward Endcap | + Shashlik

L1   13 ▶ 75.6 Gb   10 ◀ <75.6 Gb

L1   10 ▶ 106 Gb   10 ◀ <106 Gb   10 ▶ 94 Gb   10 ◀ <94 Gb   L1

Network Node L2   ... x10

Send to CN by superburst
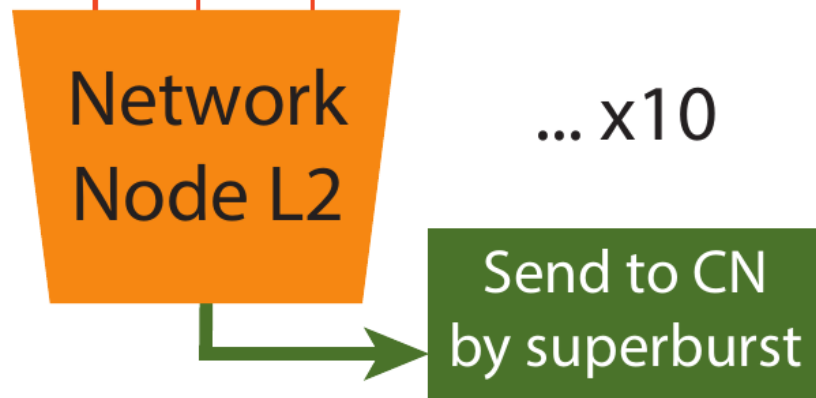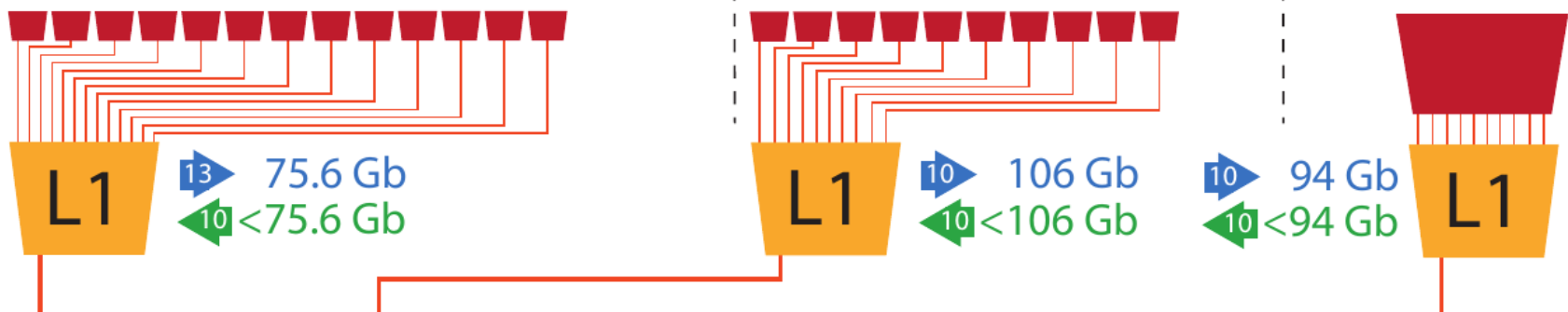
LEGEND:
- **n** ▶ Data in
- **n** ◀ Data out
- EMC DC
- **L1** Network Node L1
- Optical fibre

Push-Only Readout

Event-building network with data pre-processing
(**Concentrators**/**compute nodes**)

Physics-event reconstruction, filtering

SODANET
- **data transfer**
- **configuration**

Analogue front-end
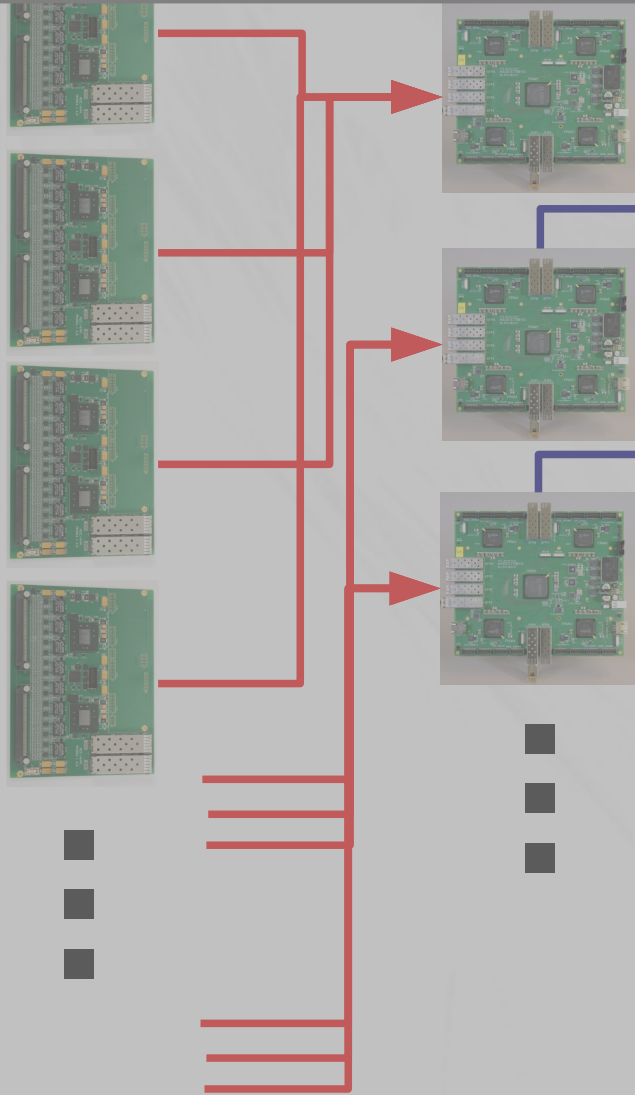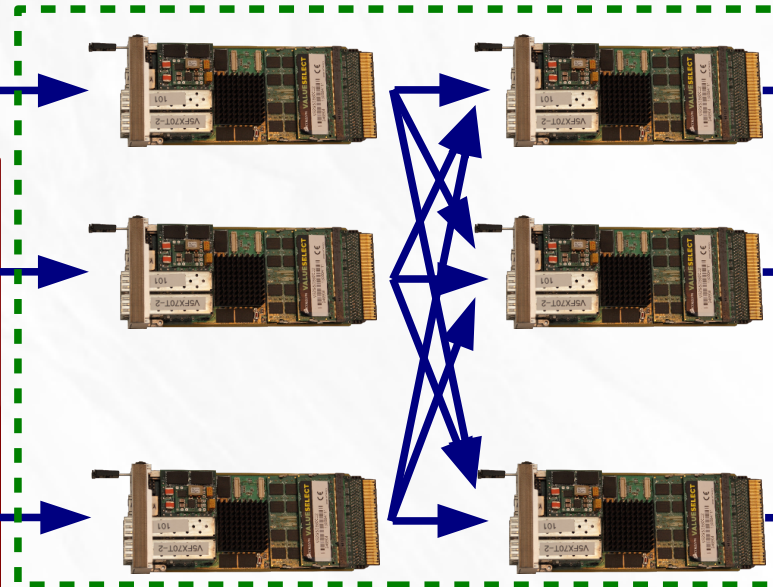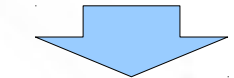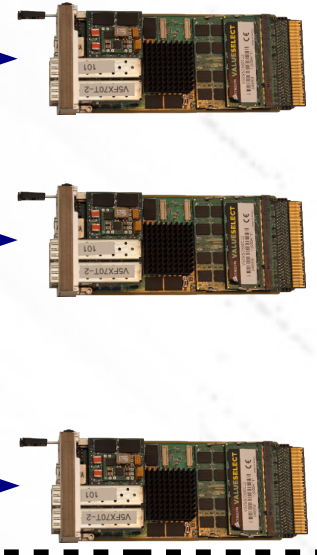
Single Clock-source for complete detector

PC farm, final event filtering

SODANET Topology
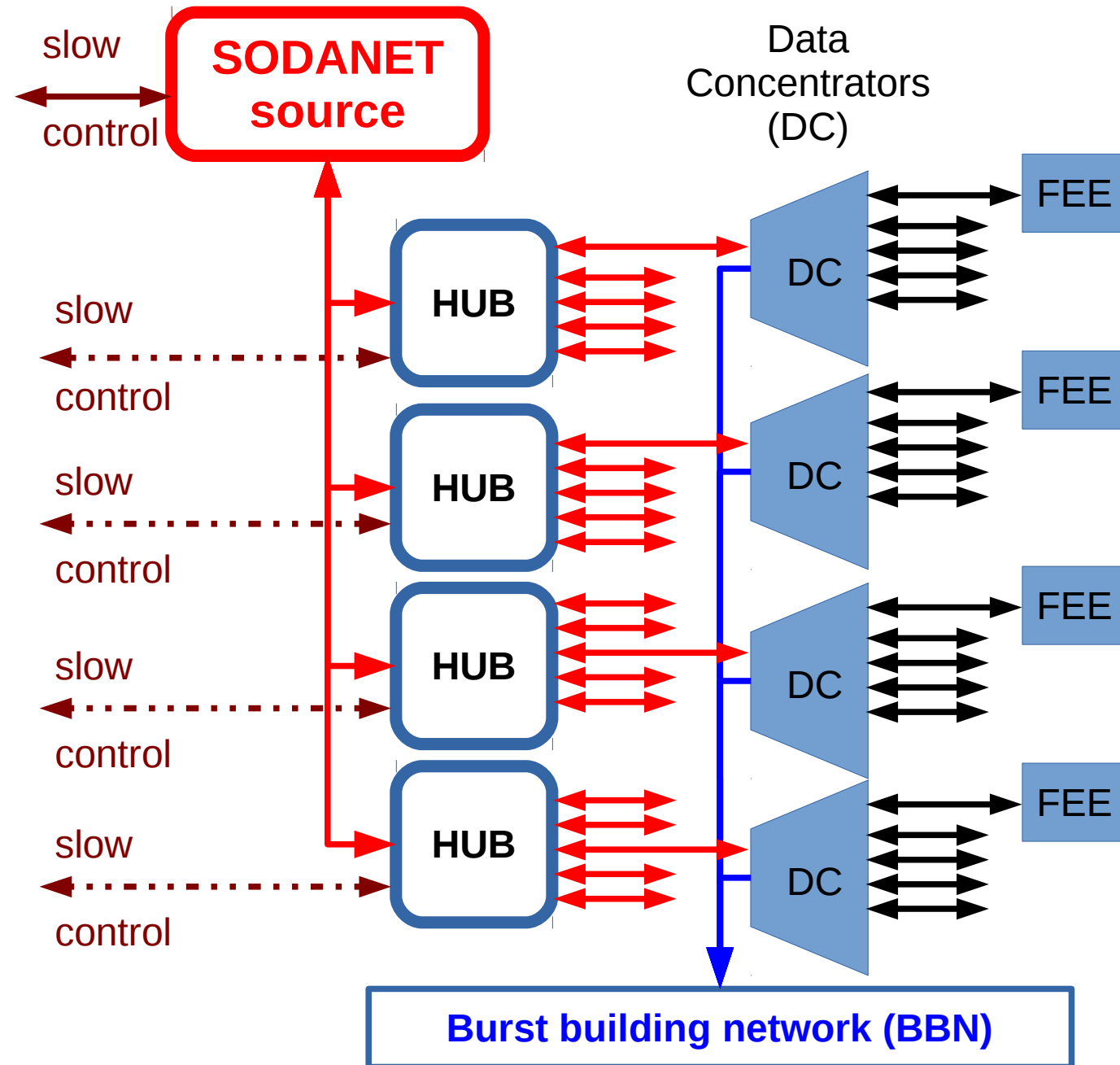
SODANET link:
- Bidirectional
- Synchronous (only in one direction)
- Transfer:
  - source → DC: synchronization information and FEE configuration
  - DC → source: slow control, used for time calibration

Data link (DC → BBN):
- Unidirectional

Link DC ↔ FEE:
- Bidirectional, synchronous
- Protocol up to subsystem

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DC Output Data-format

- DC can start transmitting FEE data once it is available
  (without waiting till the end of a super-burst)
- If no data are available –
  DC sends an empty package at the end of the Super-burst

Data-package

31 16	15 0
last-packet flag; packet number	data size in bytes
Not used (same as HADES)	Not used (same as HADES)
Status and error	System ID
Super-burst number	
Data	

All FEE modules should issue "empty packet" in case no data is measured – assures readout integrity

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Push-Only Readout

Intelligent front-end (**Digitizers**)

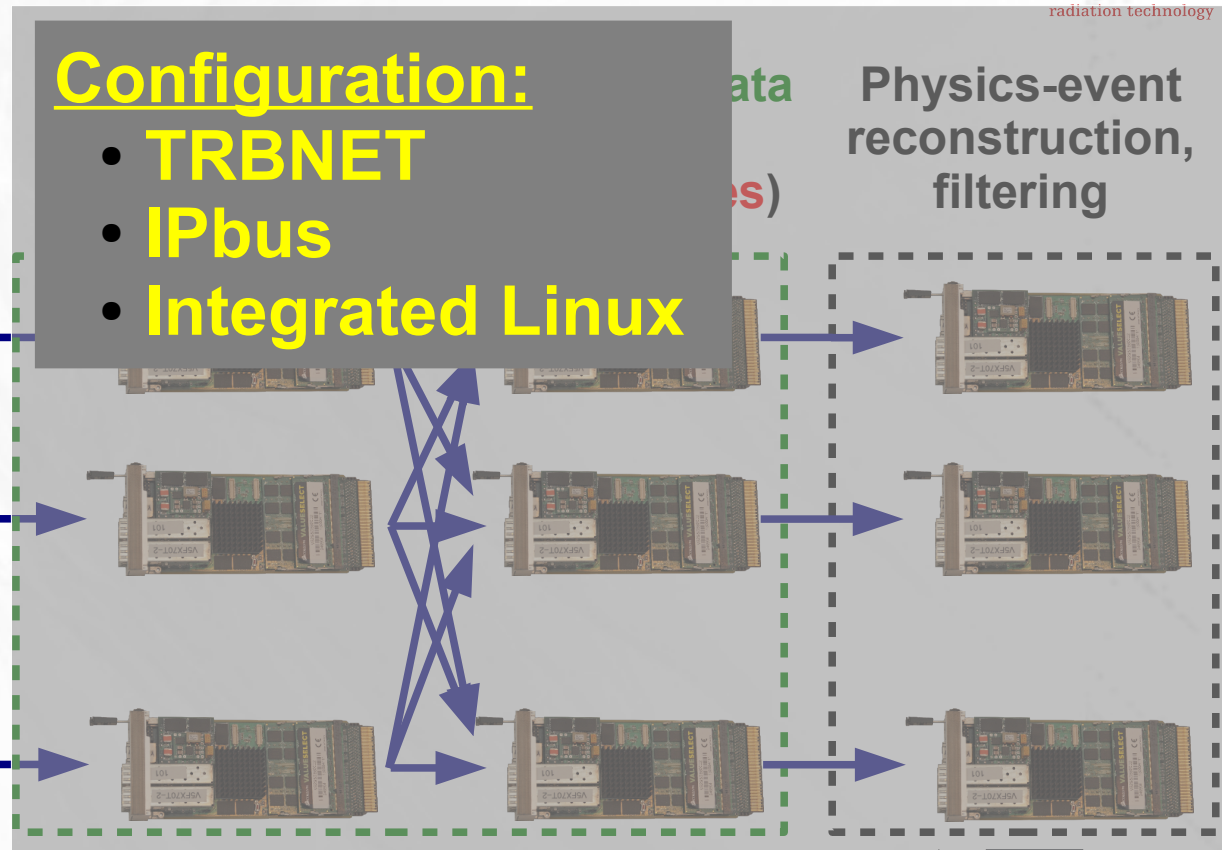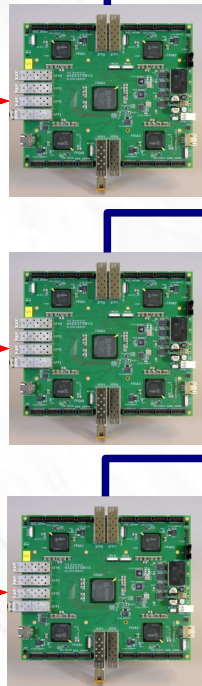Intelligent front-end (**Concentrators**)

Configuration:
- TRBNET
- IPbus
- Integrated Linux

Physics-event reconstruction, filtering

Analogue front-end

Single Clock-source for complete detector

PC farm, final event filtering

Extra slides on SODANET

SODANET Protocol

All data and clock are transferred using optical link (speed multiple to 40 MHz clock, e.g. 2 Gbs, 2.4 Gbs, 4.8 Gbs...):

- All SERializes-DE-Serializes (SerDeS) are working in synchronous mode: parallel clock has defined phase with respect to bit #1 of a serial clock

- Time-synchronization commands can interrupt low priority transmission of a slow-control package

- Synchronous commands are identified by the receiving side by special K-characters (FB)

- Synchronization commands are regular and define periods which are named **"Super-bursts"** (related to the timing of accelerator)

- TRBNET protocol [J. Michel, PhD thesis, University of Frankfurt, 2012] is used to transfer slow-control data and TRB v3 hardware is used for the development of the SODANET protocol

Timing with SODANET

Time of the SODA-signal propagation

Combined value: T_d

slow control

SODANET source

HUB

DC

FEE
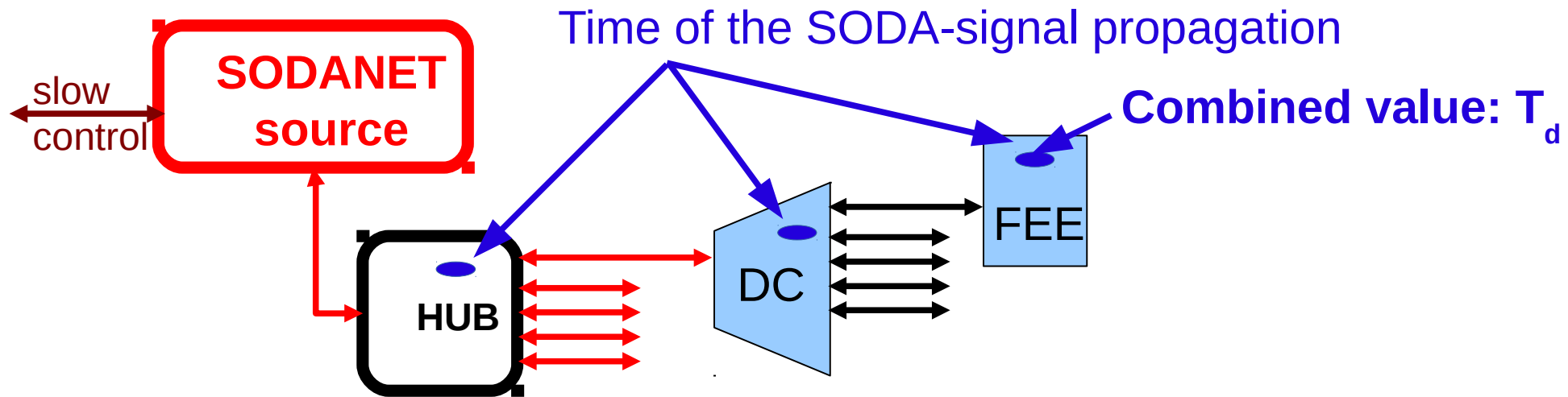
Protocol foresees **measurement of the propagation time (T_d)** of a synchronization command from the source to each FEE –
used to correct local timestamps:

- Each FEE module has own timing
- Local "time zero" is reset with each synchronization SODANET command "start of a super-burst"
- Each hit time-stamp is corrected with a T_d value
- After correction the time-stamp the hit data, including current super-burst number, are sent to DC module
- At the DC module decision is taken to which superburst the hit belongs
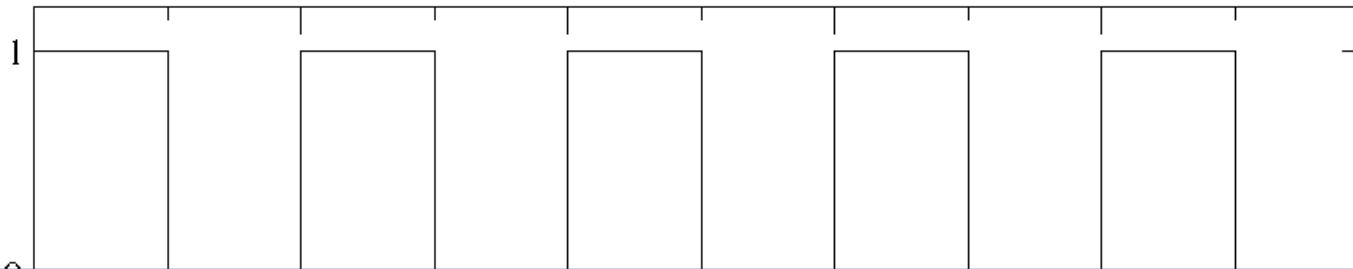
Synchronous Clocks

N * 25 ns (periods of 40 MHz clock)
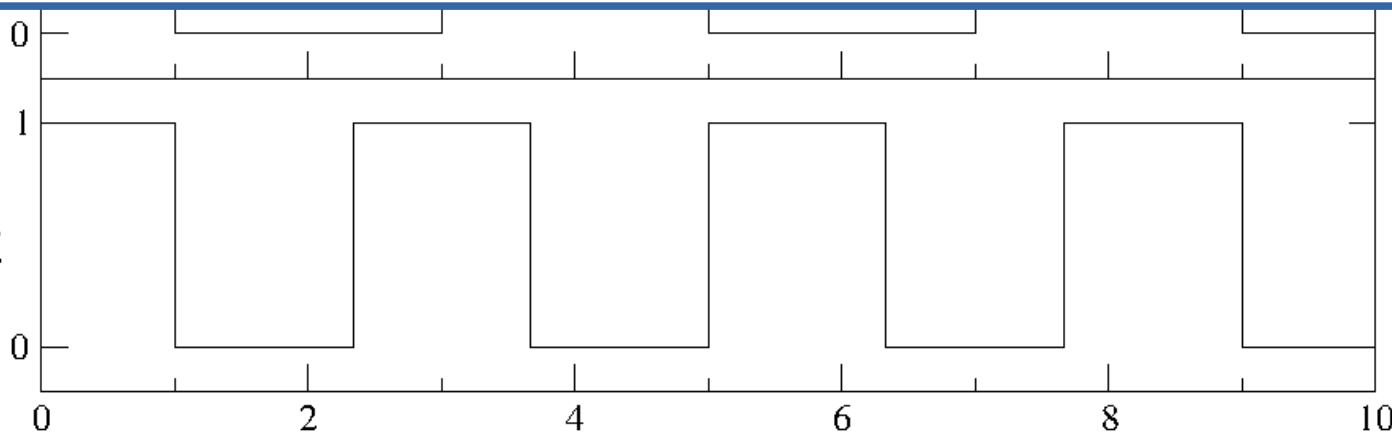
Start of superburst

Start of superburst

160 MHz

Synchronous clocks which can be derived:
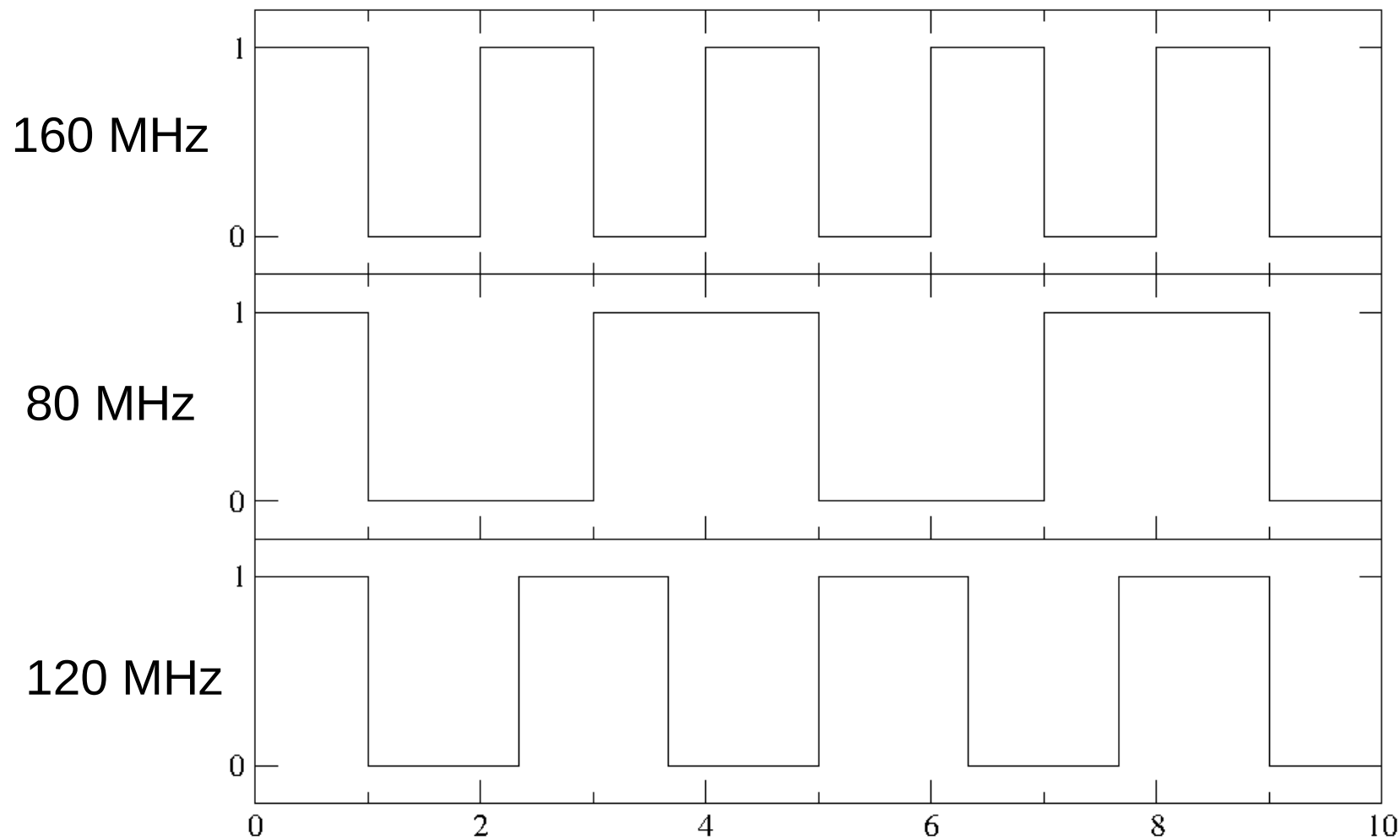- 40, 80, 120, 160, 200, 240 … MHz

120 MHz

Synchronous Clocks

N * 25 ns (periods of 40 MHz clock)

Start of superburst

Start of superburst

160 MHz

80 MHz

120 MHz

Start of a Super-burst

**Start of
superburst**

— — — — — — — — — — — — — — — — — —   **SODANET clock**

**Accelerator
cycle**
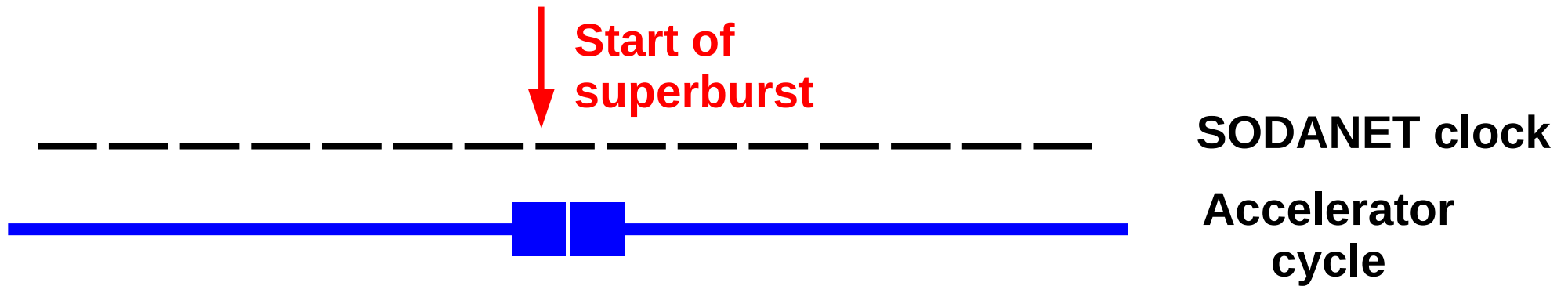
Accuracy of the super-burst start:
- **40 MHz clock: 25.00 ns**

Super-burst signals will not be periodic:
➔ most of the super-bursts have the same length
➔ once in several cycles a "correction" (shorter/longer by one cycle)
super-burst will be issued
➔ In general, global timing is not required

"Triggered" Mode Compatibility mode of operation

- External "trigger" signal is feed to one of the TDC/ADC

- "trigger" is timestamped, and sent
  to the burst-building network

- Event builder will select only hits with timestamps, which are in coincidence with the "trigger" signal
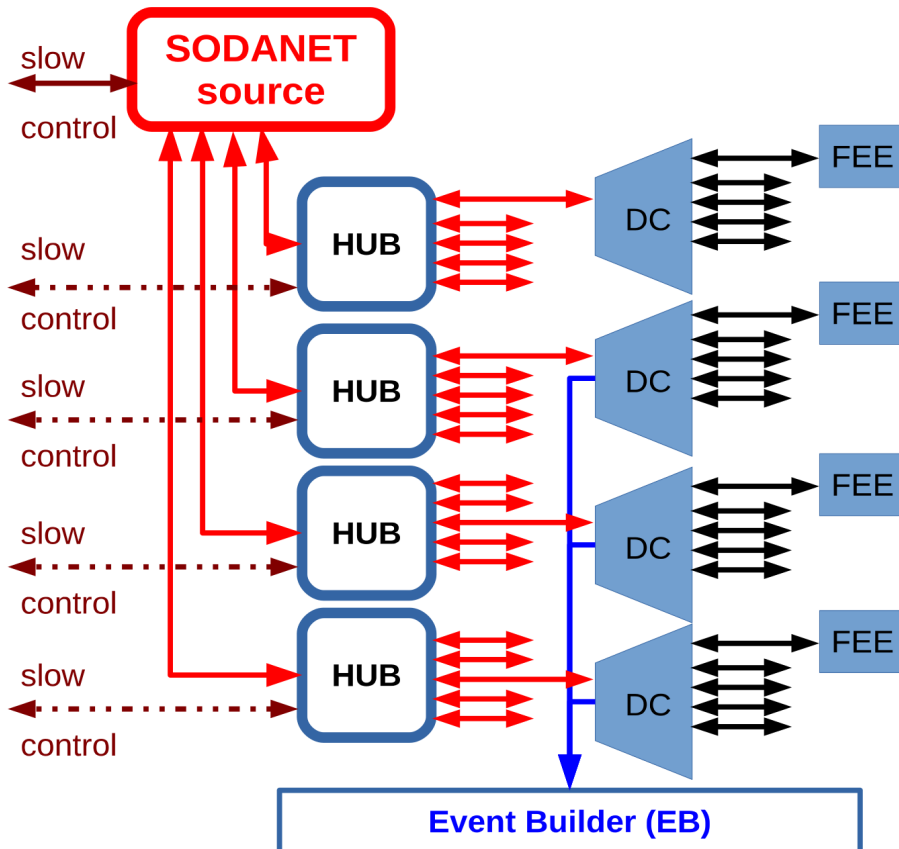
The SODANET

Implementation

The SODANET protocol implemented on several FPGA platforms (available VHDL code):

- Lattice ECP3
- Xilinx Kintex 7
- Xilinx Virtex 6

Jitter-cleaner (zero-delay) is mandatory for Xilinx architecture!
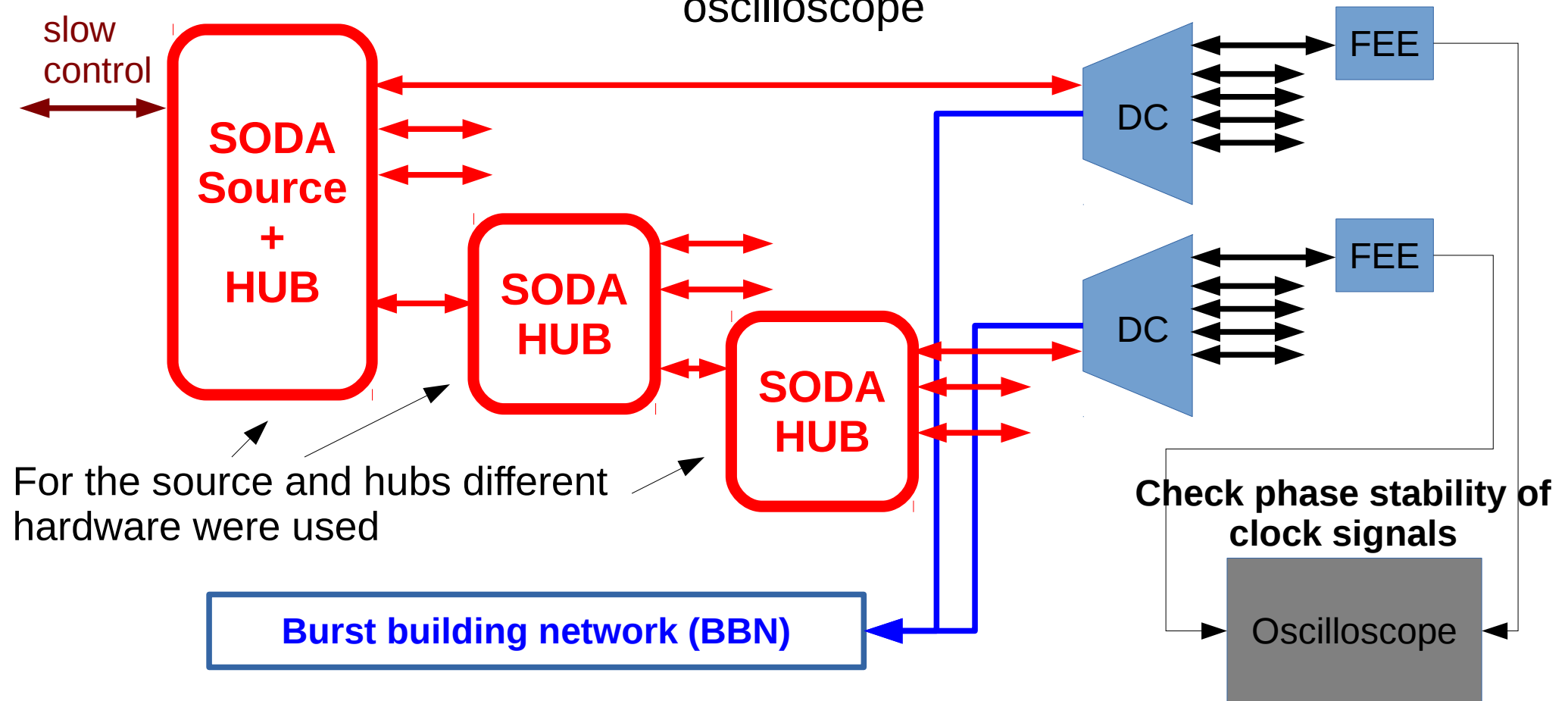
Verification

- Stability of the clock phase after reset/power cycle of the optical link

- Synchronisation of several FEE modules (using "SB start" command)

- Long-term stability of the system

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SODANET Test System
Clocking

During test relevant SODANET links were randomly disconnected and after recovery of the system stability of the clock-signal phase was checked with oscilloscope

slow control

SODA Source + HUB

SODA HUB

SODA HUB

DC

FEE

DC

FEE

Check phase stability of clock signals

Oscilloscope

For the source and hubs different hardware were used

Burst building network (BBN)

Systems with up to three levels of SODANET hubs did not show any instability

SODANET Test System
Synchronisation

Signal from one pulse generator was measured by two different front-ends.

During measurement FEE modules were reset to test synchronisation procedure
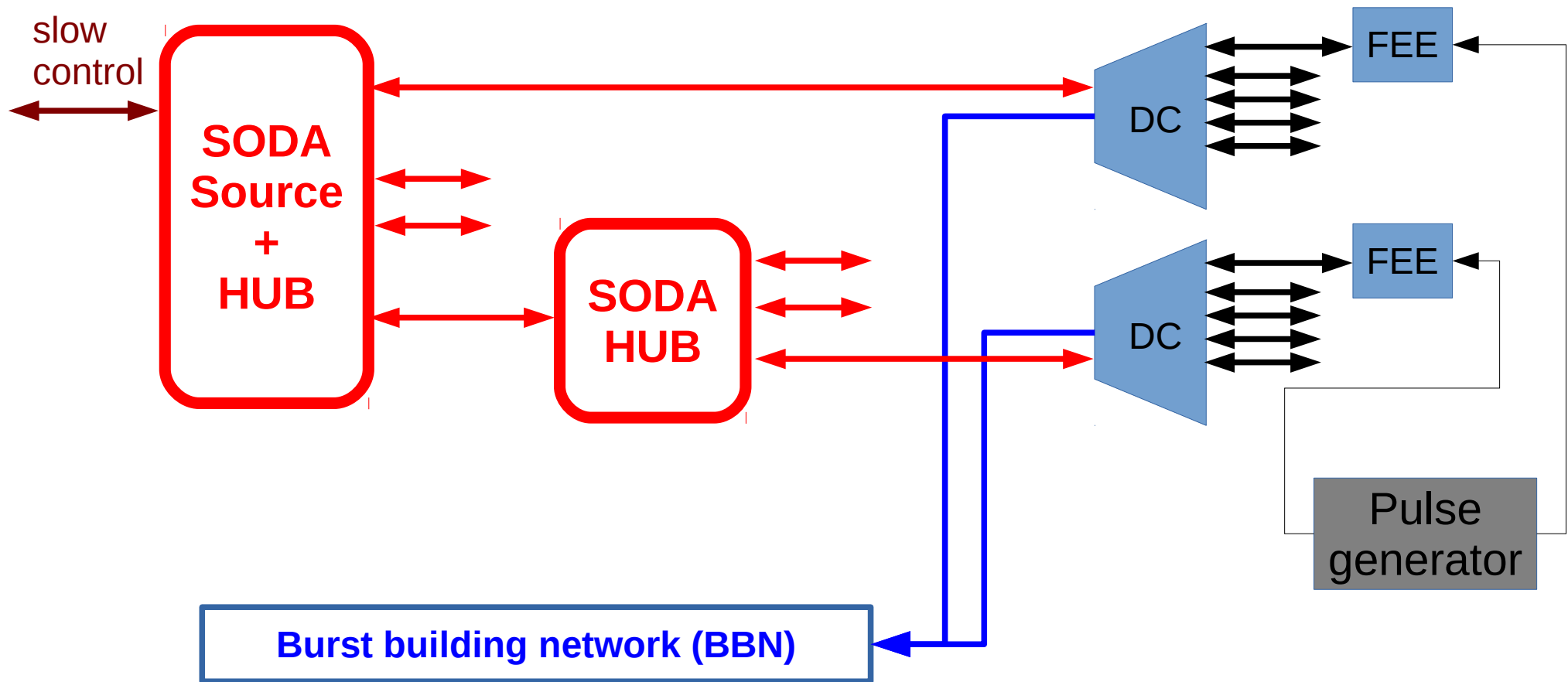
Time-stamps of measured pulses were compared:

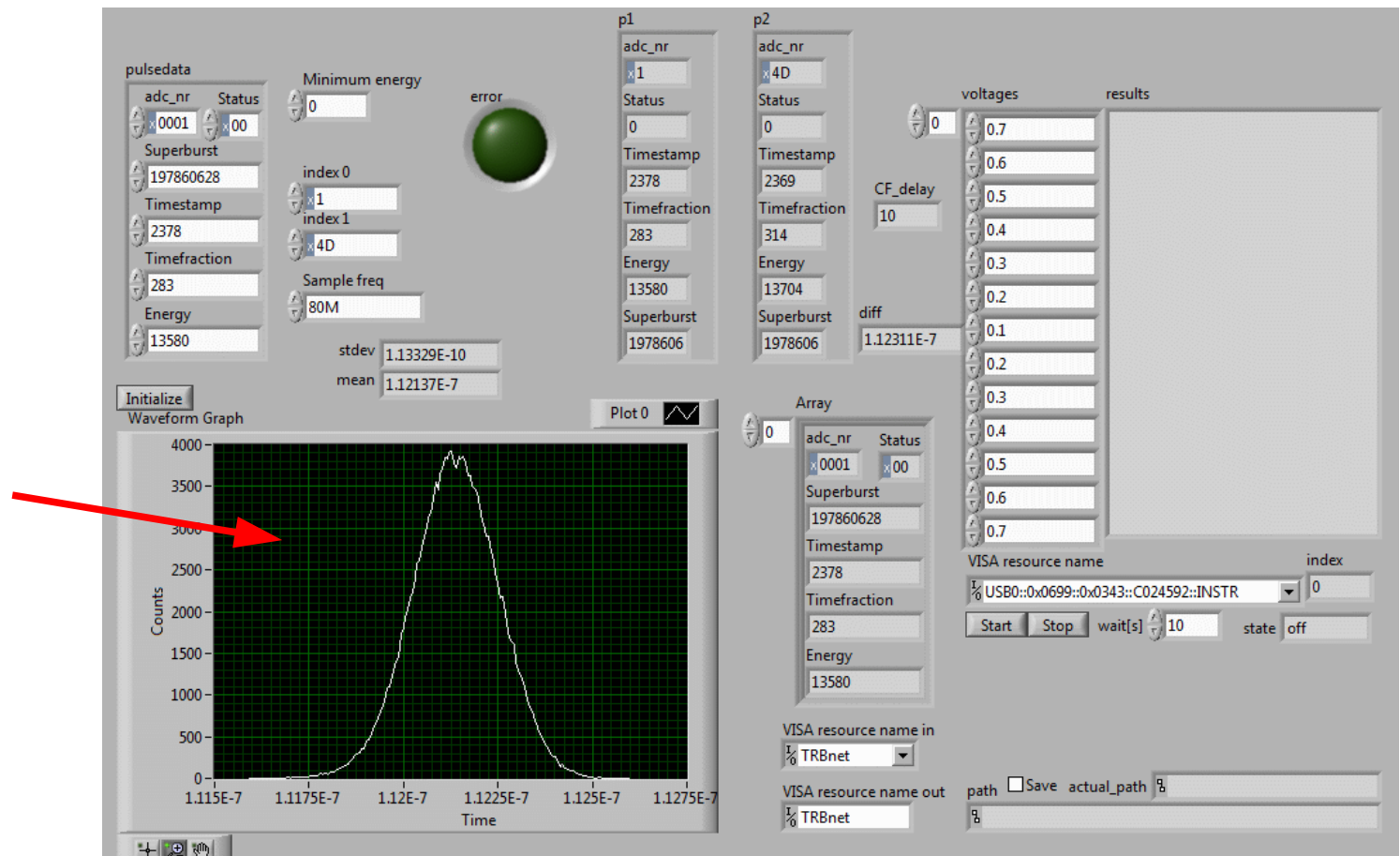**time difference should be constant**

SODANET Test System
Synchronisation

Signal from one pulse generator was measured by two different front-ends.

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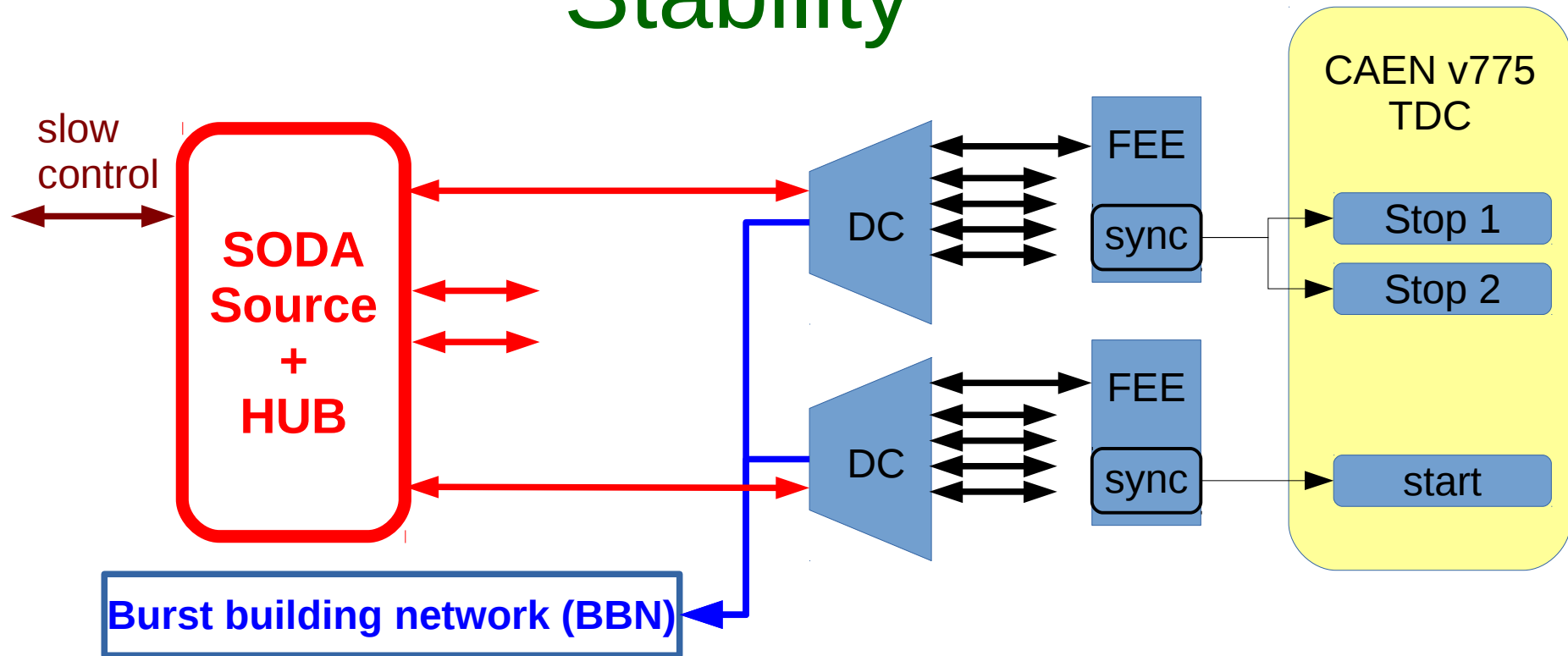Measured time-difference between detected pulses

Measured time difference is constant →

synchronisation is working properly
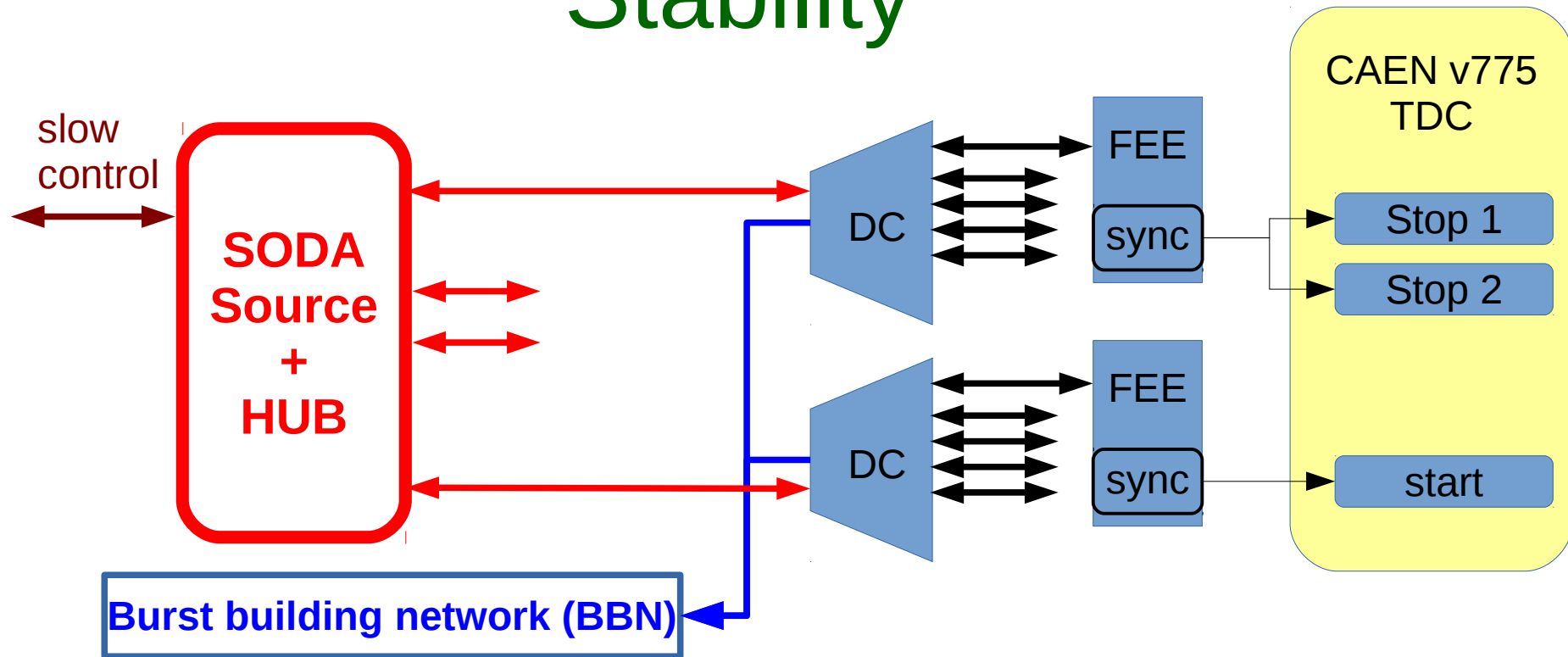
SODANET Test System
Stability

Measurements:

- Time-data were recorded with the rate of 100 Hz – 2 kHz (depending on the duration of the experiment)

- Data were accumulated for ~ 1 min (one measurement)

- For each measurement histograms of accumulated data were analysed
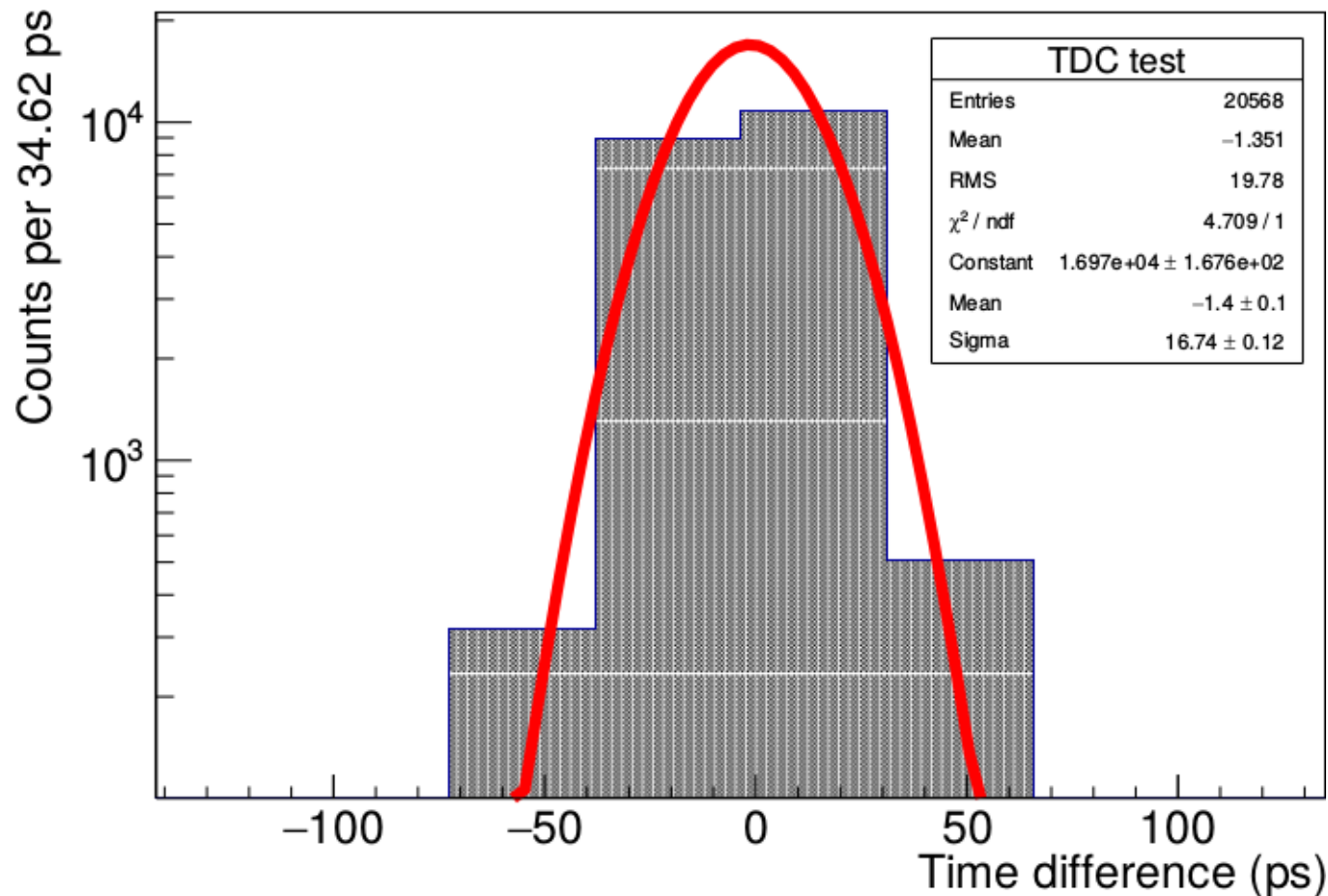
SODANET Test System
Stability

Measured quantities:

- $\Delta T = T_1$ (time difference between receives "SB start" signals): *stability of the SODANET system*

- $T_{TDC} = T_1 - T_2$: *stability of the TDC*
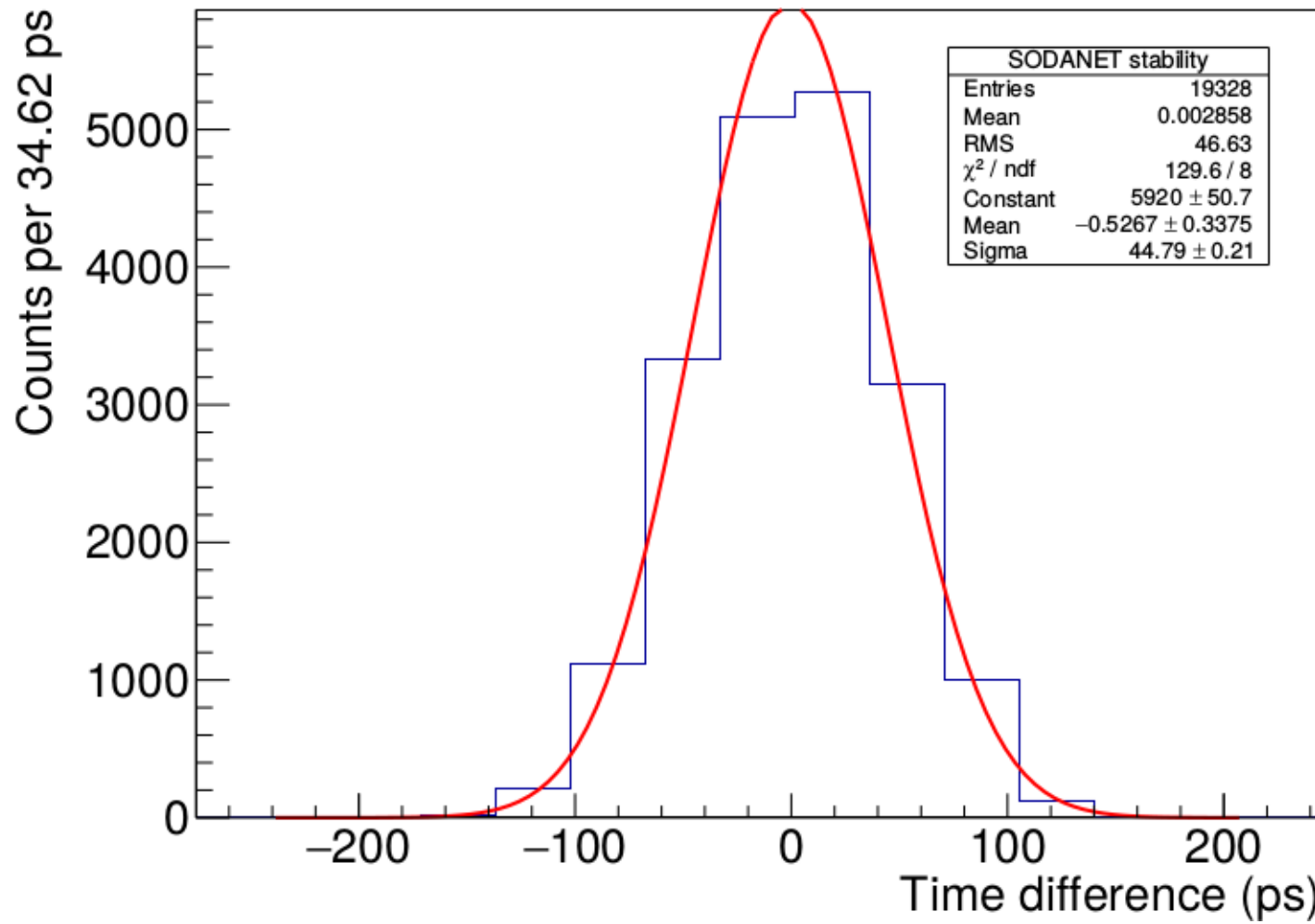
Measurements Precision

T_1-T_2
(difference between the same signal)

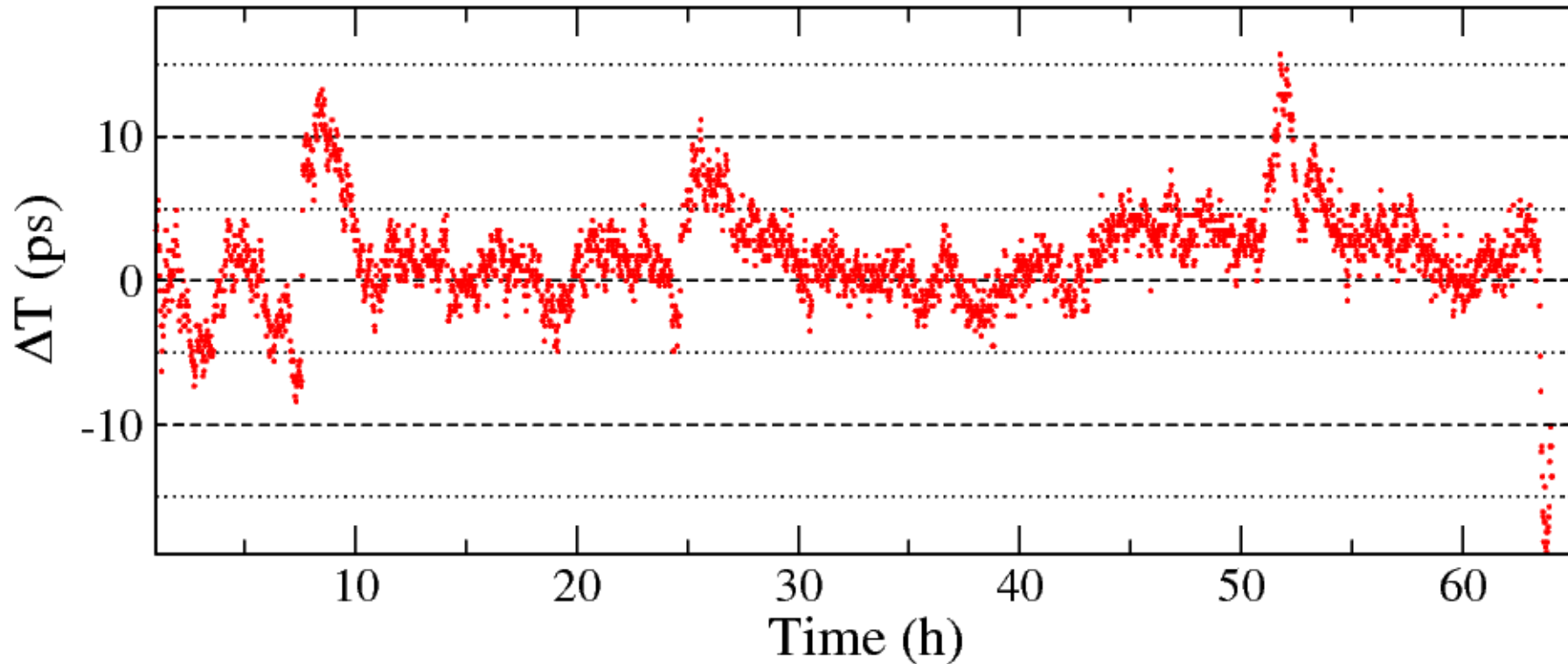
Jitter due to the TDC instability ~ 17 ps (standard deviation)

Jitter on SODANET

Typical T1 measurement
(time difference between recovered "SB start" signals)

SODANET stability	
Entries	19328
Mean	0.002858
RMS	46.63
χ^2 / ndf	129.6 / 8
Constant	5920 ± 50.7
Mean	-0.5267 ± 0.3375
Sigma	44.79 ± 0.21

Jitter of recovered "SB start" ~ $\sqrt{((47^2-17^2)/2)}$ = 29 ps
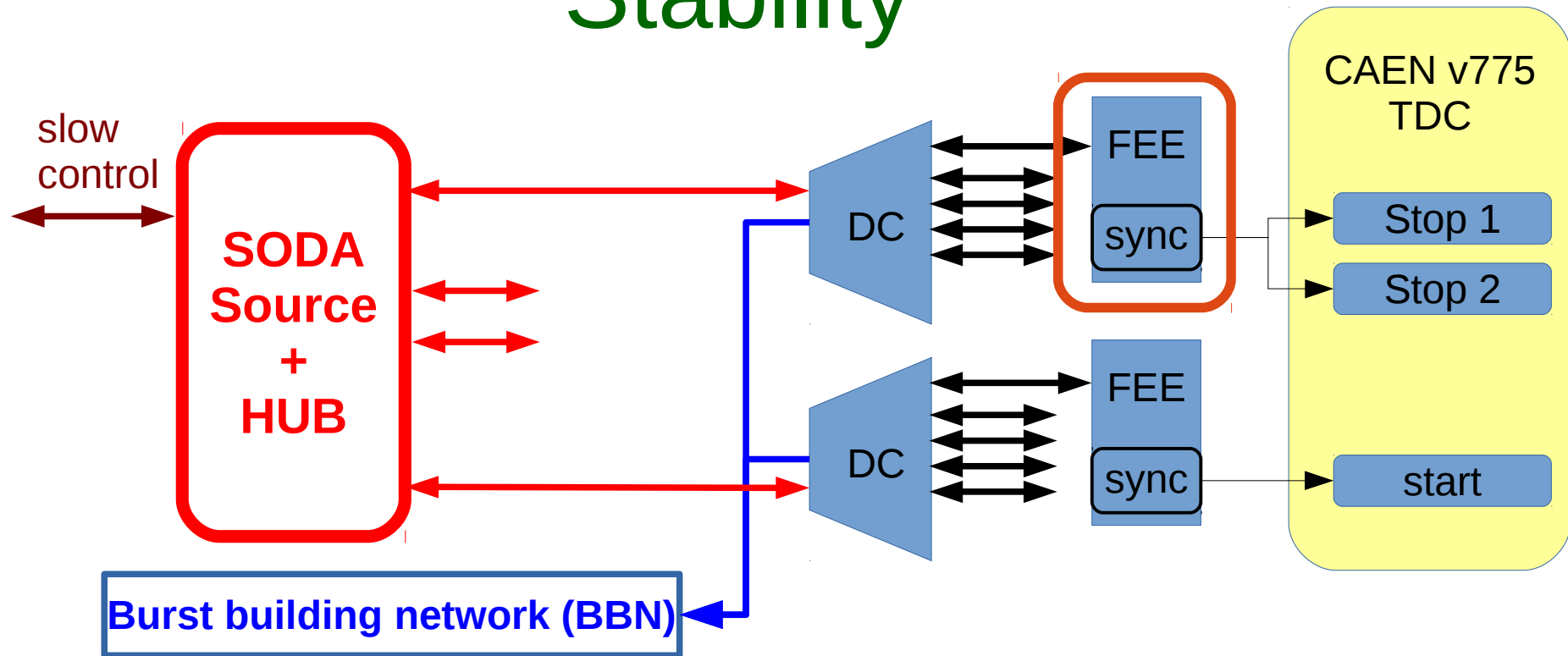
Synchronization Stability

Most of the jumps in ΔT could be correlated to changes of the room temperature

Once the system is warmed-up it is stable within 30 ps:
sufficient for the most of the PANDA subsystems.
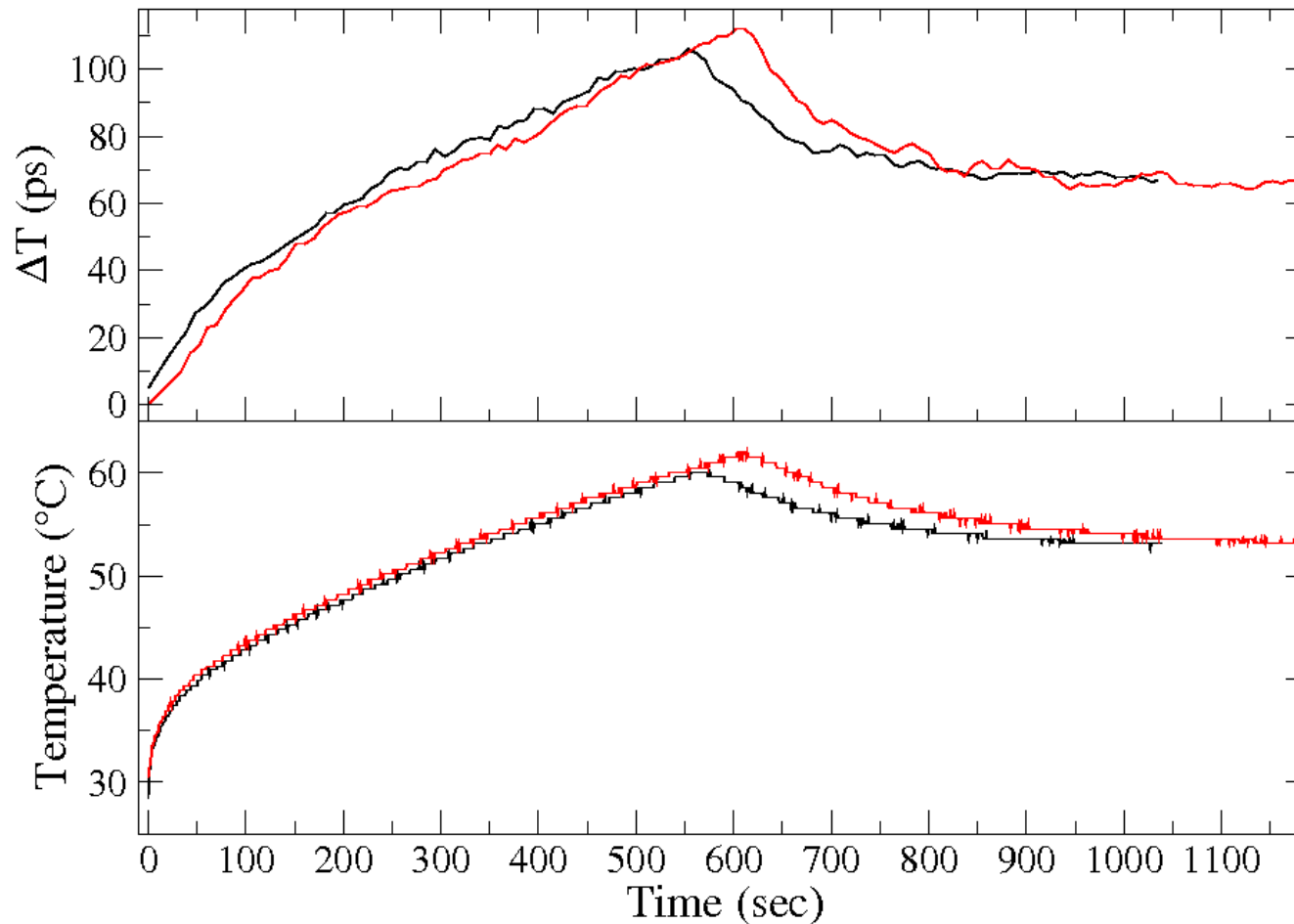
SODANET Test System
Stability

Measurements:

- At the beginning of the measurement one FEE unit was cooled to the room temperature while all other components were warmed-up
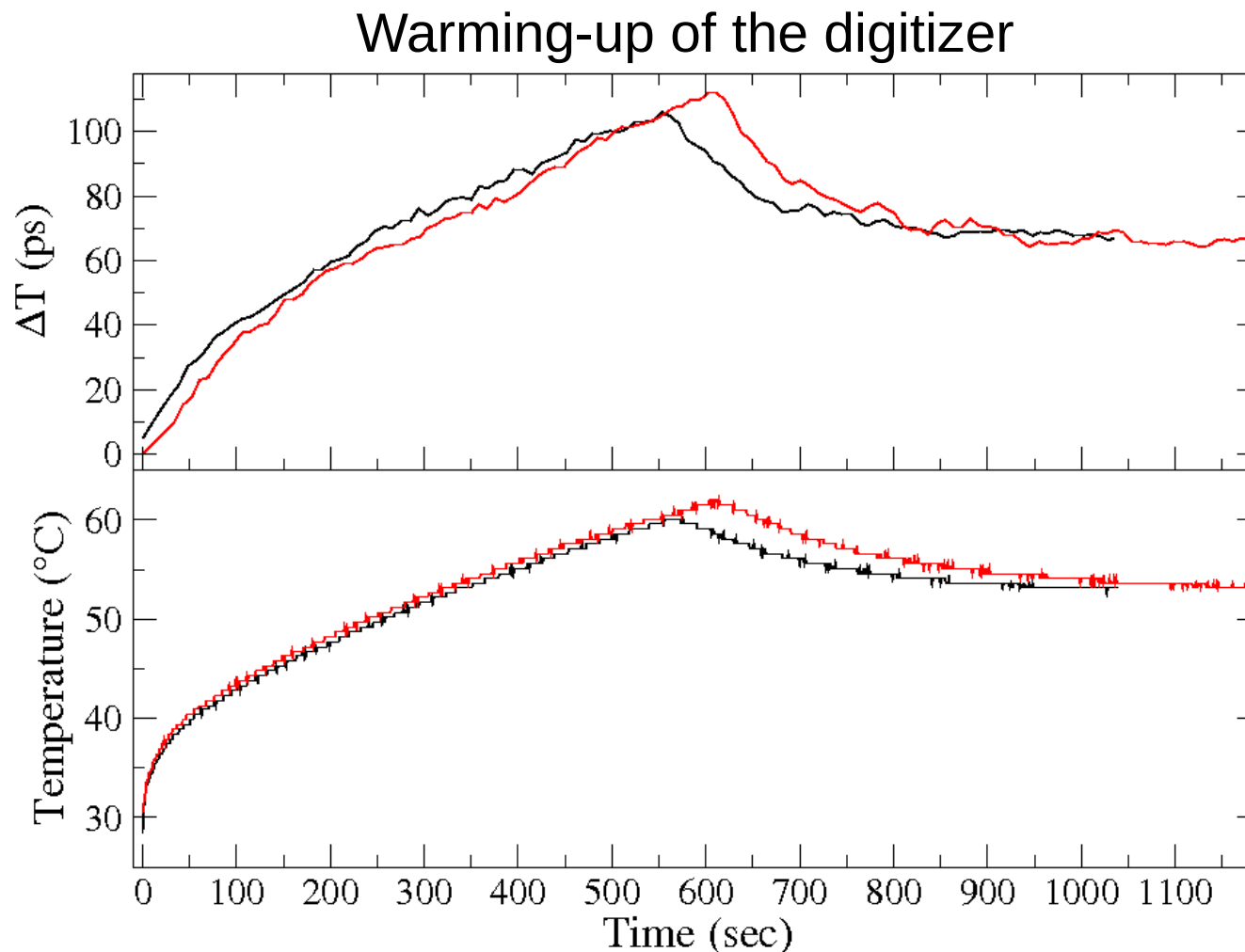
Temperature Dependence

Warming-up of the digitizer *

Delay-dependency on temperature is reproducible with required precision (~20 ps, systematic uncertainty 30 ps**)**

* Working FPGA temperature ~45-55 °C

Temperature Dependence

Warming-up of the digitizer

If necessary, precision of the SODANET system can be improved **by:**
- Stabilizing temperature (in range of ~10 °C): preferable, otherwise FPGA-based TDC would fail as well
- Implementing temperature monitoring and automatic correction of time-stamps

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Summary

university of groningen
kvi - center for advanced
radiation technology

New clock-distribution and synchronisation protocol SODANET has been developed

SODANET provides:
- **Clocking and synchronisation**
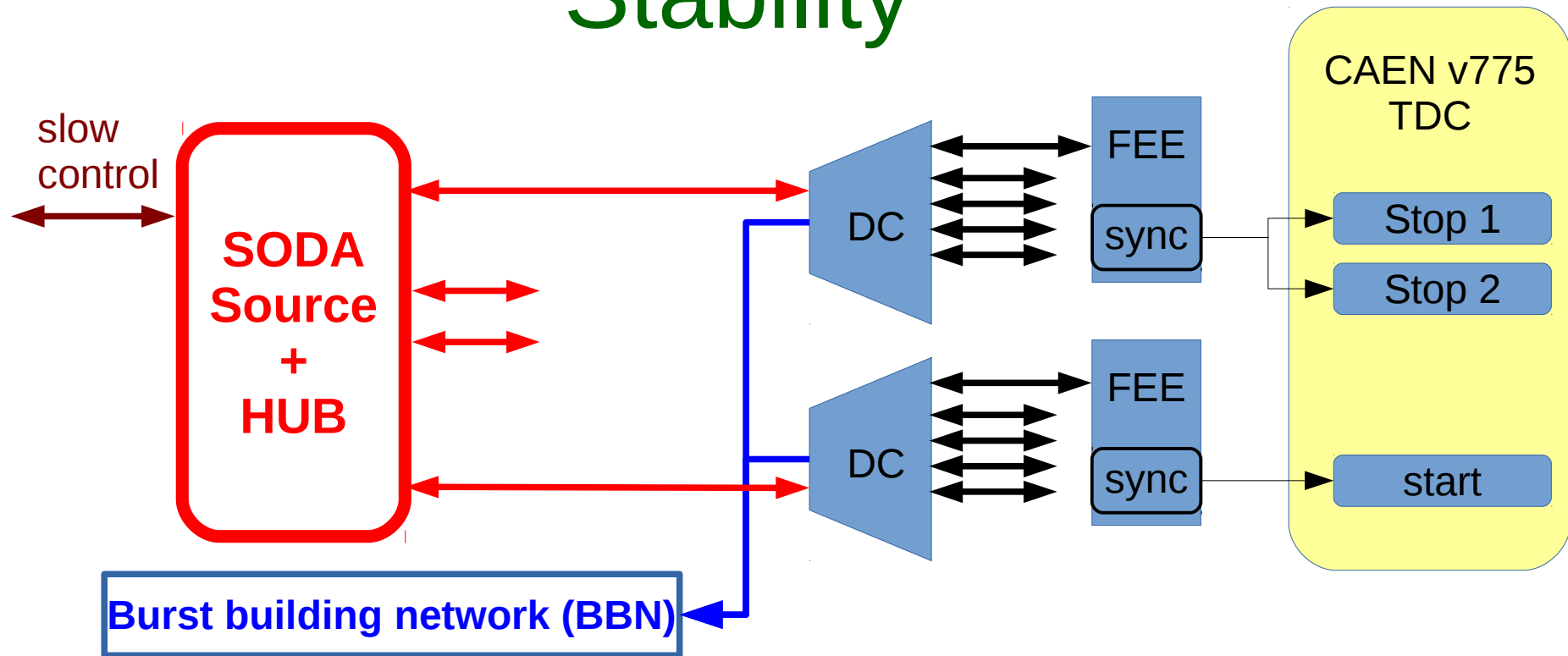- **Slow control of FEE**
- **Bunching of collected data**

SODANET implemented for FPGA-based electronics interconnected with optical (serial) links:
- **Lattice ECP3**
- **Xilinx Kintex 7**
- **Xilinx Virtex 6**

The SODANET system is stable in long terms with precision ~30 ps
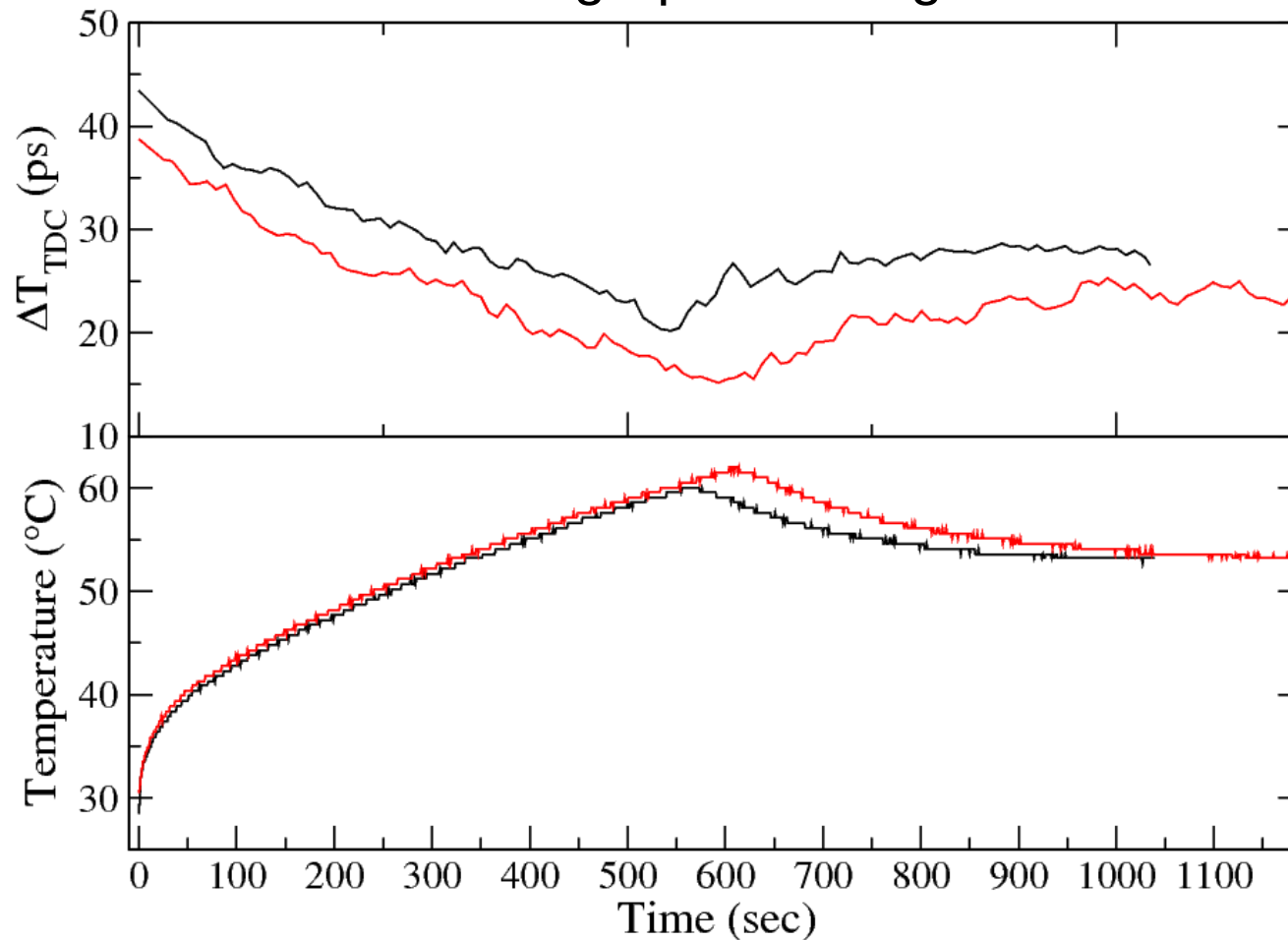
SODANET Test System
Stability

Measured quantities:

- $\Delta T = T_1$ (time difference between receives "SB start" signals): *stability of the SODANET system*

- $T_{TDC} = T_1 - T_2$: *stability of the TDC*

Temperature Dependence
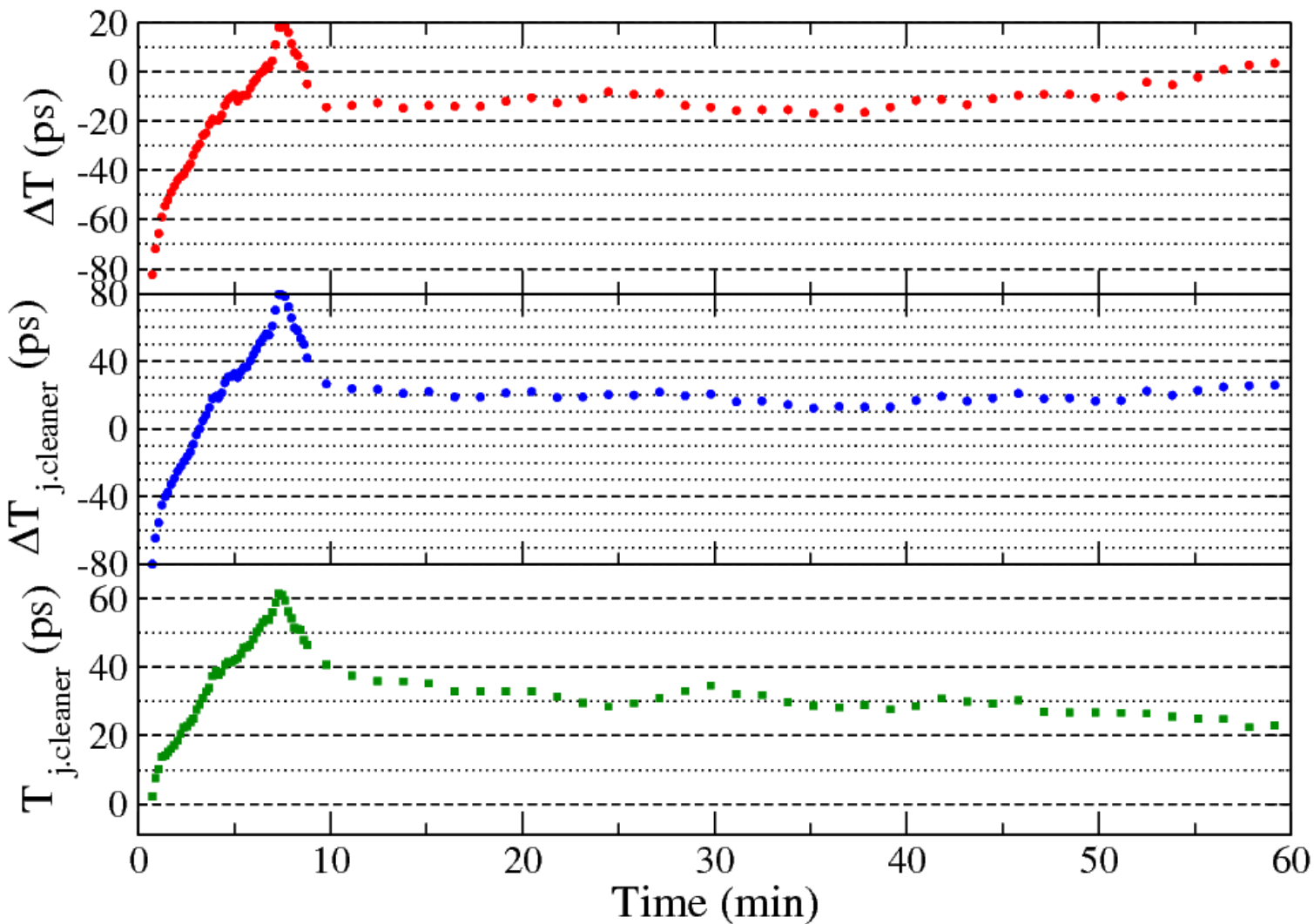
Warming-up of the digitizer

Shift in the time-difference of a split signal occurs most probably due to the change in the rise-time of the output signal (from FPGA) and different reaction to this change in different TDC inputs…
Therefore, we assume

systematic uncertainty on our measurement ~30 ps 30
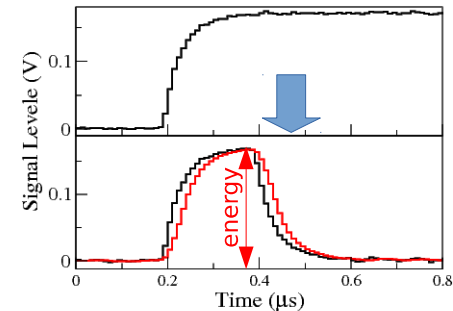
Synchronization Stability

Jump at the beginning is due to warming-up process
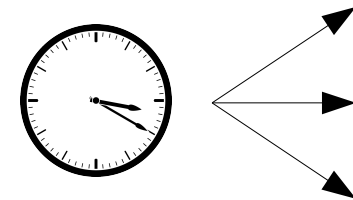
Readout Approach for PANDA

The PANDA readout consist of:

- **Intelligent self-triggered front-end**:
autonomous hit detection and data pre-processing (e.g. based on
Sampling **A**nalogue to **D**igital **C**onverter)

100101101

- **a very precise time distribution system (Synchronization Of DAq NETwork)**:
single clock-source for PANDA (event correlation)

- **time-sorting and processing data in real-time**:
processing in FPGA (**F**ield-**P**rogrammable **G**ate **A**rray)