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Status of the Readout Chain for the CBM-TRD Experiment

DPG Frühjahrstagung 2018, Bochum

Bundesministerium
für Bildung
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The CBM Experiment

Overview

- The Compressed Baryonic Matter Experiment
- Located at the International Facility for Antiproton and Ion Research (FAIR) in Darmstadt
- Fixed-target
- Primary beams from the *SIS100* synchrotron. Following phase: *SIS300*
- Self-triggered readout electronics (no hierarchical trigger system)

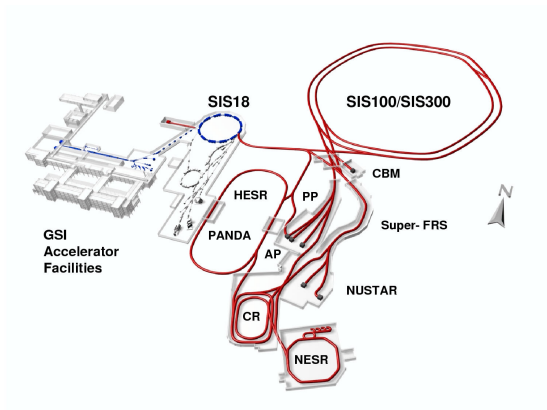
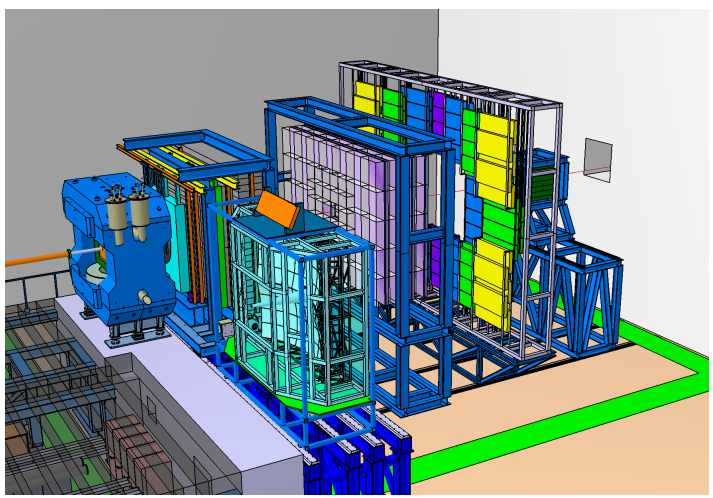


Figure: Left: Aerial view of FAIR. Right: Layout of FAIR.

The CBM-TRD Experiment

Overview

- Transition Radiation Detector
- Interaction rates of 100 kHz up to 1 MHz
- Pion suppression factor of 10 – 20
- Located 4.1m to 5.9m downstream the target



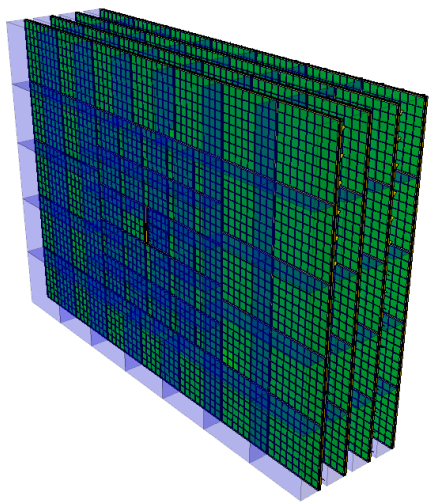


Figure: Left: Experimental setup of CBM for the SIS100. Right: Readout chamber with radiator boxes.

The Data Acquisition Chain

Concept

- Front-End Electronics based on the SPADIC ASIC
- Data Processing Board (DPB) : data combining and pre-processing
- First Level Event Selector (FLES) : event reconstruction
- Central timing and synchronization system (tDPB)

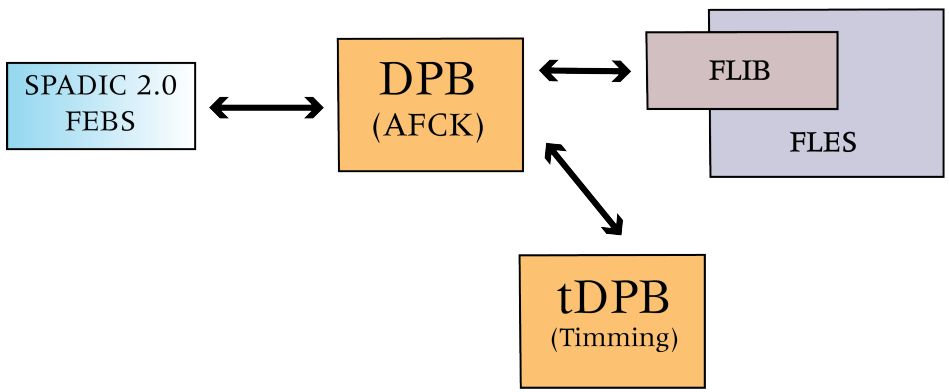


Figure: The TRD data acquisition chain using the SPADIC 2.0 ASIC and AFCK board.

Front-End Electronics

The SPADIC project

- Self-triggered Pulse Amplification and Digitization ASIC
- 32 channel mixed-signal readout ASIC
- Low-noise and low-power analog pre-amplification
- 16 MHz samplig rate
- Nine bit digitization
- Double-hit detection

SPADIC
Self triggered Pulse Amplification and Digitization asIC

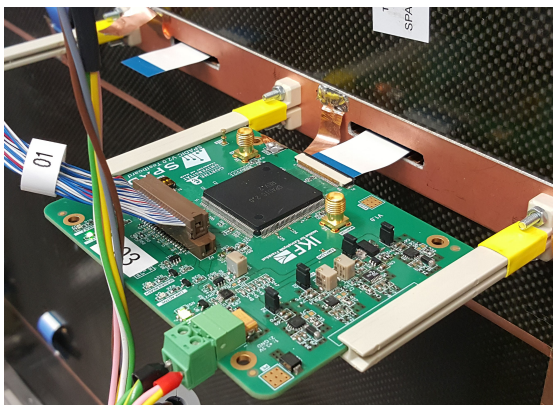


Figure: Right: SPADIC project logo. Left: SPADIC 2.0 test board.

The Data Processing Board

Overview

- Read-out controller, data concentrator and pre-processing platform
- Implements the TRD feature extraction pre-processing
- Developed on the AMC FMC Carrier Kintex (AFCK)
- Xilinx Kintex 7 device

Figure: AMC FMC Carrier Kintex.

The Data Acquisition Chain

Implementation

- Read-out of three SPADIC 2.0 FEBs per AFCK
- Slow-control and system configuration implemented by IPbus
  - Used for initialization and configuration of the SPADIC 2.0 FEBs
  - Baseline measurement and correction
  - Digital and analog configuration of the SPADIC 2.0
- The SPADIC v2.0 uses the STS-HCTSP protocol for data transmission and configuration

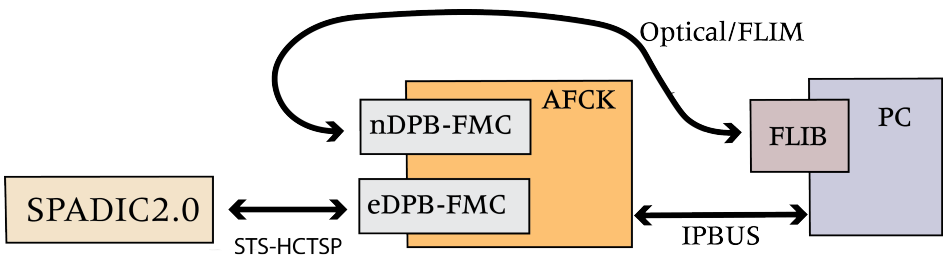


Figure: The TRD data acquisition chain using the SPADIC 2.0 ASIC and AFCK board.

Feature Extraction

Simulation framework

- Relevant signal processing stages: baseline correction and cluster finder
- Simulation framework has been developed using:
  - GARFILD simulation
  - Test beam recordings
- Simulation engine performs:
  - Hardware simulation
  - HDL (Hardware Description Language) simulation
  - Direct interface to CbmRoot

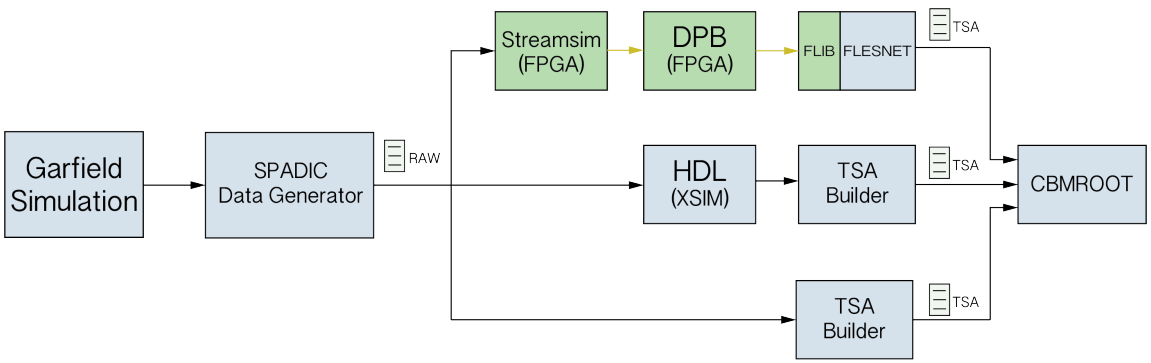


Figure: Feature extraction simulation chain.

DESY Testbeam 2017

Experimental setup

- Performed in August at the Deutsches Elektronen-Synchrotron (DESY)
- Four CBM-TRD prototypes (near-to-final $95 \times 95\ cm^2$ MWPCs)
- Two 2012-style TRD prototypes for position reference
- Two Scintillator/PMT stations
- Eight SPADIC 2.0 front-end boards

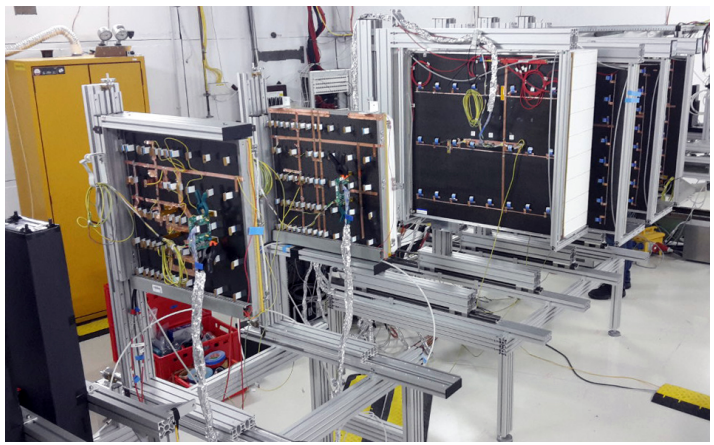


Figure: Experimental setup at DESY. Beam table and mounted TRD MWPCs with SPADIC 2.0 front-end boards.

GIF Testbeam 2017

Experimental setup

- One 2012-style MWPC prototype at a distance of 1.5m to the centre of the source
- Four SPADIC 2.0 front-end boards
- Four AFCK used to read-out the front-end boards

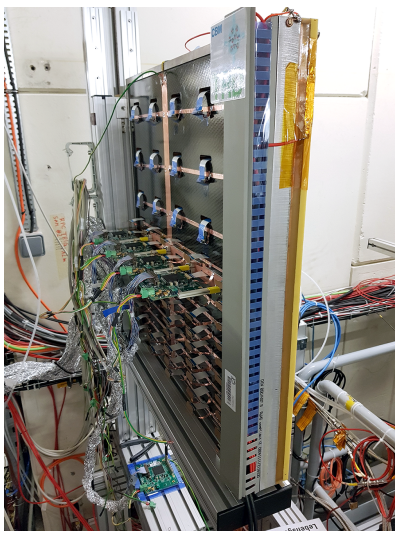


Figure: Experimental setup at GIF. A 2012-style MWPC prototype with four SPADIC 2.0 front-end boards.

Next Steps

Comissioning

- Front-end boards using the SPADIC 2.1 are to be produced during the first quarter of 2018
  - Improved message format implemented on the STS-HCTSP protocol
  - Increase the usage of the data transmission link
- Production and testing of Quad-FEBs
- Production and testing of the GBTx based Common Read-Out Controller Board (C-ROB)

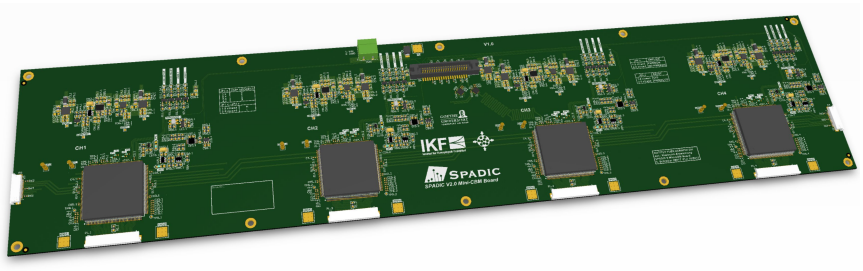


Figure: View in three dimensions of the quad SPADIC 2.0 FEB (courtesy IKP, Frankfurt).

Closing notes

Summary

- Two testbeams for CBM-TRD were performed during 2017
- Four near to final CBM-TRDs were used
- A total of eight SPADIC 2.0 front-end boards were distributed across the detectors
- Four AFCK boards were used a Data Processing Boards and one AFCK as timinig master
- Production and testing of the new SPADIC 2.1 during first quarted of 2018
- GBTx based readout and C-ROB development on-going