Data preprocessing of the DAQ system for TOF detector in CBM experiment

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Outline

- Introduction of CBM experiment
- Structure of DAQ for TOF subsystem
- Data preprocessing strategy
- Outlook

1. Introduction of CBM experiment

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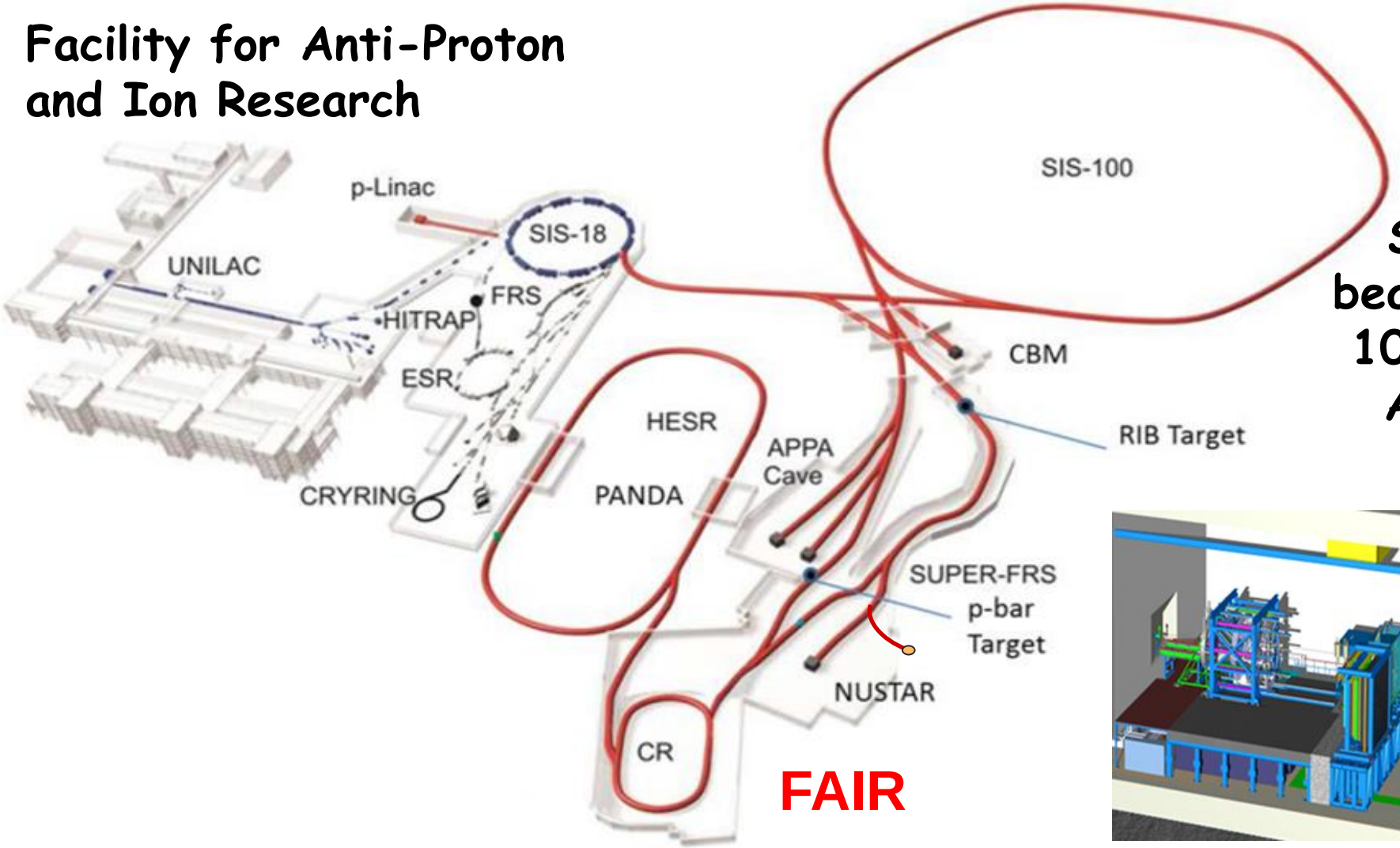
Facility for Anti-Proton and Ion Research



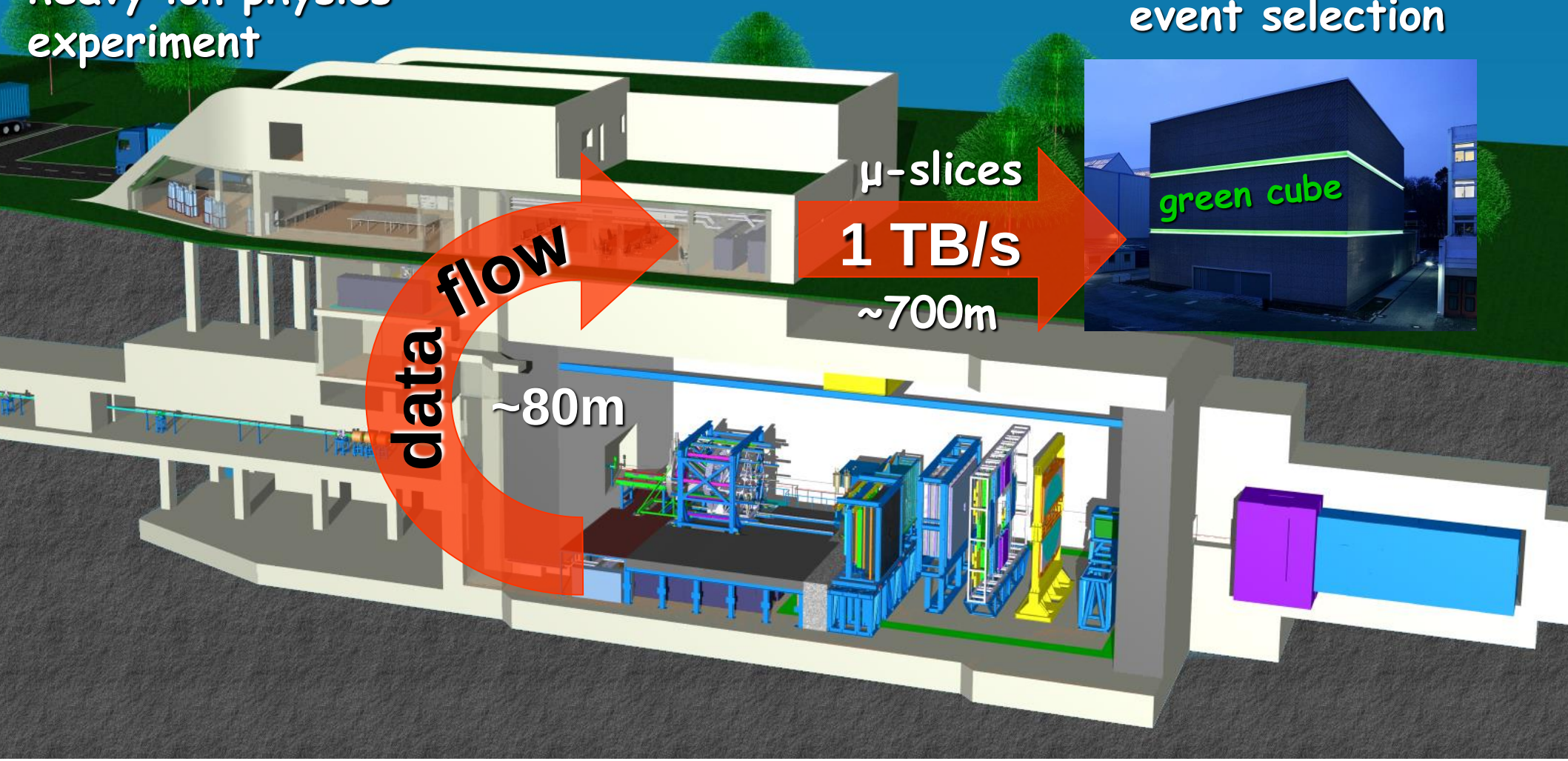
SIS100
beam energy
10 AGeV/c
Au-beam

1. Introduction of CBM experiment

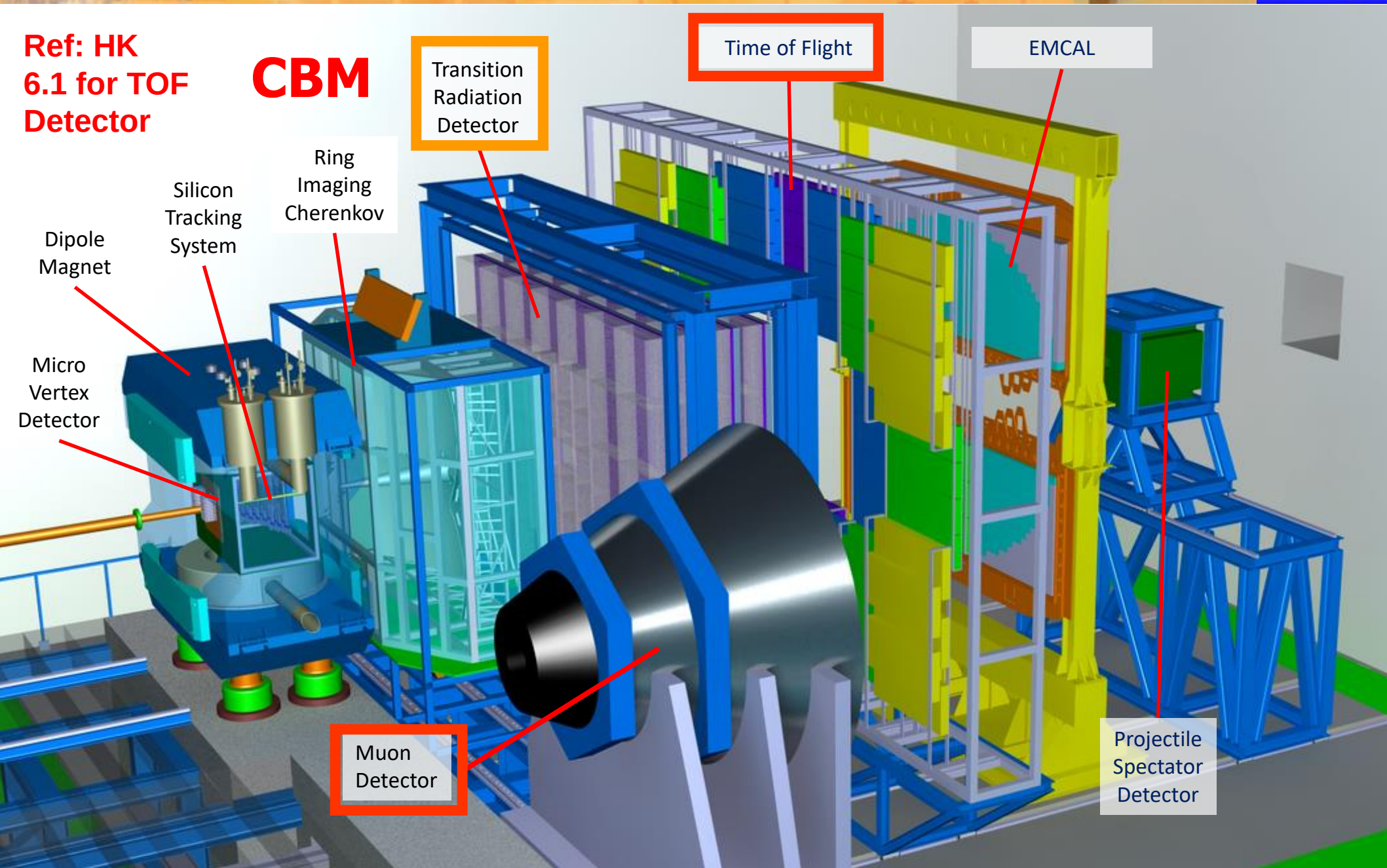
A fixed target, high interaction rate, heavy ion physics experiment

data pre-processing FLES input cluster

online timeslice building and event selection

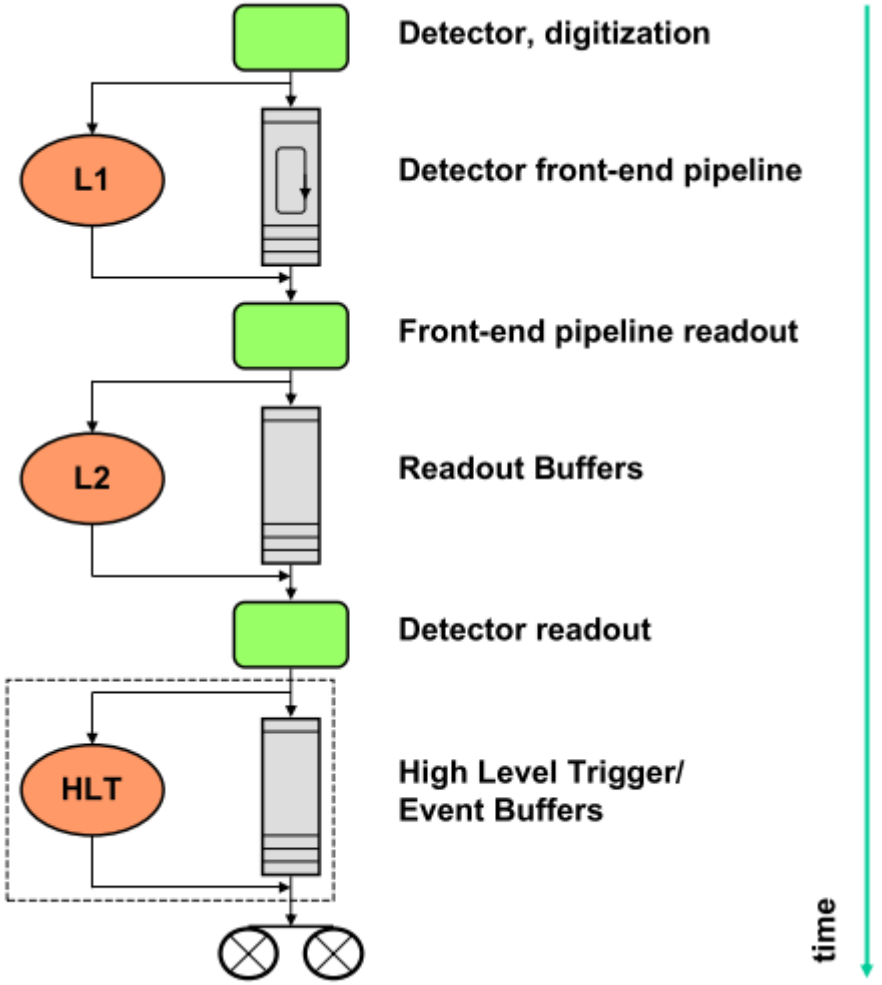


1. Introduction of CBM experiment



2. Structure of DAQ for TOF subsystem

2. Structure of DAQ for TOF

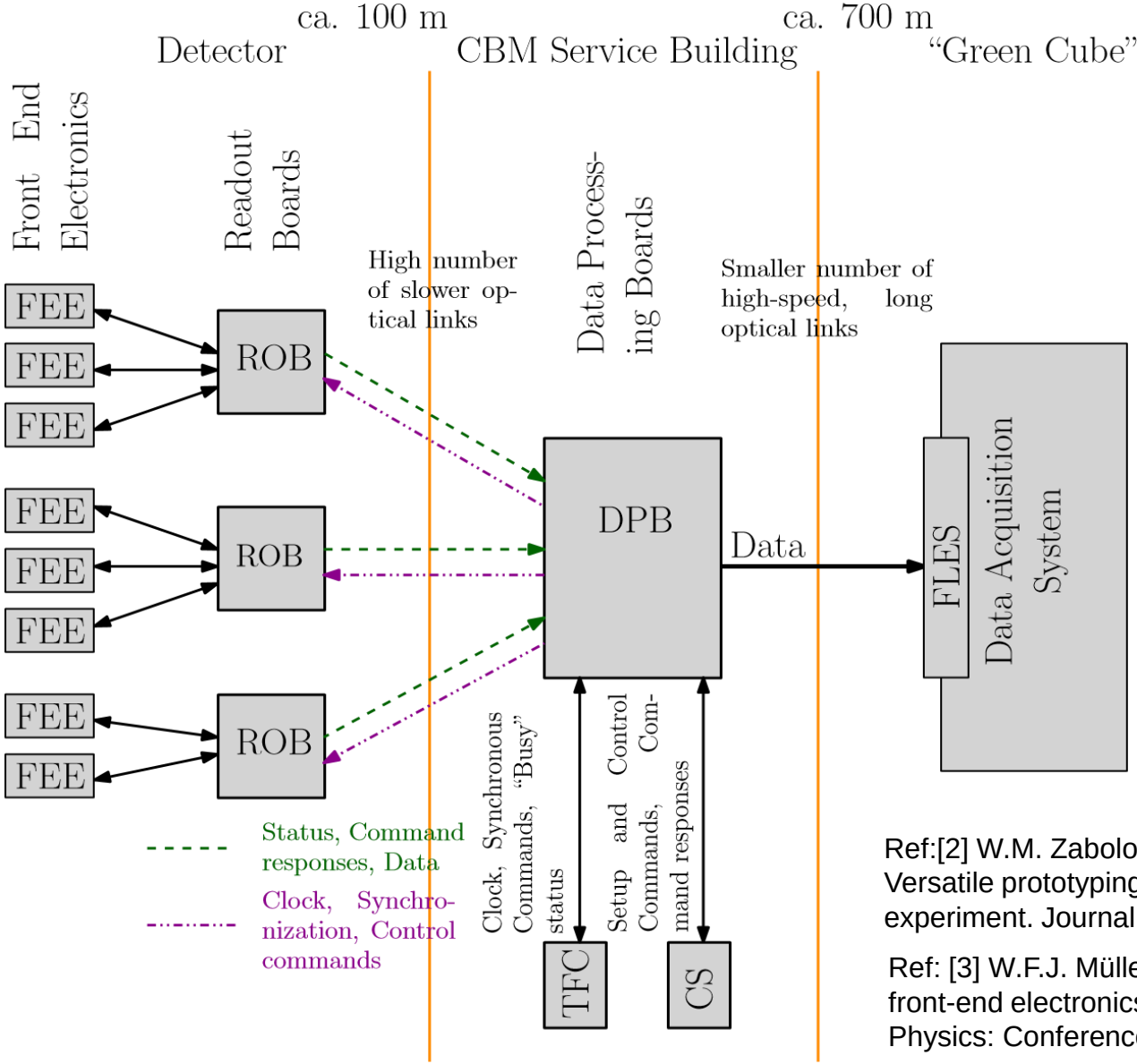


Conventional DAQ system:

1. Multi-Level trigger system. (several microseconds are need for level 1 triger)
2. Pipeline readout.

Ref:[1] V. Lindenstruth, I. Kisel, Overview of trigger systems. Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment. 2004, 535: 48–56.

2. Structure of DAQ for TOF



CBM requirement:

Complex algorithms are needed for trigger.

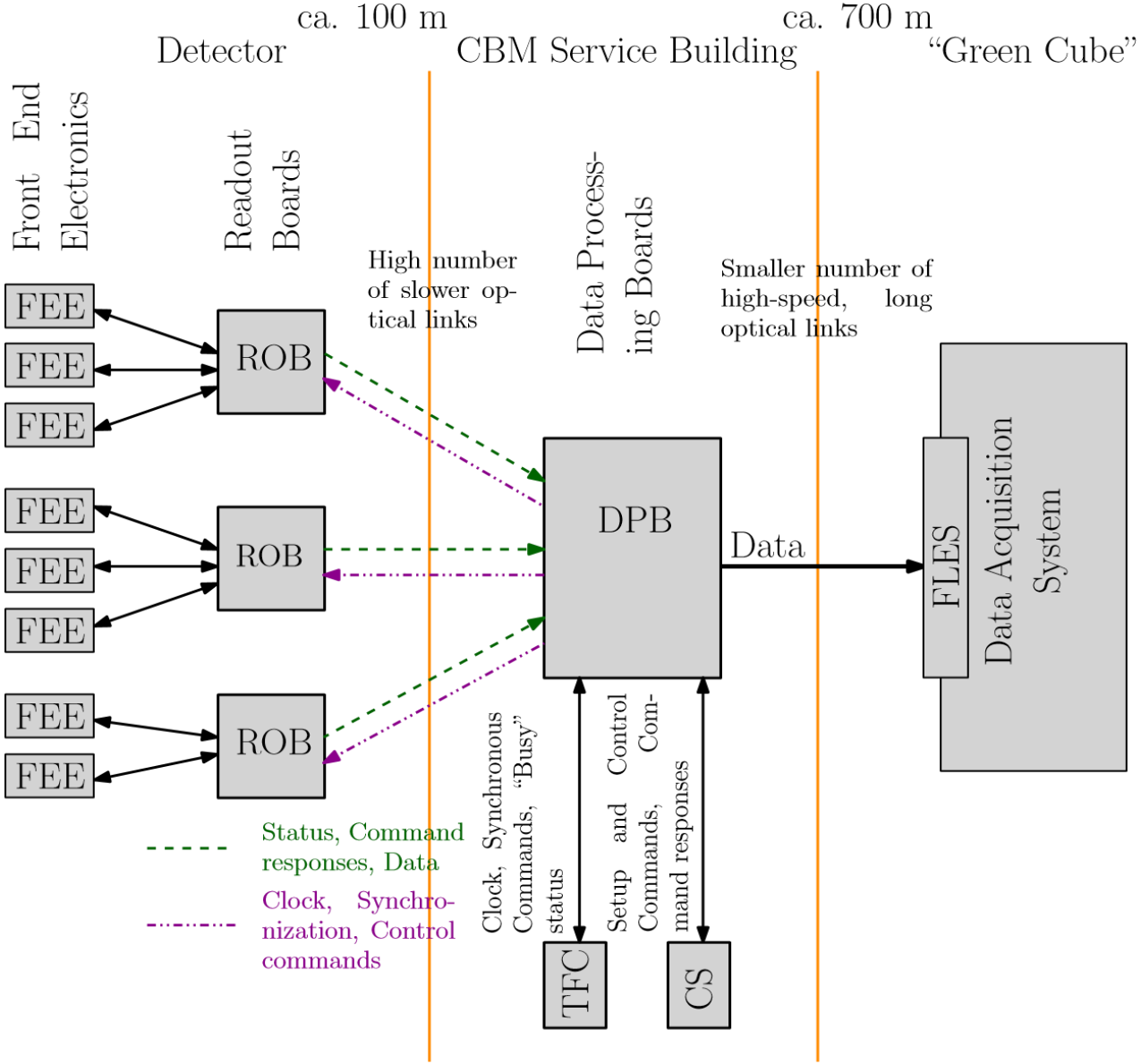
Features:

1. Data must have timestamp to allow event selection in computer farm.
2. High transfer speed is needed to acquire all the data.

Ref:[2] W.M. Zabolotny, G. Kasprowicz, A.P. Byszuk, D. Emschermann, et al., Versatile prototyping platform for Data Processing Boards for CBM experiment. Journal of Instrumentation. 2016, 11: C02031.

Ref: [3] W.F.J. Müller, The CBM experiment @ FAIR-new challenges for front-end electronics, data acquisition and trigger systems. Journal of Physics: Conference Series. 2006, 50: 371–376.

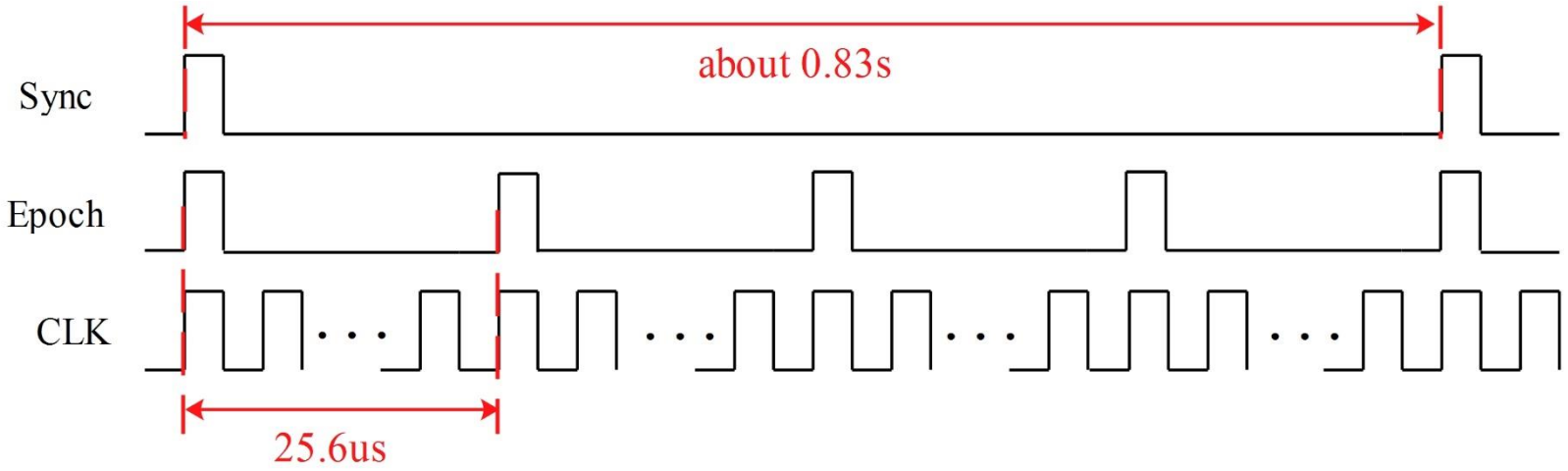
2. Structure of DAQ for TOF



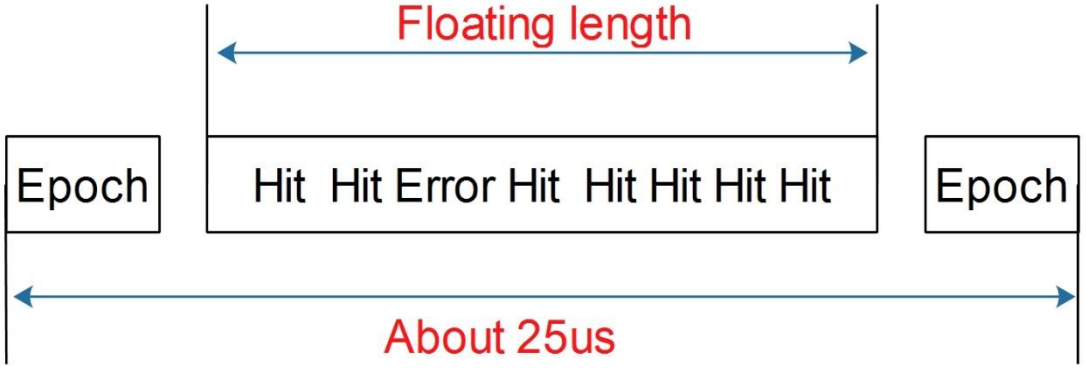
DPB: Data Preprocessing Board.
FLES: First Level Event Selection.
FLIB: FLES Interface Board.
GET4: FEE for TOF detector. There are 4 channels for one chip.

Epoch Message: timestamp from GET4.
Hit Message: data information from detector sent out by GET4.
MicroSlice(MS): data frame used in DPB board.
TimeSlice: data frame used in computer farm.

2. Structure of DAQ for TOF

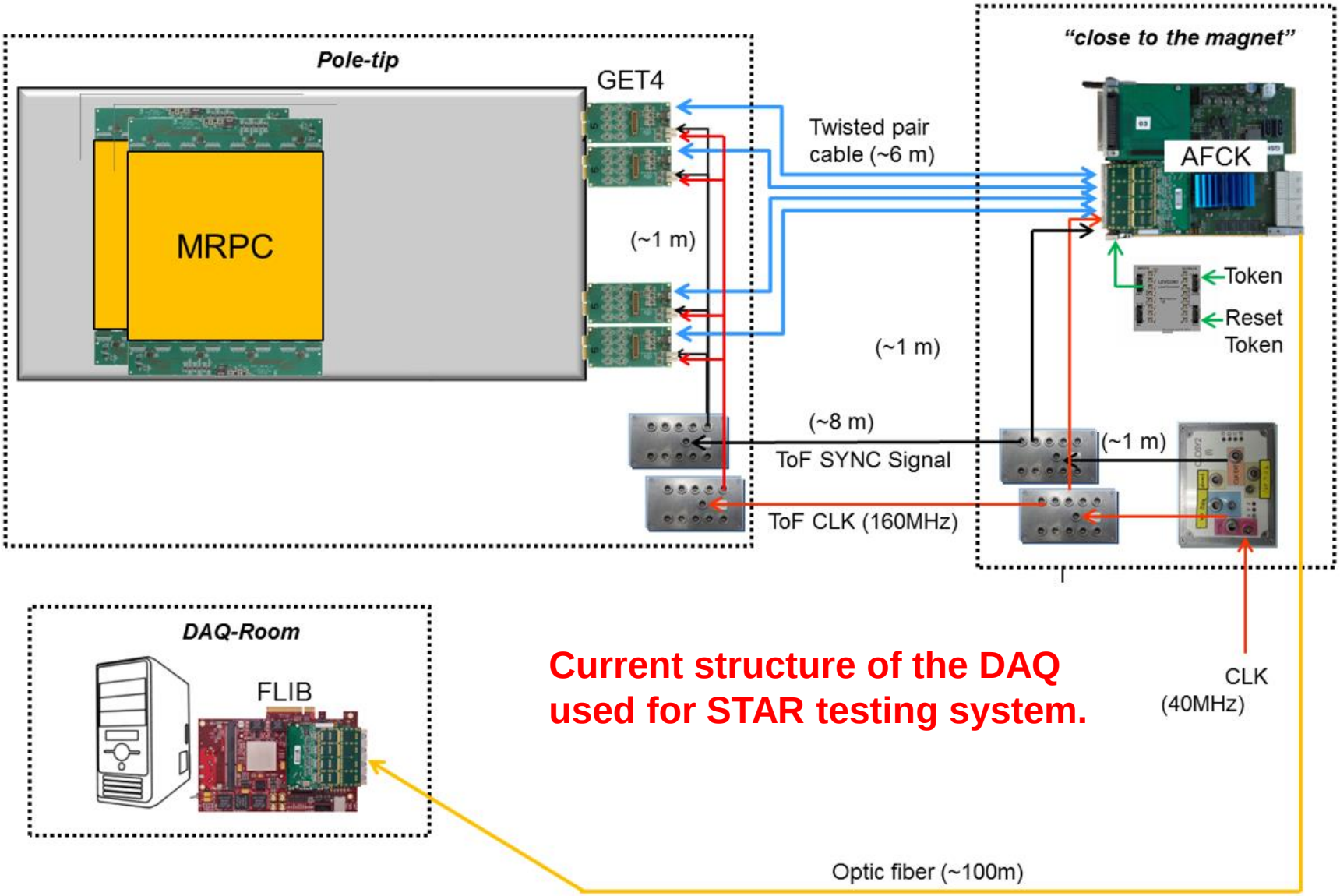


Logic of the clock, epoch and sync



Structure of MicroSlice

2. Structure of DAQ for TOF



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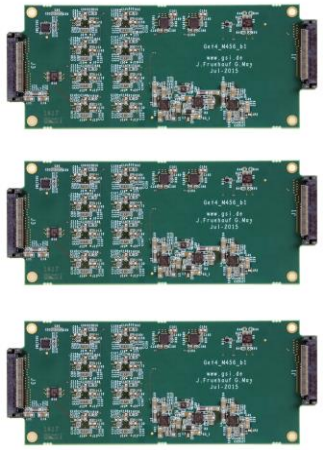
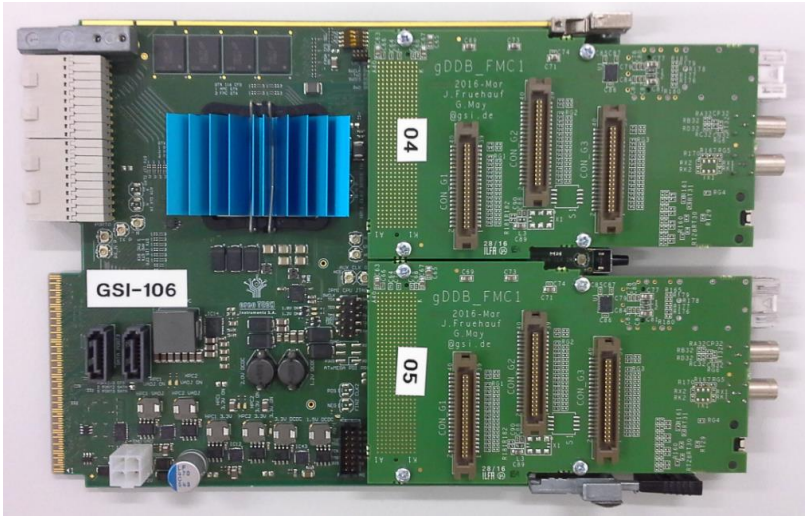
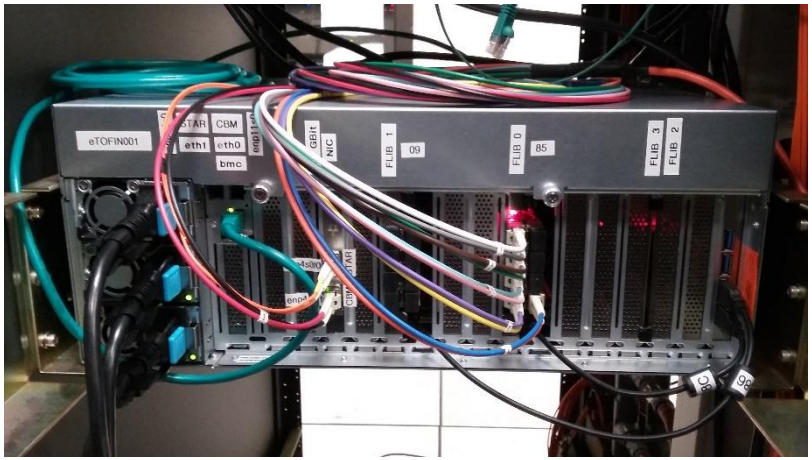


GET4 Board
(8 GET4 chips/board)

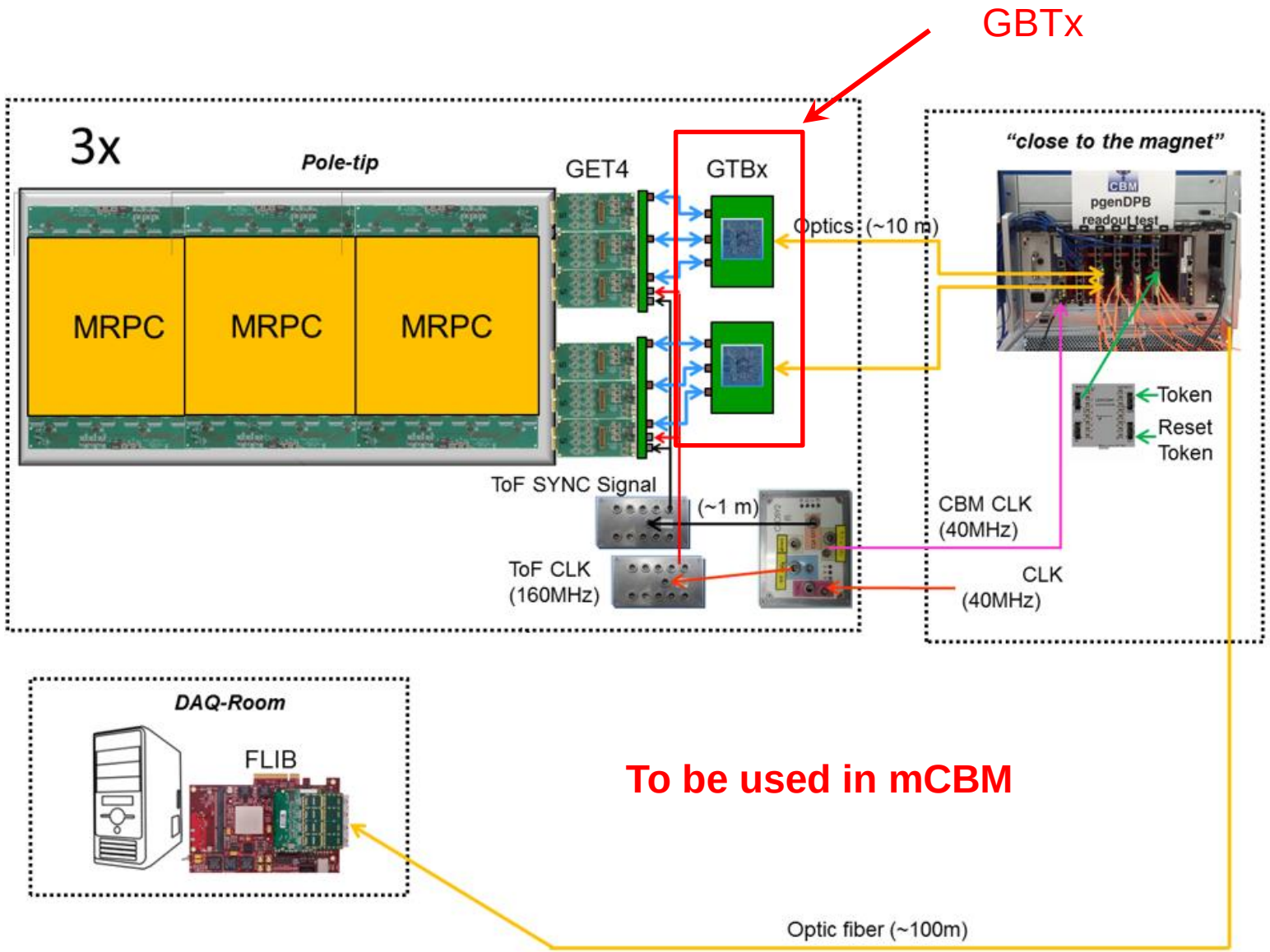


AFCK
DPB Board



DAQ PC
FLIB

2. Structure of DAQ for TOF



To be used in mCBM

Ref: HK 20.5 for GBTx

3. Data preprocessing strategy

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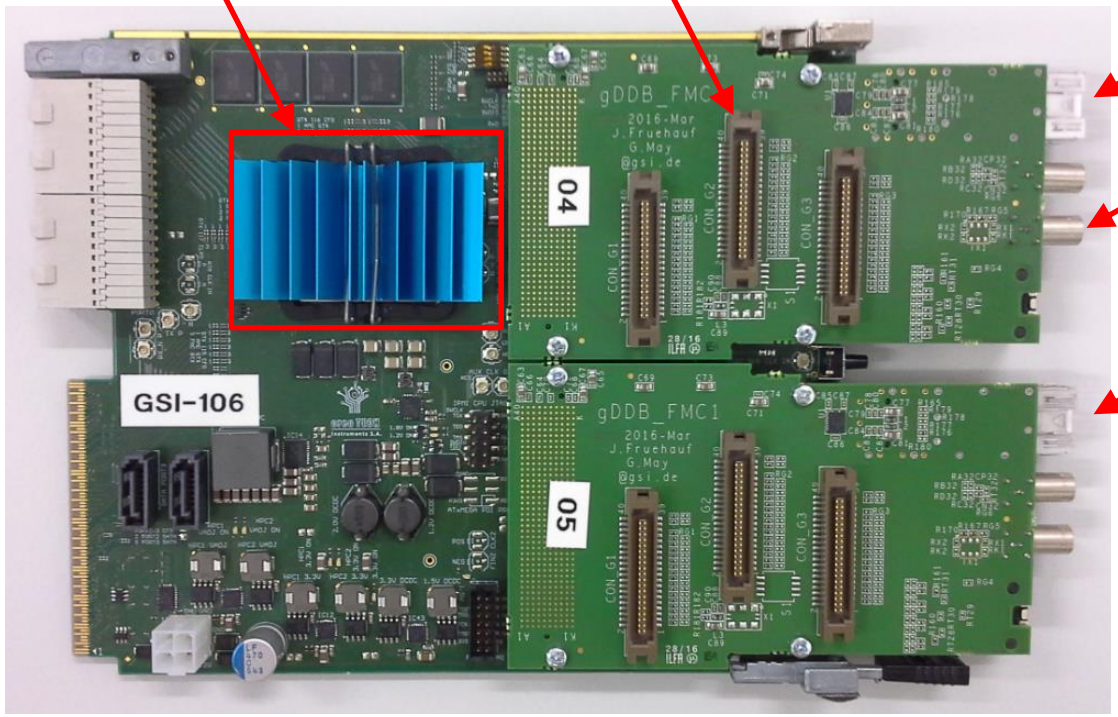
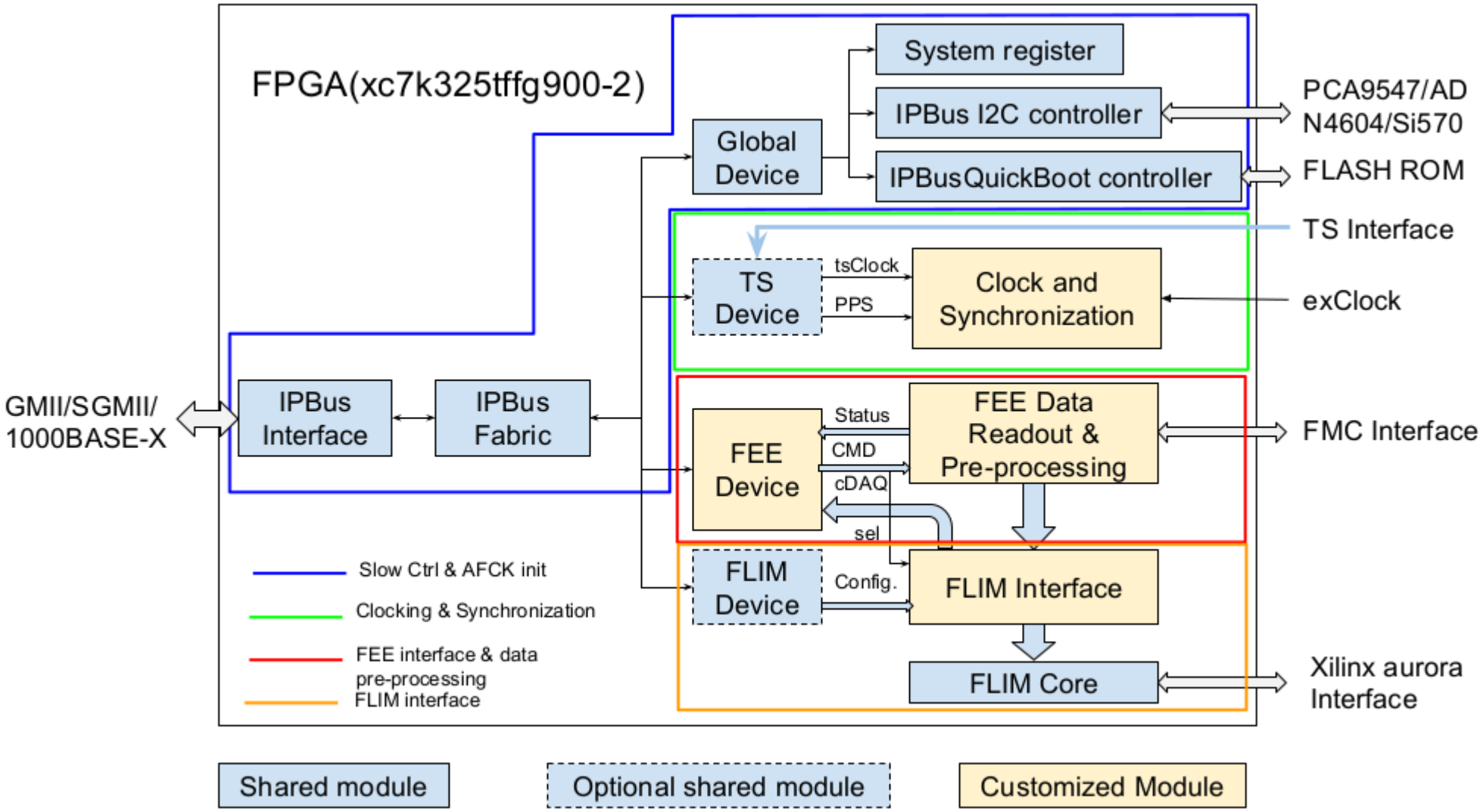


3. Data preprocessing strategy



FLIM: FLES Interface Module

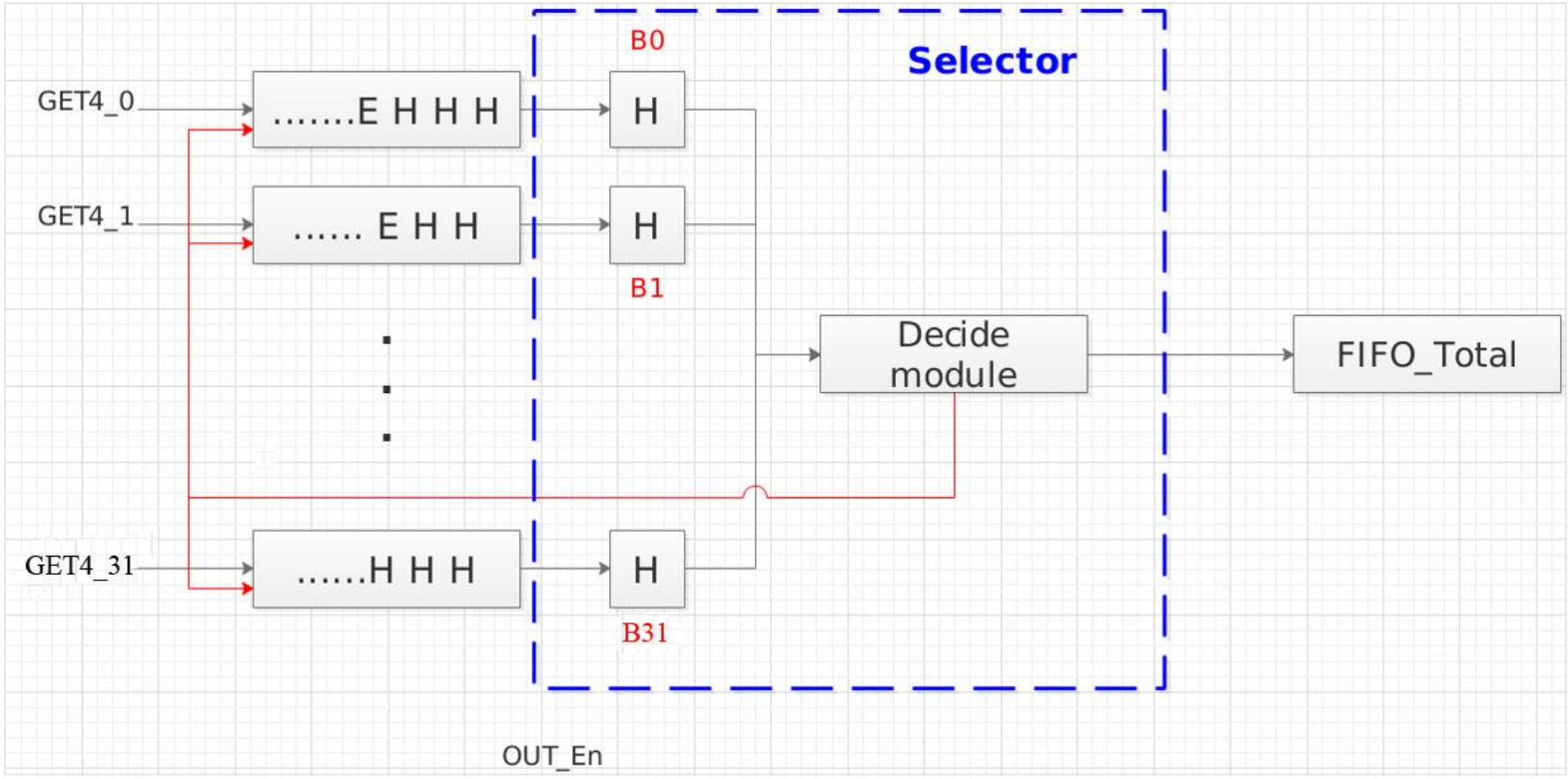
3. Data preprocessing strategy

- RealMicroSlice (RealMS) basic requirements
- 1. All GET4 share one same epoch.
- 2. Hit message must be sorted at first(to be implemented).

3. Data preprocessing strategy

- Requirements
- 1. Data acquisition has to detect and remove all different kinds of error:
  - **Epoch loss**: caused by GET4 errors.
  - **GET4 stop sending data**: because of GET4 broken.
  - **Corrupted data**: due to interference.
- 2. Broken GET4 should be recovered if it is possible.

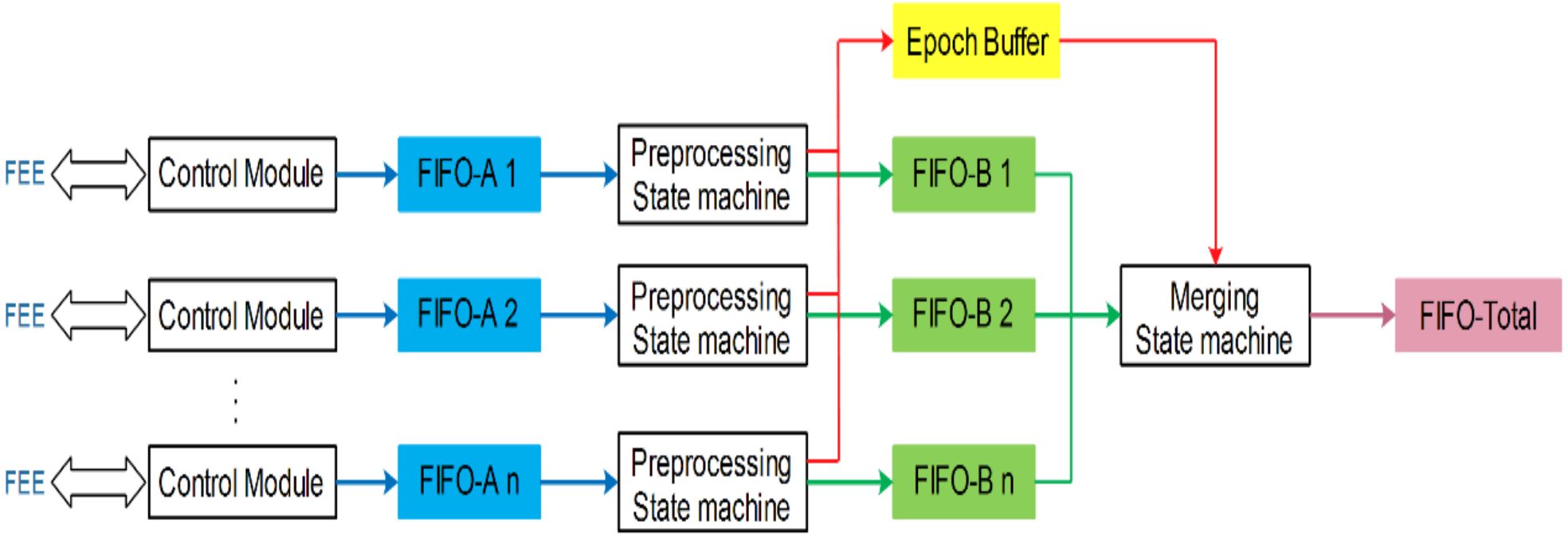
3. Data preprocessing strategy



One possible strategy

Input speed	Channel	Read speed	Read clock
80Mbit/s	<=32	2-3 cycle/ data	> 160MHz

3. Data preprocessing strategy



Improved Data Merging strategy(It is used now)

Input speed	Read speed	Merging speed	Channel
80Mbit/s	2 cycle/data	1 cycle /data	**64**

3. Data preprocessing strategy

Error detecting and removing strategy

Error detection:

1. There are no epoch message in one GET4 for 30μs: epoch interval time is 25.6 μs, and there may be not epoch sent out from GET4 due to chip broken.
2. There are mismatch for epoch: the received epoch counter number is different from the counter number got from local FPGA.
3. Same epochs are received from one GET4: a broken GET4 may send same epoch for several times.
4. Epochs are lost: the received epoch counter number is not continued.

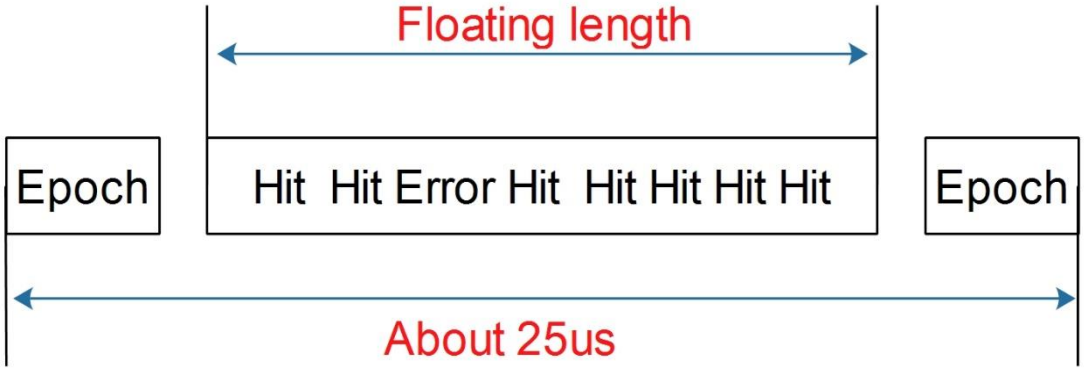
Error processing:

1. Synchronization command are sent out for Error GET4 chips every **2s(It is also a method used to recover GET4 chips**).
2. Remove the same epoch.
3. Repair the lost epoch.

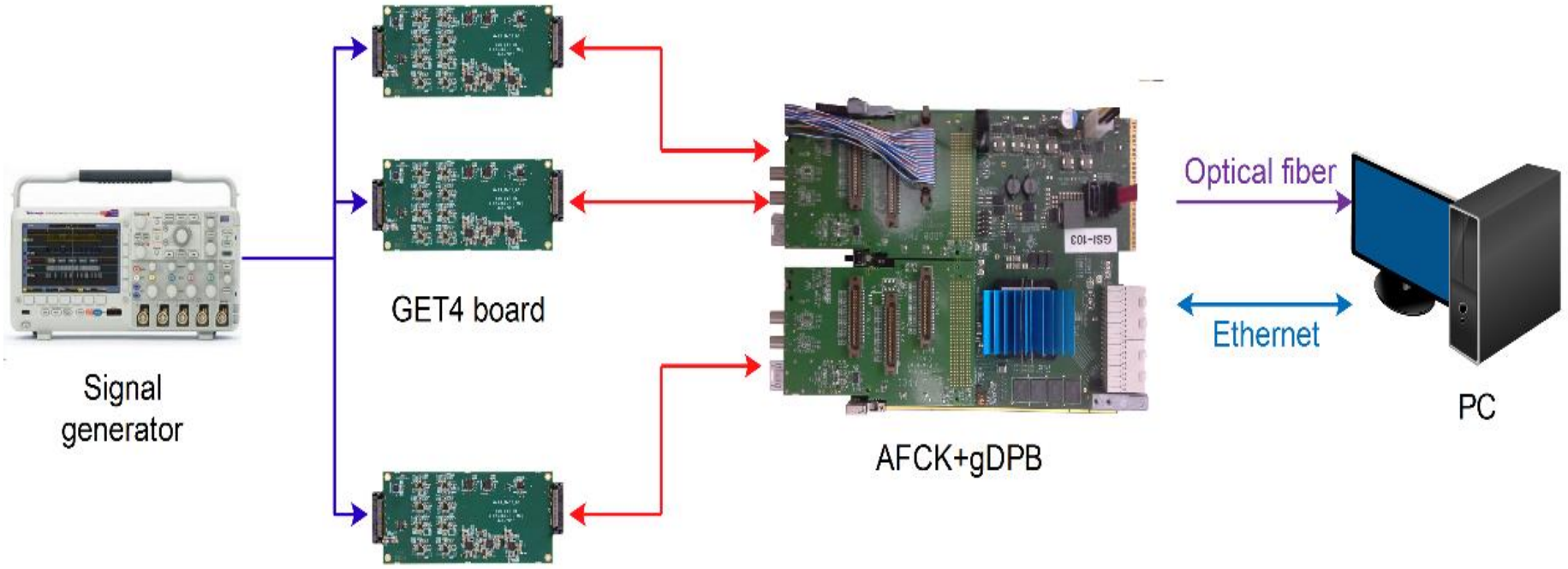
3. Data preprocessing strategy

Real MS

1. All epochs are aggregated into one epoch with a special ID.
2. Data length is not fixed.
3. The interval time between two epoch marks is about 25us.

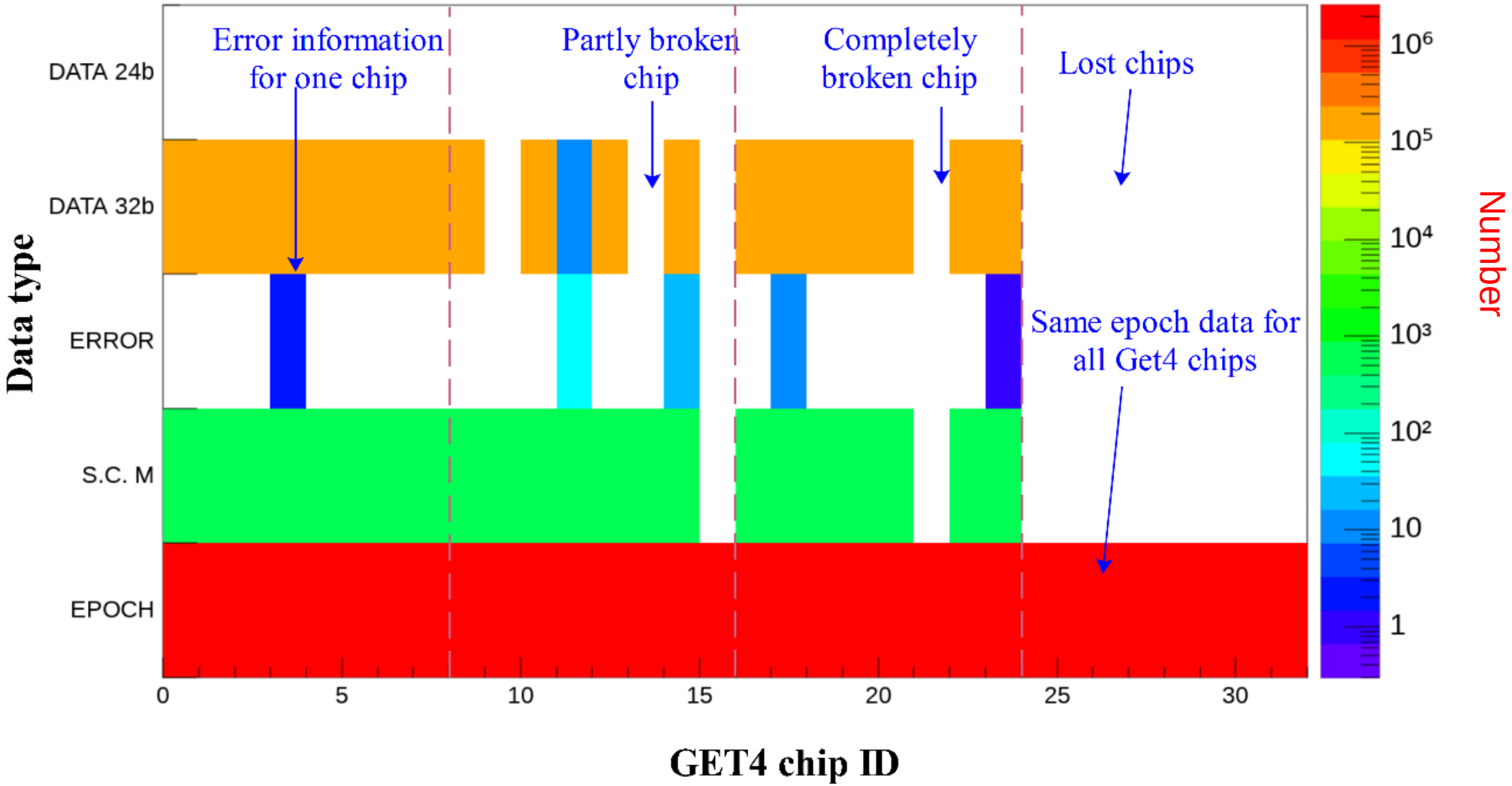


3. Data preprocessing strategy



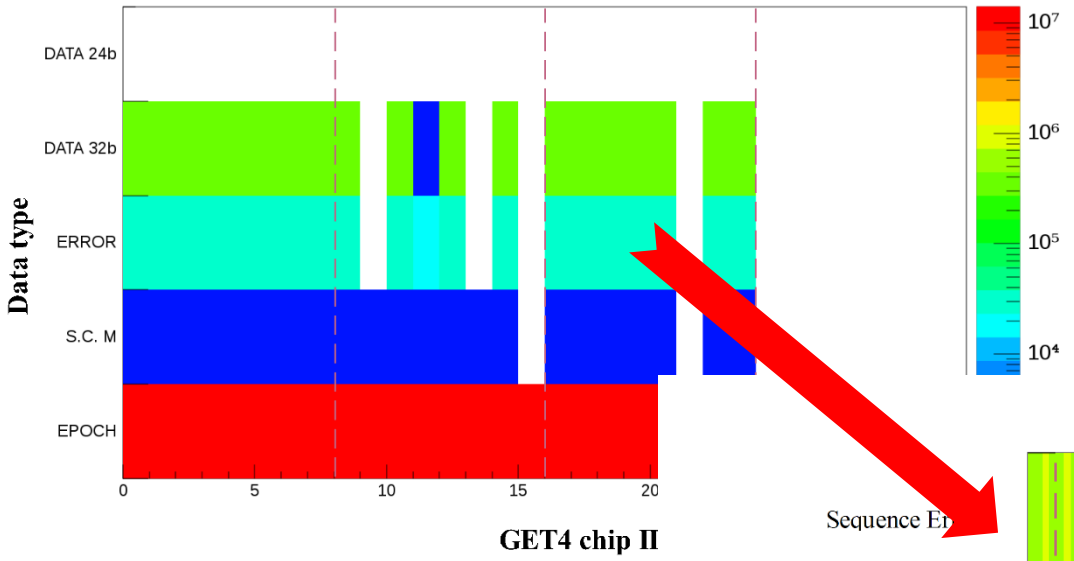
Test setup for the preprocessing firmware

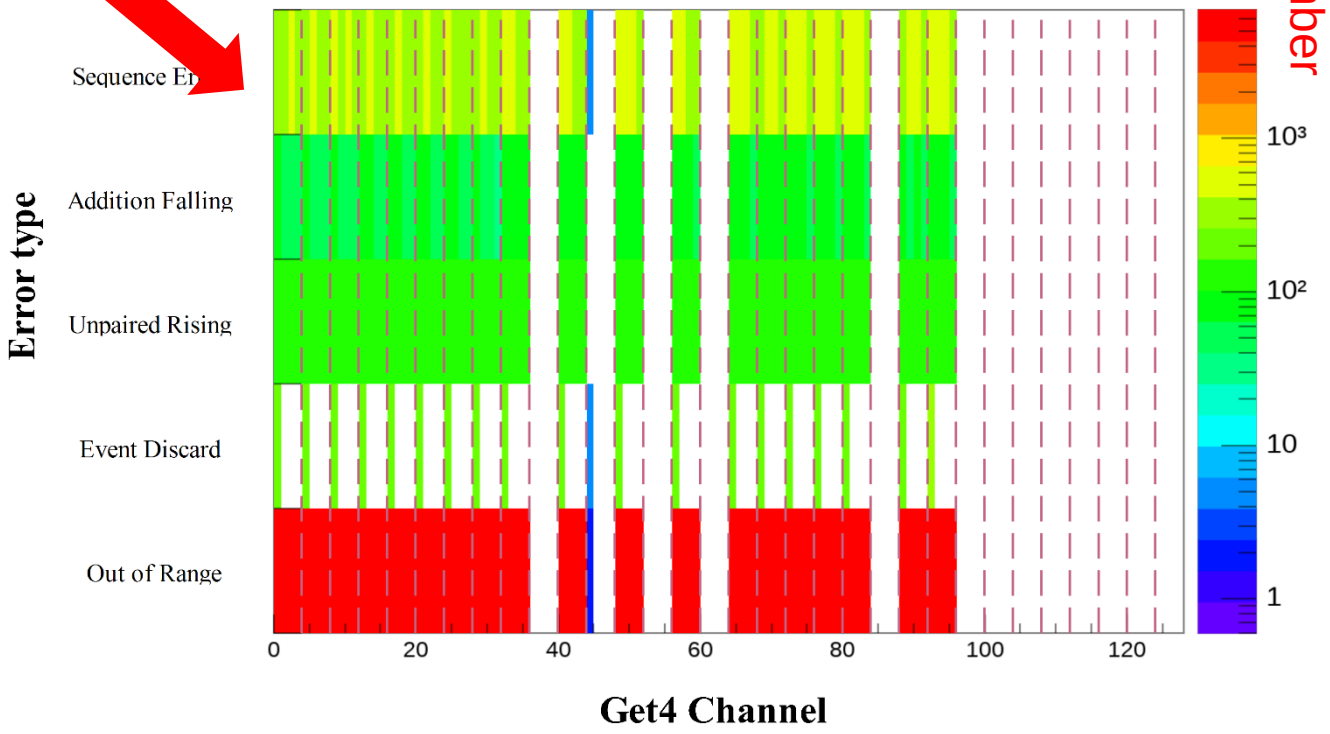
3. Data preprocessing strategy



S.C.M: Slow Control Message

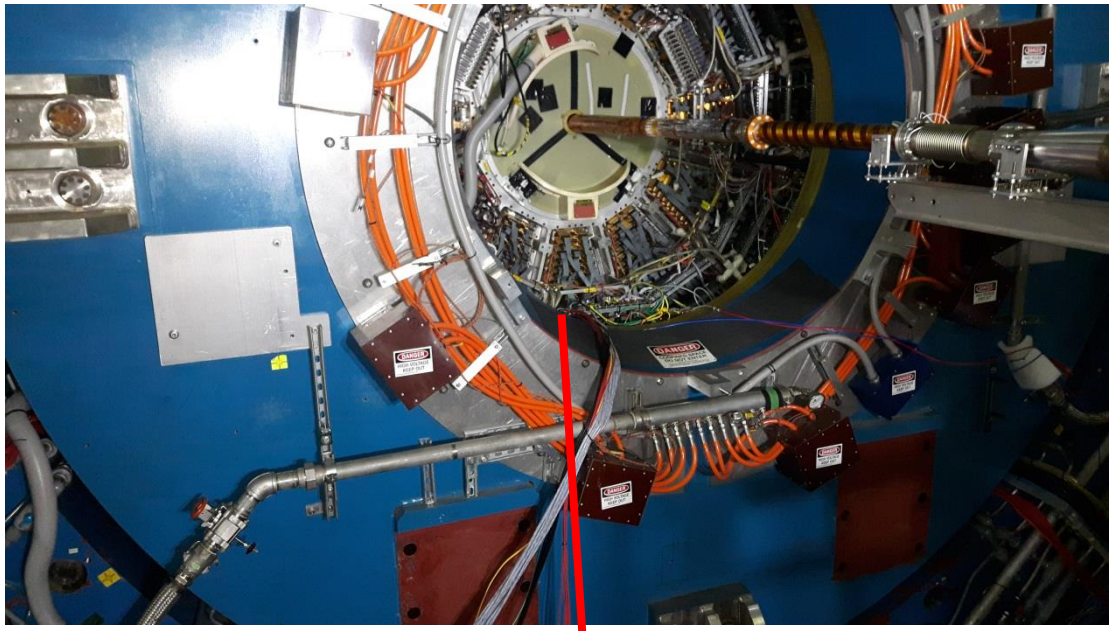
3. Data preprocessing strategy

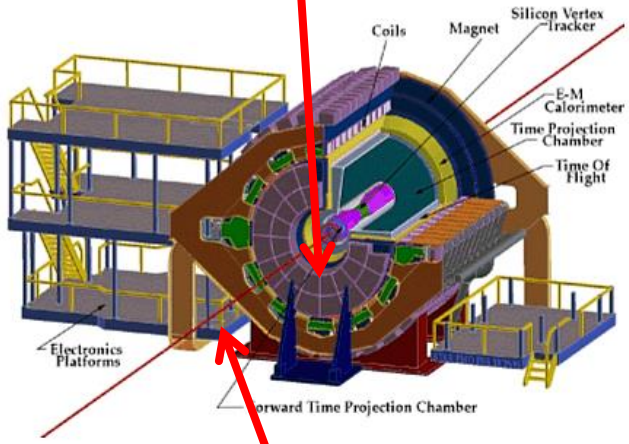




3. Data preprocessing strategy

DAQ system testing in STAR

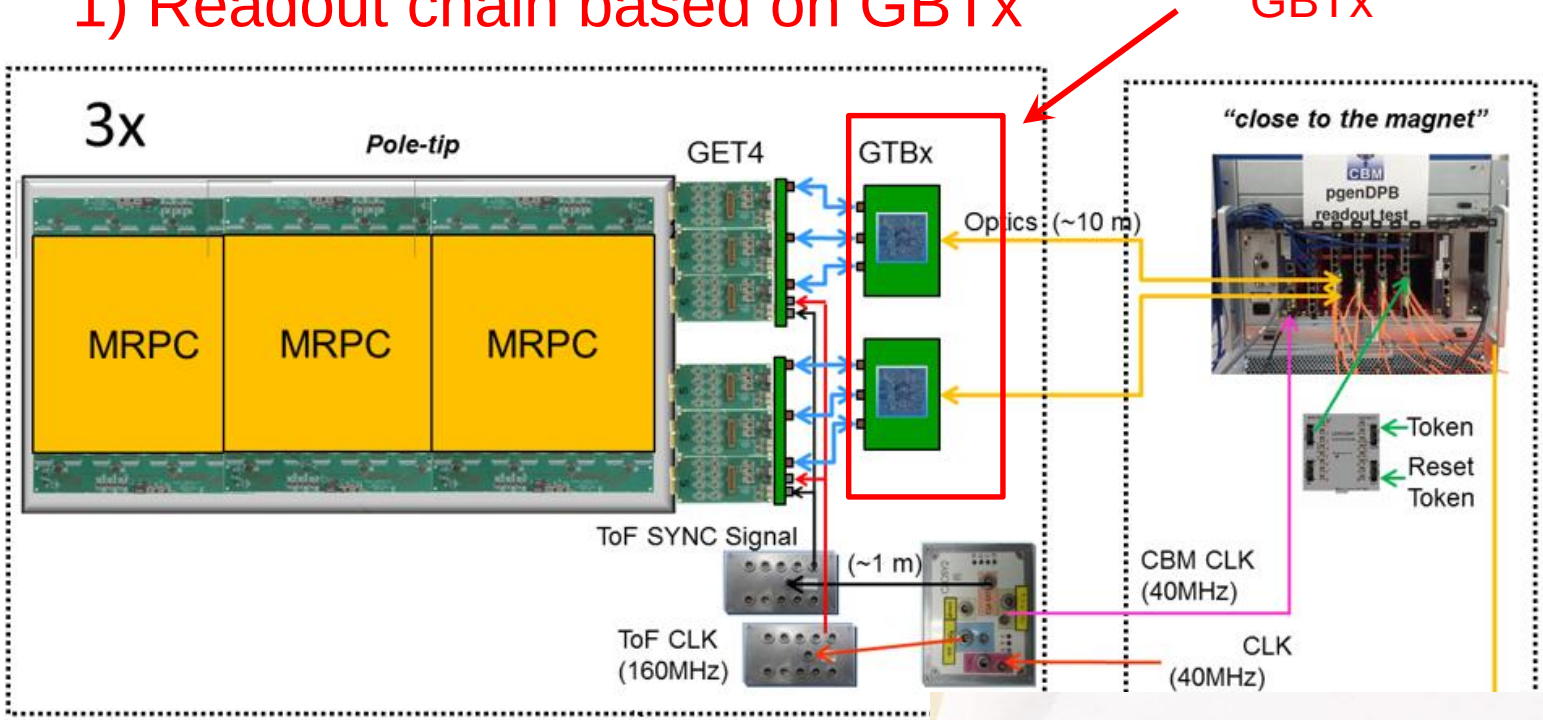


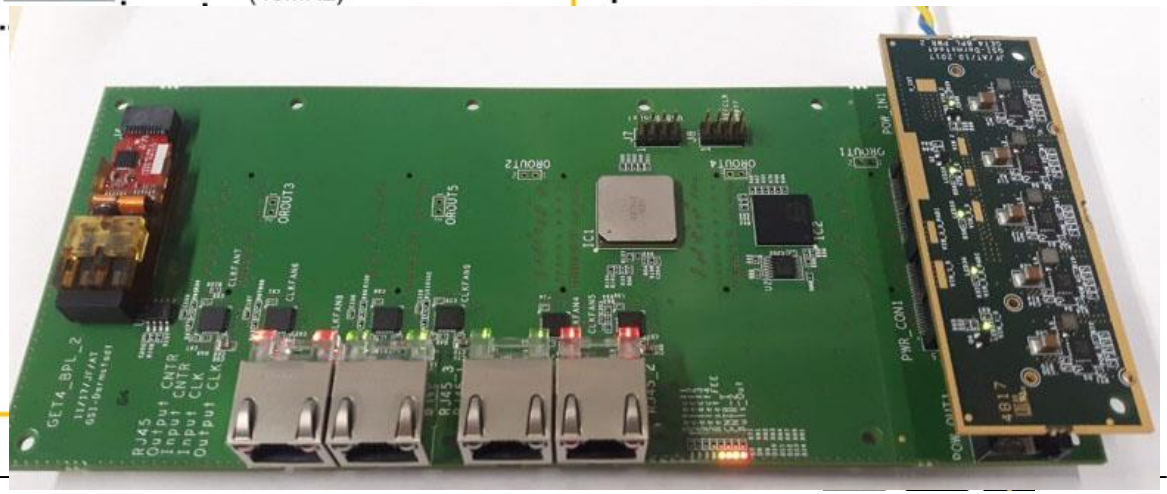


4. Outlook

4. Outlook

1) Readout chain based on GBTx

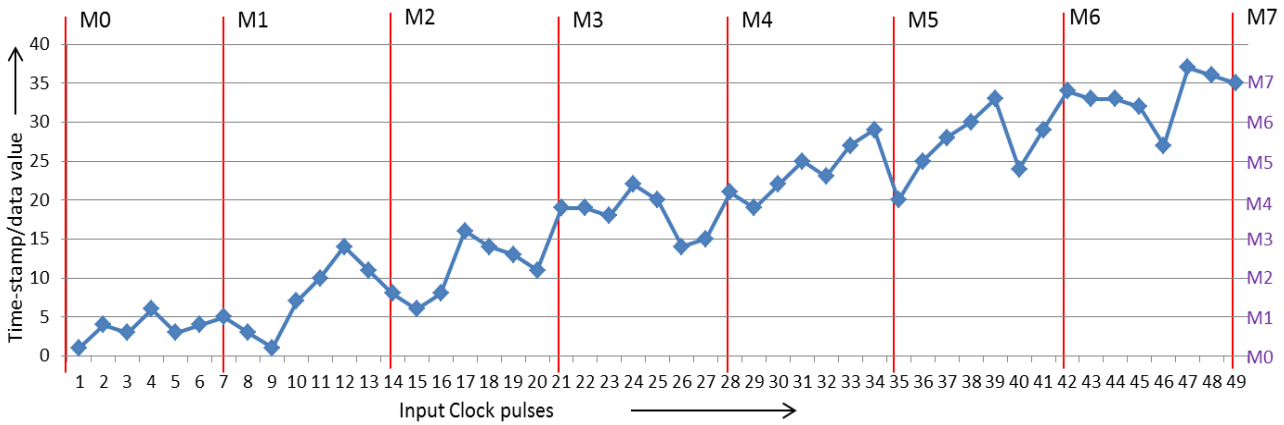




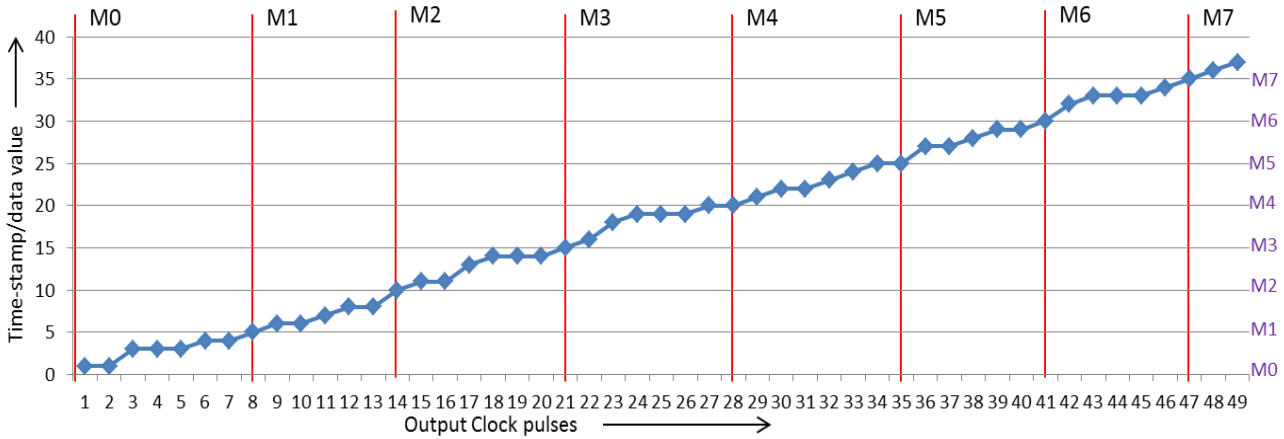
Ref: HK 20.5 for GBTx

4. Outlook

2) Real-time data sorting



Input data



Output data

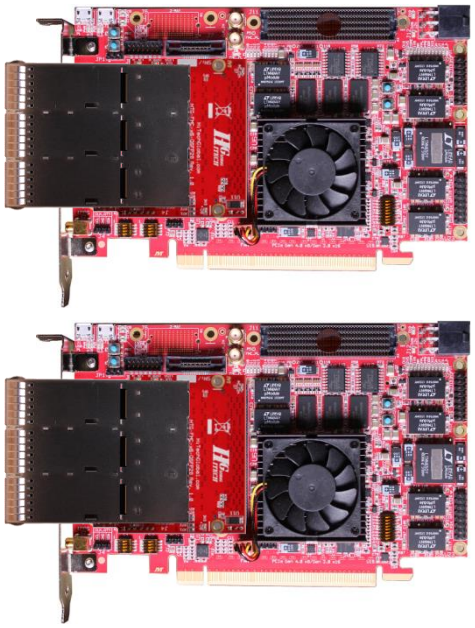
Reason to sort:

1. Epoch message are sorted by GET4
2. The sequence of Hit message is disrupted when the state machine of GET4 read data from different channels.

Ref: [4]J. Saini, S. Mandal, A. Chakrabarti, S. Chattopadhyay, A real time sorting algorithm to time sort any deterministic time disordered data stream. Journal of Instrumentation. 2017, 12: P12023.

4. Outlook

3) DAQ based on CRI



Infiniband Net

CRI = AFCK + FLIB

Ref: HK 20.5 for CRI

Thank you!

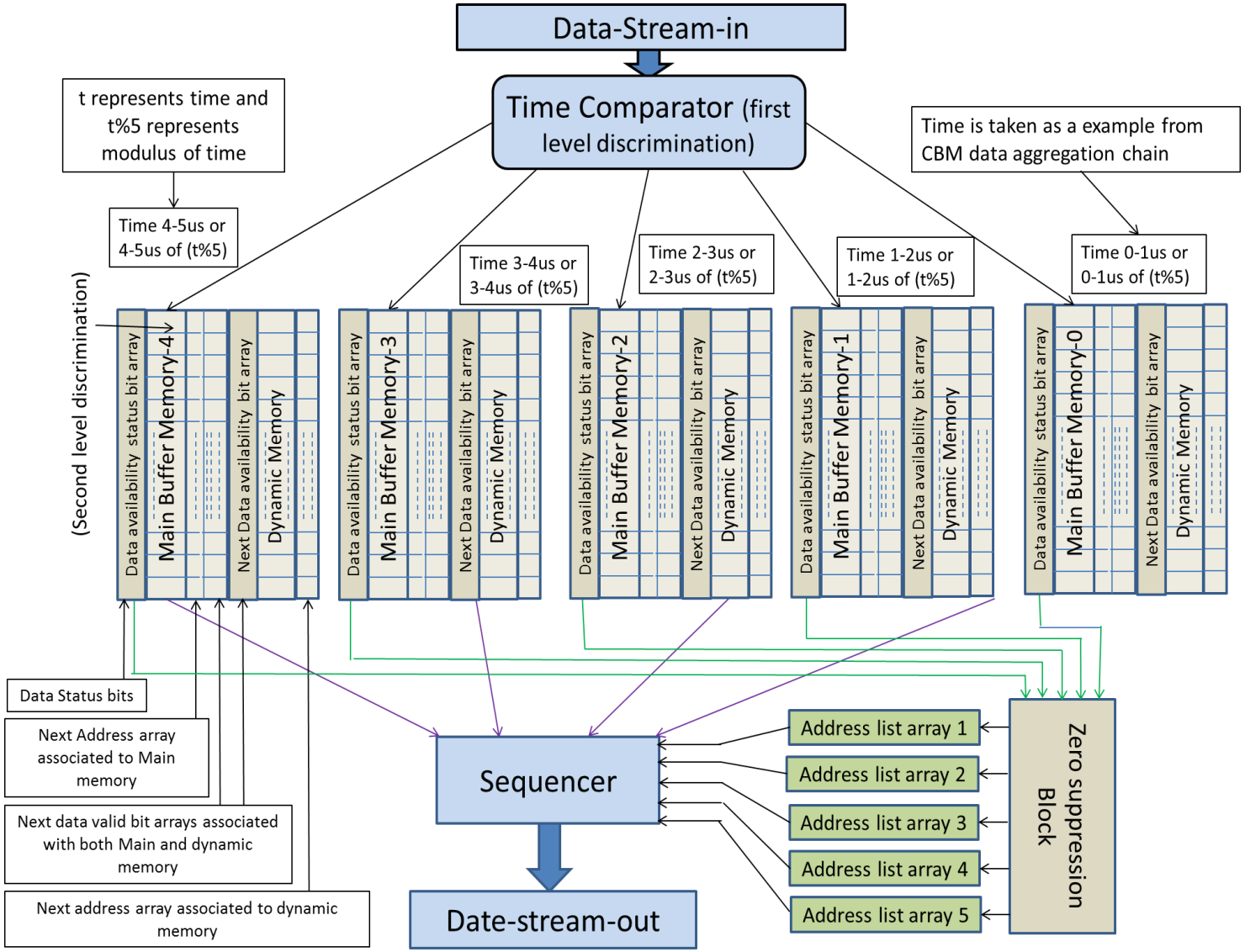
Backup

- SimplifiedMS
- 1. Each GET4 has their own epoch event.
- 2. Epoch event from GET4 are used directly.
- RealMS
- 1. All GET4 share one same epoch.
- 2. Hit message must be sorted at first.

Time Slices

- Time is the only way to organize data at DAQ level
- Events {'one interaction'} are defined during reconstruction
- → Time slice building instead of 'event building'
- Requirements for time slice building
  - collect all data of a time slice in one compute node
  - adjacent time slices must have some small overlap
    {otherwise interactions at the slice boundary can not be reconstructed}
- Efficient solution
  - define a micro slice, length few µsec
  - macro slice is build from micro slices
    {e.g. 100 mirco slices with 1 micro slice overlap}

Backup


Data-Stream-in
Time Comparator (first level discrimination)
t represents time and t%5 represents modulus of time
Time is taken as a example from CBM data aggregation chain
Time 4-5us or 4-5us of (t%5)
Time 3-4us or 3-4us of (t%5)
Time 2-3us or 2-3us of (t%5)
Time 1-2us or 1-2us of (t%5)
Time 0-1us or 0-1us of (t%5)
(Second level discrimination)
Data availability status bit array
Main Buffer Memory-4
Next Data availability bit array
Dynamic Memory
Data availability status bit array
Main Buffer Memory-3
Next Data availability bit array
Dynamic Memory
Data availability status bit array
Main Buffer Memory-2
Next Data availability bit array
Dynamic Memory
Data availability status bit array
Main Buffer Memory-1
Next Data availability bit array
Dynamic Memory
Data availability status bit array
Main Buffer Memory-0
Next Data availability bit array
Dynamic Memory
Data Status bits
Next Address array associated to Main memory
Next data valid bit arrays associated with both Main and dynamic memory
Next address array associated to dynamic memory
Sequencer
Date-stream-out
Address list array 1
Address list array 2
Address list array 3
Address list array 4
Address list array 5
Zero suppression Block