# Single-Photon Timing Resolution in Digital Silicon Photomultipliers

#### **<u>E. Venialgo<sup>1</sup></u>**, J.-F. Pratte<sup>2</sup>, S. Brunner<sup>3</sup>, and E. Charbon<sup>4</sup>

<sup>1</sup>Applied Quantum Architectures department, Delft University of Technology, Delft, Netherlands. <sup>2</sup>Department of Electrical and Computer Engineering, Université de Sherbrooke, Sherbrooke, QC, Canada. <sup>3</sup>Radiation Science & Technology department, Delft University of Technology, Delft, The Netherlands. <sup>4</sup>Advanced Quantum Architecture Laboratory, EPFL, Lausanne, Switzerland.



#### Main objective of this talk

#### Discuss and propose a standardization methods for SPTR measurements in <u>Digital SiPMs</u>

# Outline

- Definition of SPTR
- Digital SiPM architectures
- Setup examples
- Parameters and standardization
- Conclusions









### **Conditions and techniques**

- Single-photon light level
- Uniform illumination over the sensitive area
- **TCSPC** measurement technique

511 keV Gamma Photon

SCINTILLATOR









#### **Digital SiPM architectures**

#### **Digital SiPM concepts**

digital photon counter (DPC)



1 time stamp

T. Frach et al., NSSMIC 2009

### **Digital SiPM concepts**

digital photon counter (DPC)

Multichannel digital SiPM (MD-SiPM)



T. Frach et al., NSSMIC 2009 S. Mandai et al., NSSMIC 2012

# **Digital SiPM concepts**

digital photon counter (DPC)

3D digital SiPM (3DdSiPM)

#### Multichannel digital SiPM (MD-SiPM) SPAD SPAD SPAD 26x16 SPAD 6400 SPADs **SPADs** o digital ime to di converter ching Cuit Time to digital Quenching converter Circuit Quenching ircuit 1 SPAD per TDC 48 TDC TDC N individual time stamps 48 **individual** time stamps 1 time stamp

T. Frach et al., NSSMIC 2009

S. Mandai et al., NSSMIC 2012 Pratte et al. 3DIC-IEEE 2010

# **Digital Photon Counter (DPC)**

T. Frach et al., NSSMIC 2009



S. Brunner et al., JINST 2016

TDC bin size: 24 ps

circuitry

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#### 9x18 Array of MD-SiPMs 26x16 26x16 26x16 26x16 26x16 **SPADs SPADs SPADs SPADs SPADs** 9 x 18 26x16 26x16 26x16 26x16 26x16 **Pixels SPADs SPADs SPADs SPADs MD-SiPMs** 26x16 26x16 26x16 26x16 26x16 **SPADs SPADs SPADs SPADs SPADs** 432 TDCs



# 9x18 Array of MD-SiPMs architectural overview

- a 2D 9x18 MD-SiPM array.
- 9 TDC banks with each having 48 TDCs..
- configuration memory and masking registers.
- readout logic and discriminator.



Augusto Carimatto; Shingo Mandai; Esteban Venialgo; Ting Gong; Giacomo Borghi; Dennis R. Schaart; Edoardo Charbon. ISSCC, 2015

# **3D digital SiPM**

#### **3D Integration**

- high fill factor
- heterogeneous technologies integration

Teledyne Dalsa\_ Custom process

TSMC CMOS 65 nm—

256 SPAD readout ASIC Pratte et al. 3DIC-IEEE 2010



# **Digital SiPM overview**



#### Setup examples

#### picosecond Laser



Advaced laser diode systems. EIG1000 AF. Head: PiL040F, 405 nm, SANYO laser diode DL-5146-152



#### **MD-SiPM**

- bias voltage
- temperature
- DCR



#### readout FPGA

- CLK source
- STOP/START



- ML507 Xilinx, Virtex-5
- human data [XCM-206Z]Xilinx Spartan-6 FGG676
- custom Microsemi AGL1000V2-CS281 board

#### acquisition computer

- KDE
- measurement error
- calibration procedures



- custom USB-2.0 interface
- ethernet 1Gbps
- matlab/Linux



synchronization signal

#### **SPTR measurement MD-SiPM**



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<u>reference PIN diode</u> Becker & Hickl PHD-400 200 ps rise time





<u>free space beam propagation</u> high-end Newport mirrors for ultrafast laser





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output signals

SMA cable (ref diode and DUT) oscilloscope

- LeCroy SDA 6000A 20 GS/s, 6 GHz
- Keysight MSOX91304A 80 GS/s, 13 GHz



### **Beam conditioning setup**



- neutral density filters (photon starved)
- beam focusing (down to ~2um spot size)
- XYZ motorized stage (array sweep, ~1um step)







# **Typical SPTR acquisition**



#### <u>Setup jitter</u>

- PIN ref diode pulse to pulse jitter
- include electronic jitter (SMA, scope)
- include Mai Tai / OPO pulse to pulse jitter (negligible)
- Value : 3-4 ps FWHM

- A SPAD SPTR acquisition
- time delay between the SPAD output (pink) and the ref. signal (blue)
- histogram building (100k events)
- FWHM extract

$$\sigma_{\text{mesured}}^2 = \sigma_{\text{setup}}^2 + \sigma_{\text{detector}}^2$$



#### **SPAD + front-end SPTR**

- TSMC 65 nm
- SPAD implemented for test purpose (and fun)
- 20 µm diameter





### **DPC SPTR (measurement setup)**



DPC	Active	Temp.	Inactive	SPTR	System
	area	$[^{\circ}C]$	cells [%]	FWHM [ps]	TR FWHM [ps]
3200	die	0	0	187 ±5.9	47 ±1.9
3200	die	0	20	$168 \pm 3.0$	$42 \pm 0.8$
3200	die	0	50	$153 \pm 2.3$	$45 \pm 0.6$
3200	pixel	10	20	$101 \pm 2.8$	16 <b>±</b> 2.4
3200	pixel	20	20	$113 \pm 3.5$	14 ±3.1
6400	die	0	20	$247 \pm 3.0$	$40 \pm 0.4$





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Masking level								

S. Brunner et al., JINST 2016

#### **Parameters and standardization**

readout quenching circuit operation event detection circuit discriminator mode masking memory bias voltages quenching circuit **TDC:** timing line: detection circuit single-shot resolution detection circuit masking memory range bias voltages threshold LSB bias voltage INL/DNL quenching circuit

detection circuit masking memory bias voltages







#### **Common architectural components**

- Time-to-digital converters (LSB, INL, DNL, SSR)
  - several TDCs: best, worst, and median
- Operation mode
  - event discriminator, triggering system, reset system, measurement range
- SPAD-cell operation
  - masking [%], excess bias, quenching, TH, activated area
- Timing line settings and characterization
  - inverter, comparator TH, preamplifier

### **Timing measurement (setup)**



### **Timing measurement (setup)**



#### **Common setup components**

- Optical components
  - light attenuator (SPAD rate, single-photon level)
  - light diffuser (uniformity). SPAD camera measurement
  - etc
- Laser system
  - pulse width, wavelength, CLK jitter, repetition rate
- D-SiPM controller and synchronization system with respect to the laser pulse
  - optical/electrical
- Measurement conditions: temperature, power, heatsinks, etc

### Conclusions

- Digital SiPM standardization relies on two main aspects: the <u>D-SiPM architecture</u> and the <u>measurement setup</u>
- In a standardization procedure, the common architectural parameters are established and specific features related to timing are also reported.
- The measurement setup can be divided into two types: high timing resolution (<100 ps) and standard timing resolution (>100 ps)

# Acknowledgments

- Swiss National Science Foundation
- STW
- 3IT
- RAMS
- NSERC CRSNG
- CMC MIcrosystems
- RESMIQ
- CANADA FIRST
- Fonds de recherche nature et technologie Québec

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