Test Measurements with the Hit-Detection ASIC V2.00 for the APFEL Preamplifier

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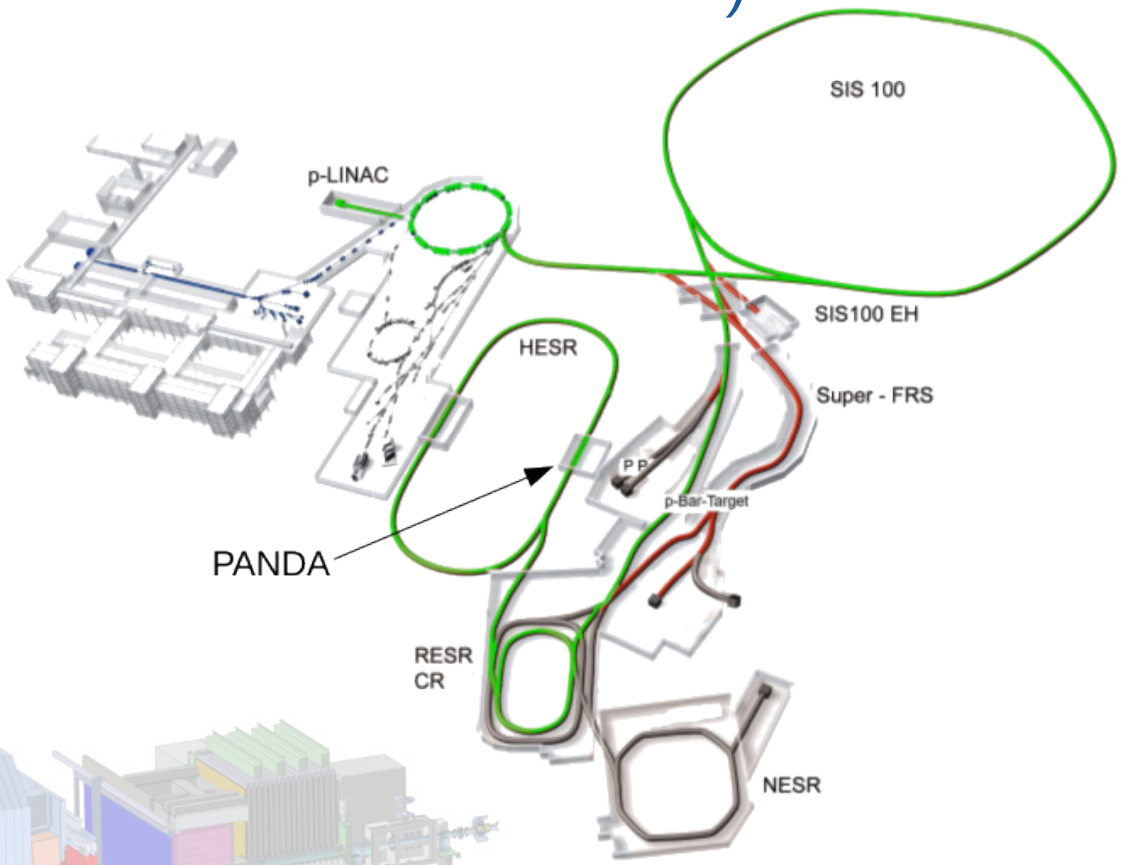
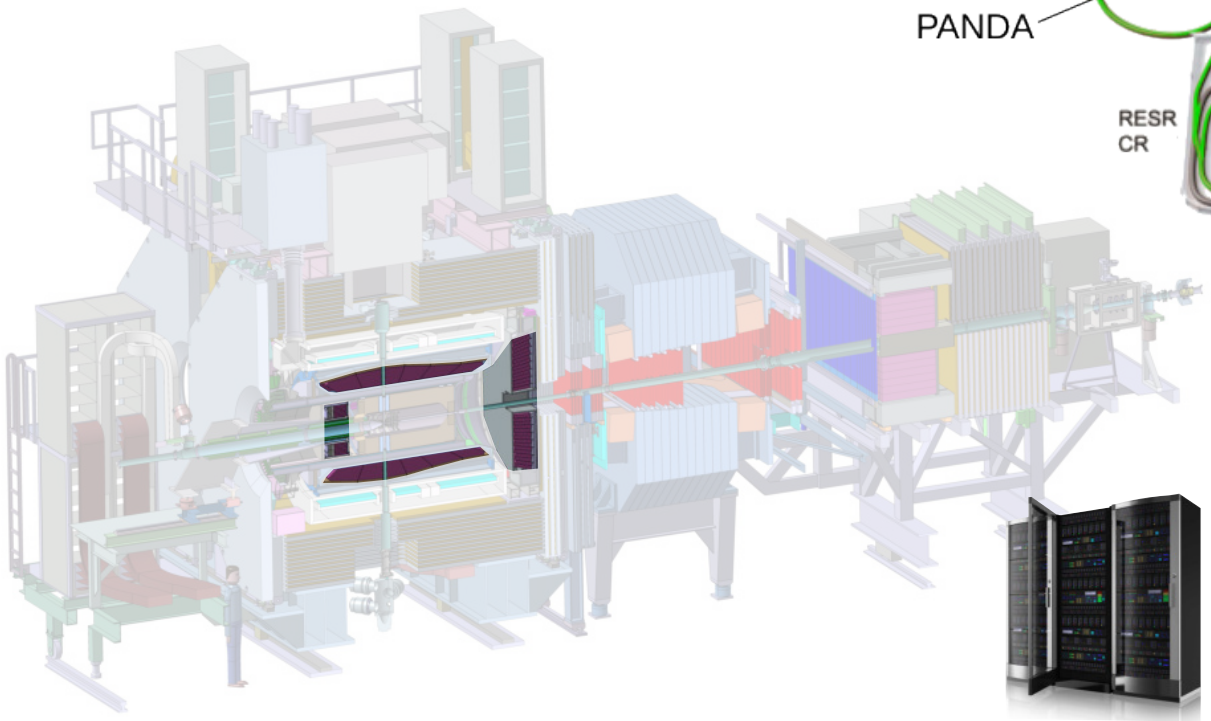
Helmholtz-Institut Mainz

$\bar{\text{P}}$ANDA Collaboration Meeting 18/1
7. March 2018

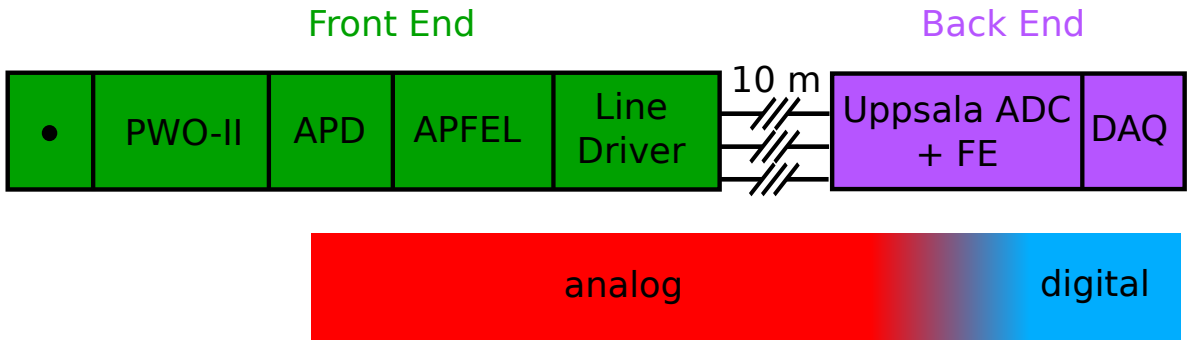
FAIR (Facility for Antiproton and Ion Research)





Data Readout Chain: Sampling ADC Board

"Uppsala ADC Design":



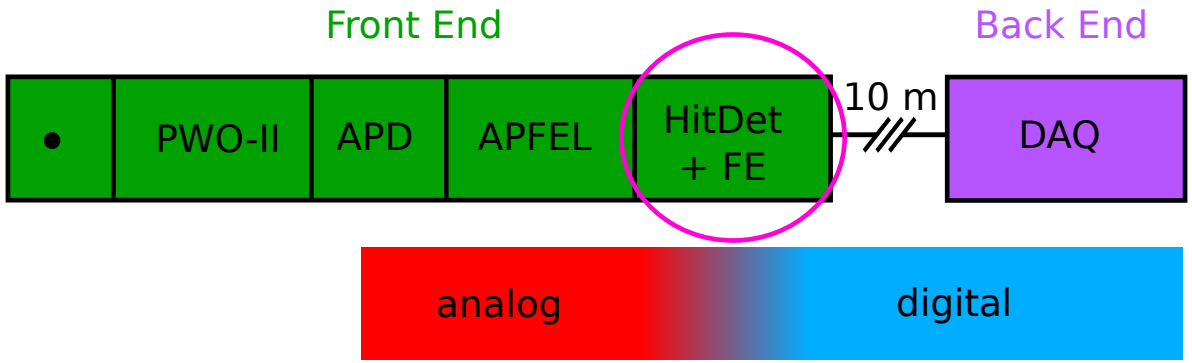
- PWO-II: Lead tungstate scintillator
- APD: Avalanche Photodiode
- APFEL: Charge sensitive preamplifier
- FE: Feature Extraction
- DAQ: Data Acquisition

Challenging Cable Guiding

[M. Moritz: Barrel slice assembly, PANDA CM, September 2017]

Data Readout Chain: Possible Design

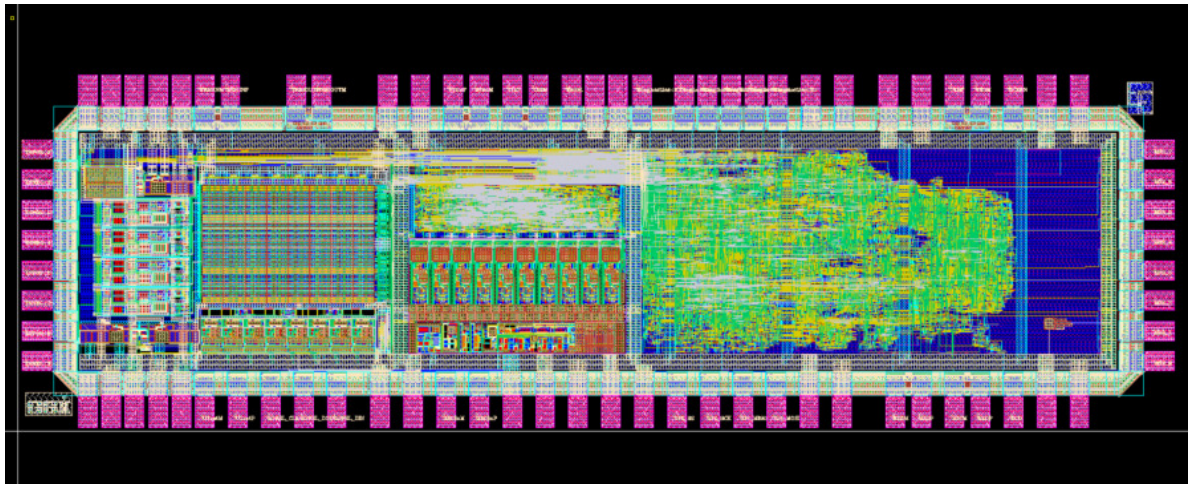
"Hit-Detection Design":



- PWO-II: Lead tungstate scintillator
- APD: Avalanche Photodiode
- APFEL: Charge sensitive preamplifier
- FE: Feature Extraction
- DAQ: Data Acquisition

Hit-Detection ASIC V2.0

- Developed at GSI (H. Deppe, H. Flemming and P. Wieczorek)
- Hit-Detection ASIC V2.0 consists of
  - Analogue part (Buffer, Trigger, Memory, Integrator, Multiplexer)
  - Pipeline ADC (12 bit)
  - Digital part (Write and read out logic, Backend)
- Front End

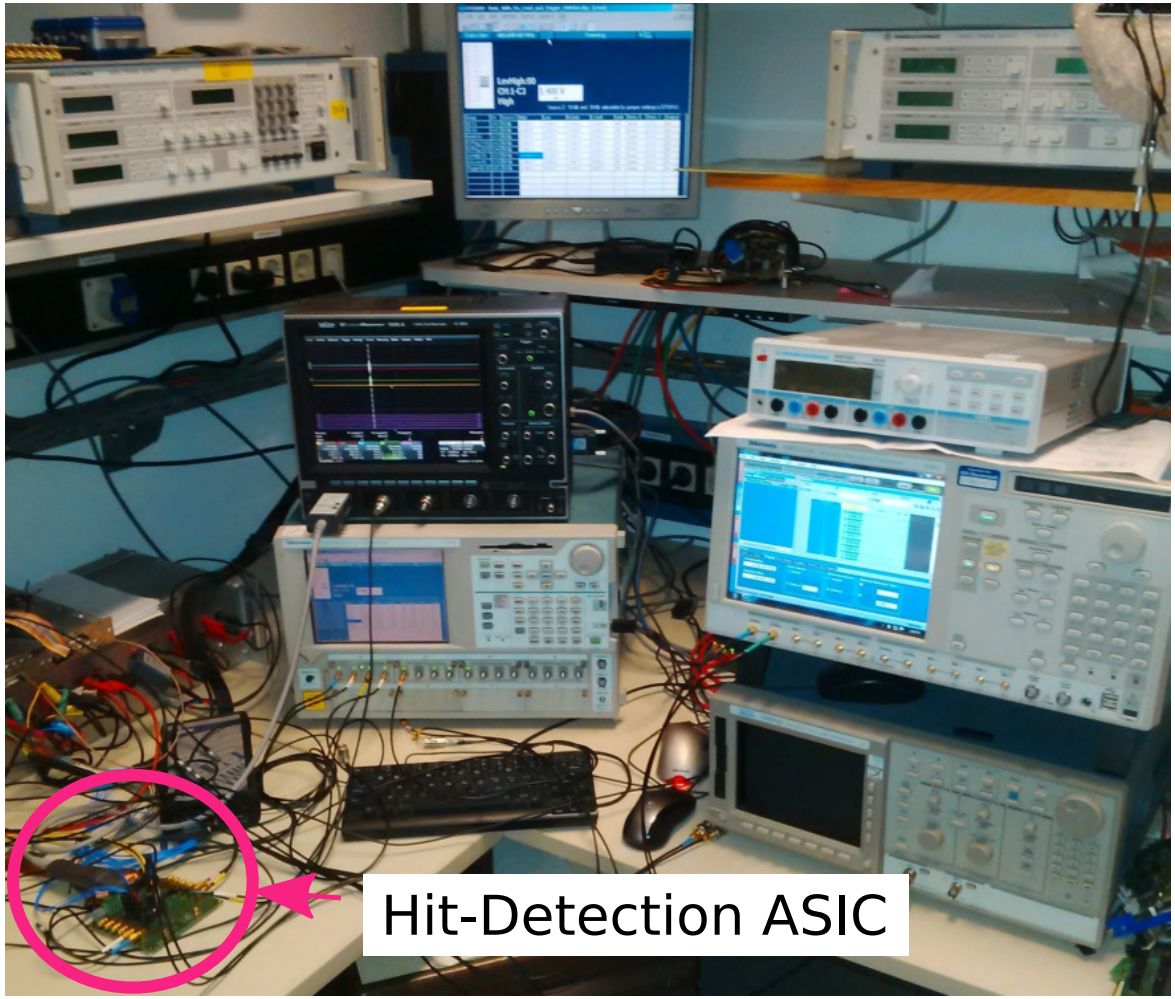


[H. Deppe, H. Flemming, P. Wieczorek:
The HitDetection ASIC - Version 2.00, 31.08.2016]

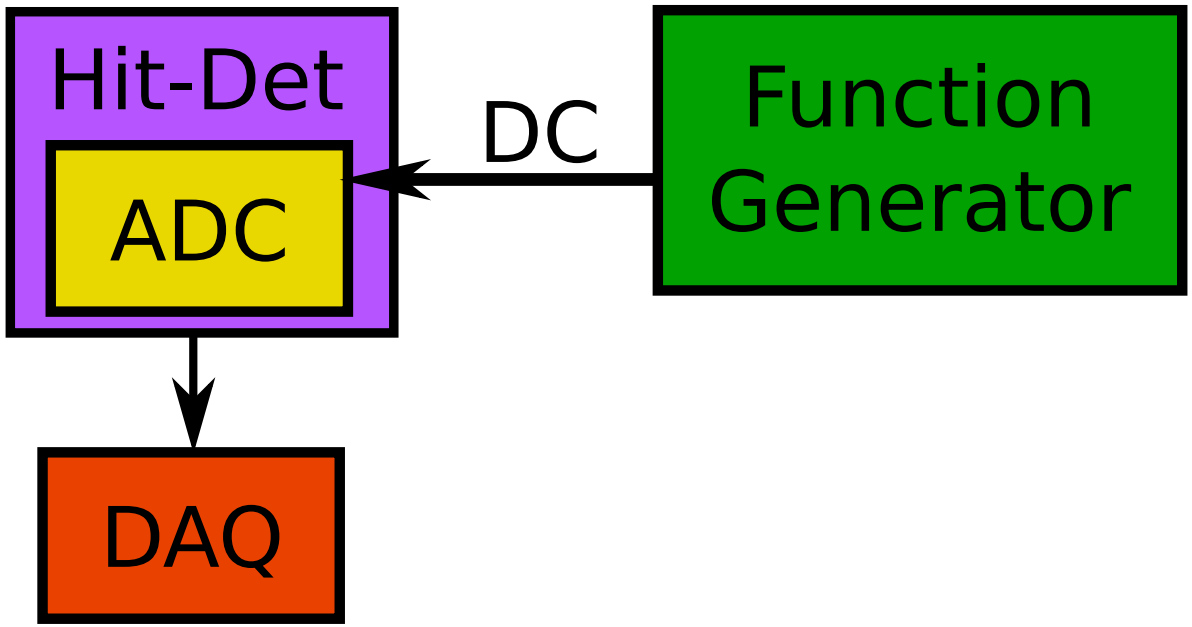
Teststand with automated measurements

Measurements:

- ADC: Linear performance
- ADC: Dynamic performance
- Analog Memory
- Threshold Trigger

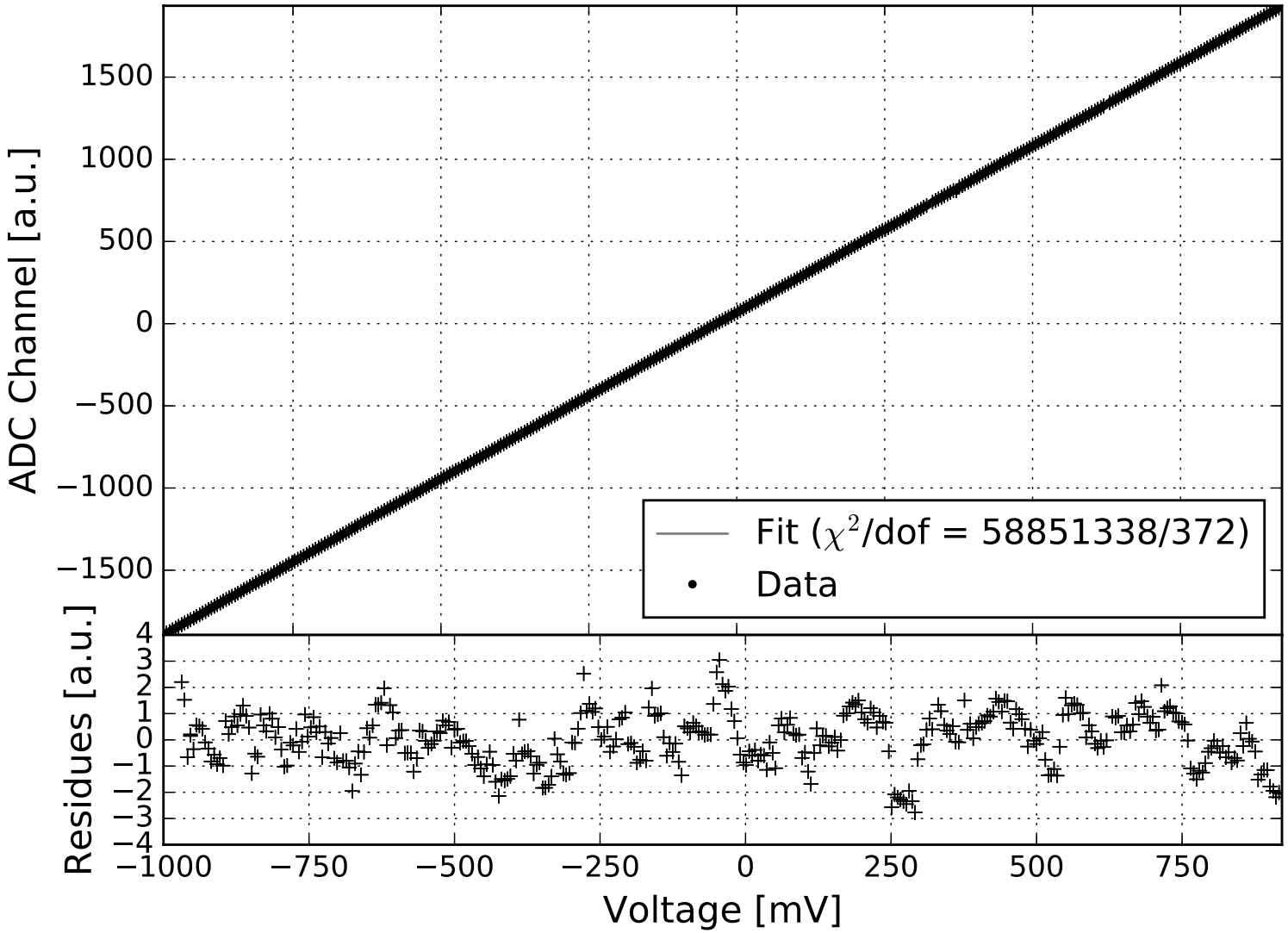


ADC: Linear Performance



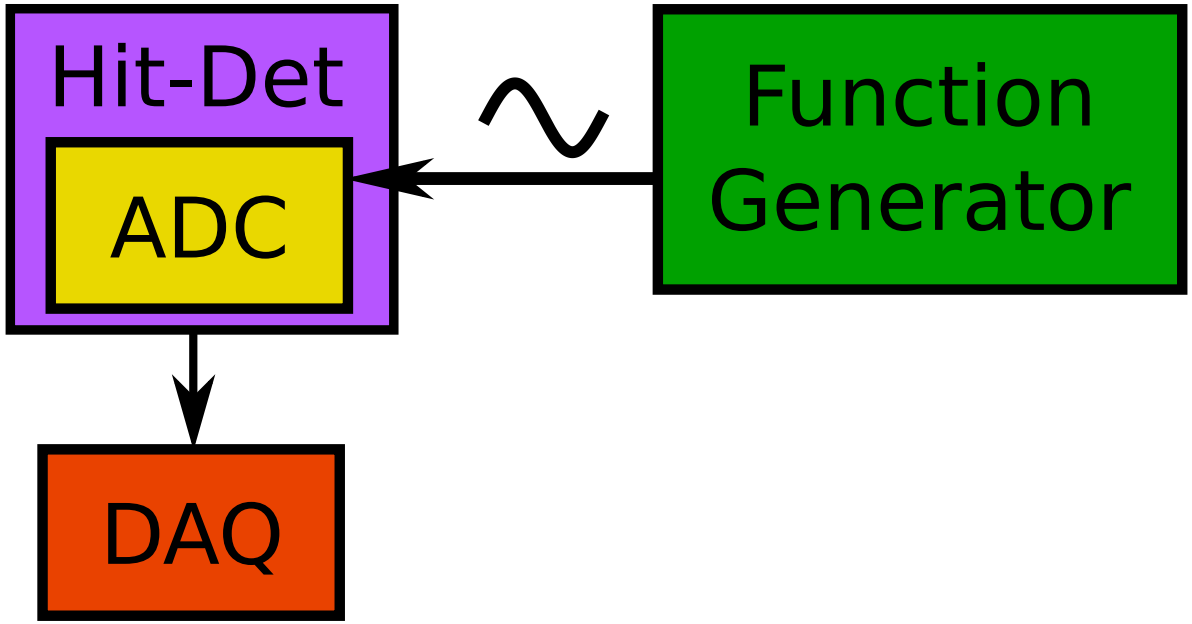
→ Ramping DC voltage through ADC input range
→ Retrieving the integral nonlinearity (INL)

ADC: Linear Performance



INL = 2.26 LSB

ADC: Dynamic Performance



→ Different input frequencies, amplitudes & sampling rates

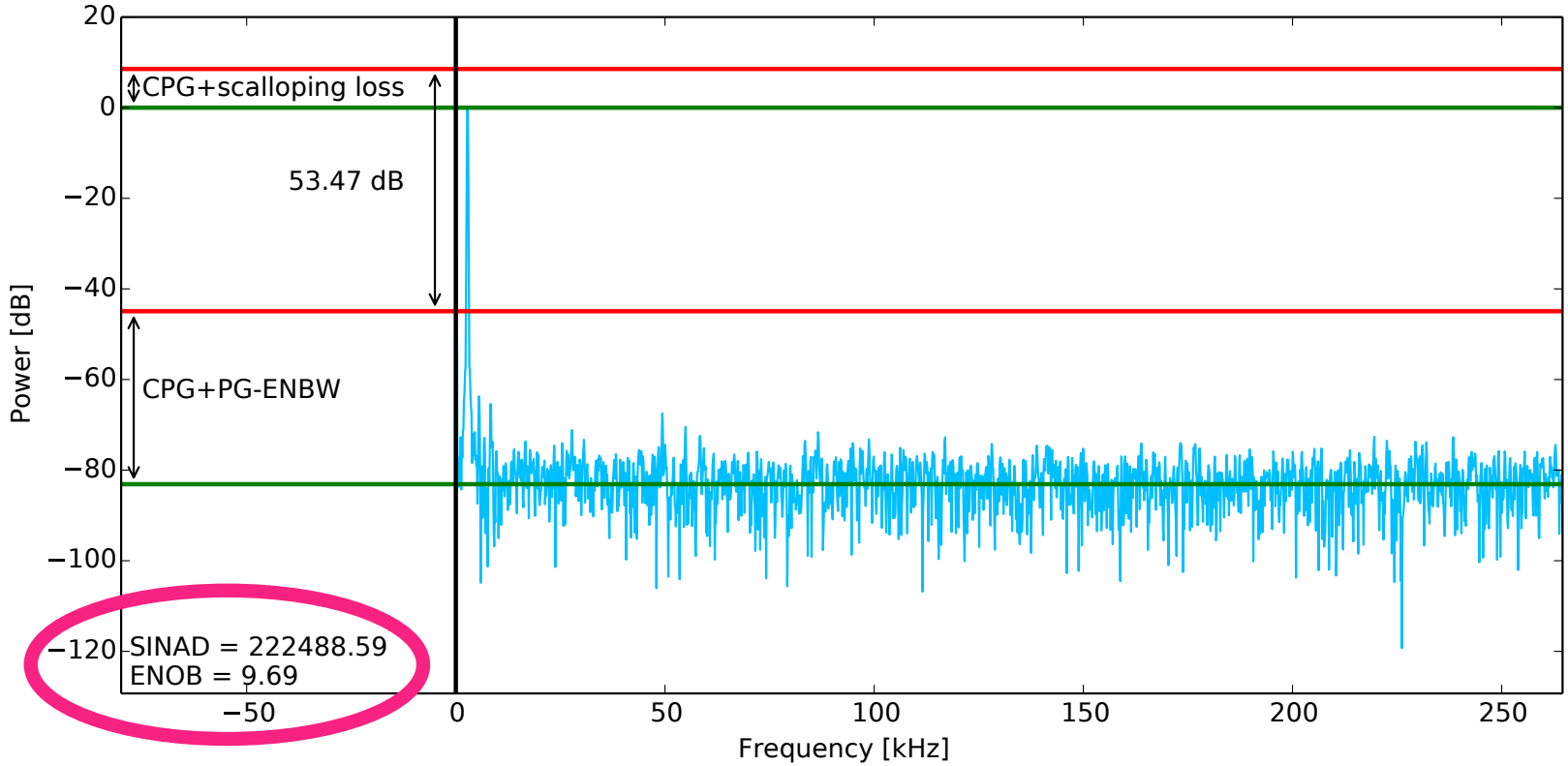
→ Retrieving the effective number of bits (ENOB):

$$ENOB = 0.5 log_2(SINAD) - 0.5 log_2(1.5) - log_2(Ampl/FS)$$

(*SINAD*: Signal to Noise and Distortion;
Ampl: Amplitude; *FS*: Full Scale)

I: FFT-Method for obtaining ENOB

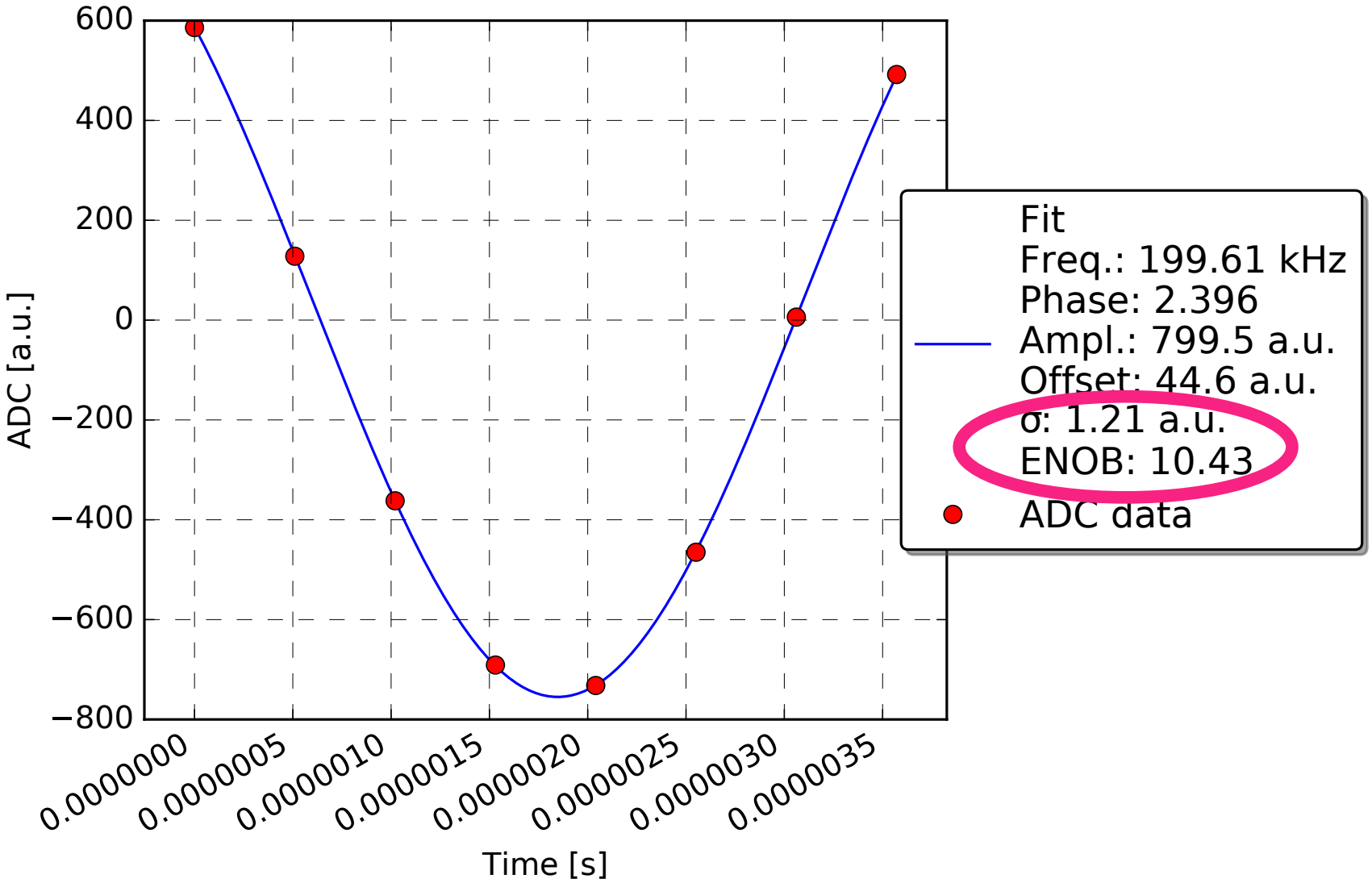
Number of samples: 2^{12}; input frequency: 3 kHz;
sampling rate: 529.1 kS/s; half amplitude



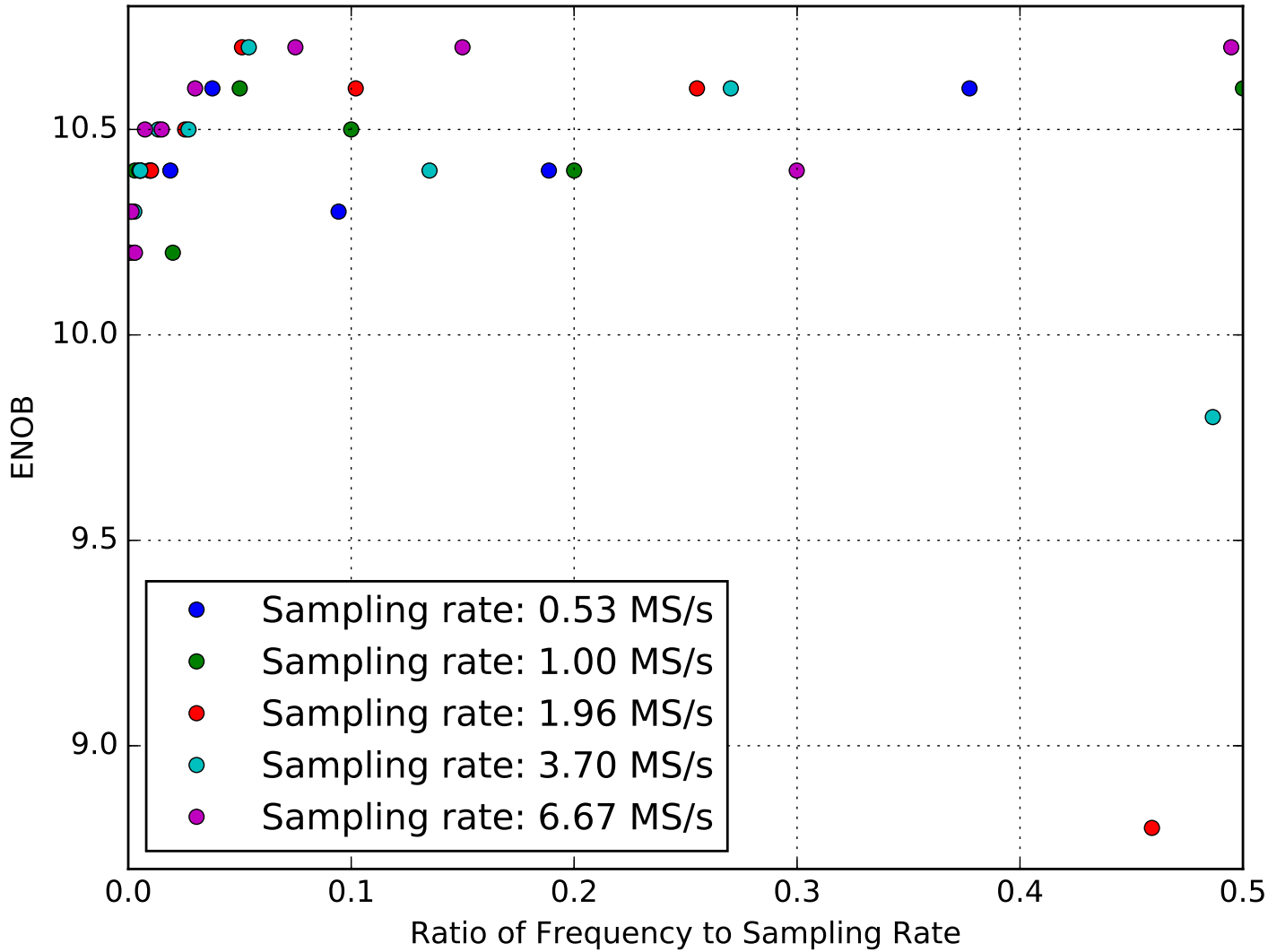
- **CPG**: Coherent Power Gain (influence of tapering function)
- **Scallopping Loss**: FFT sampling not appropriate
- **PG**: FFT Process Gain (Signal/Noise $\propto$ N)
- **ENBW**: Equivalent Noise Bandwidth (influence of tapering function)

II: Fit-Method for obtaining ENOB

Input frequency: 0.2 MHz; sampling rate: 1.96 MS/s; half amplitude

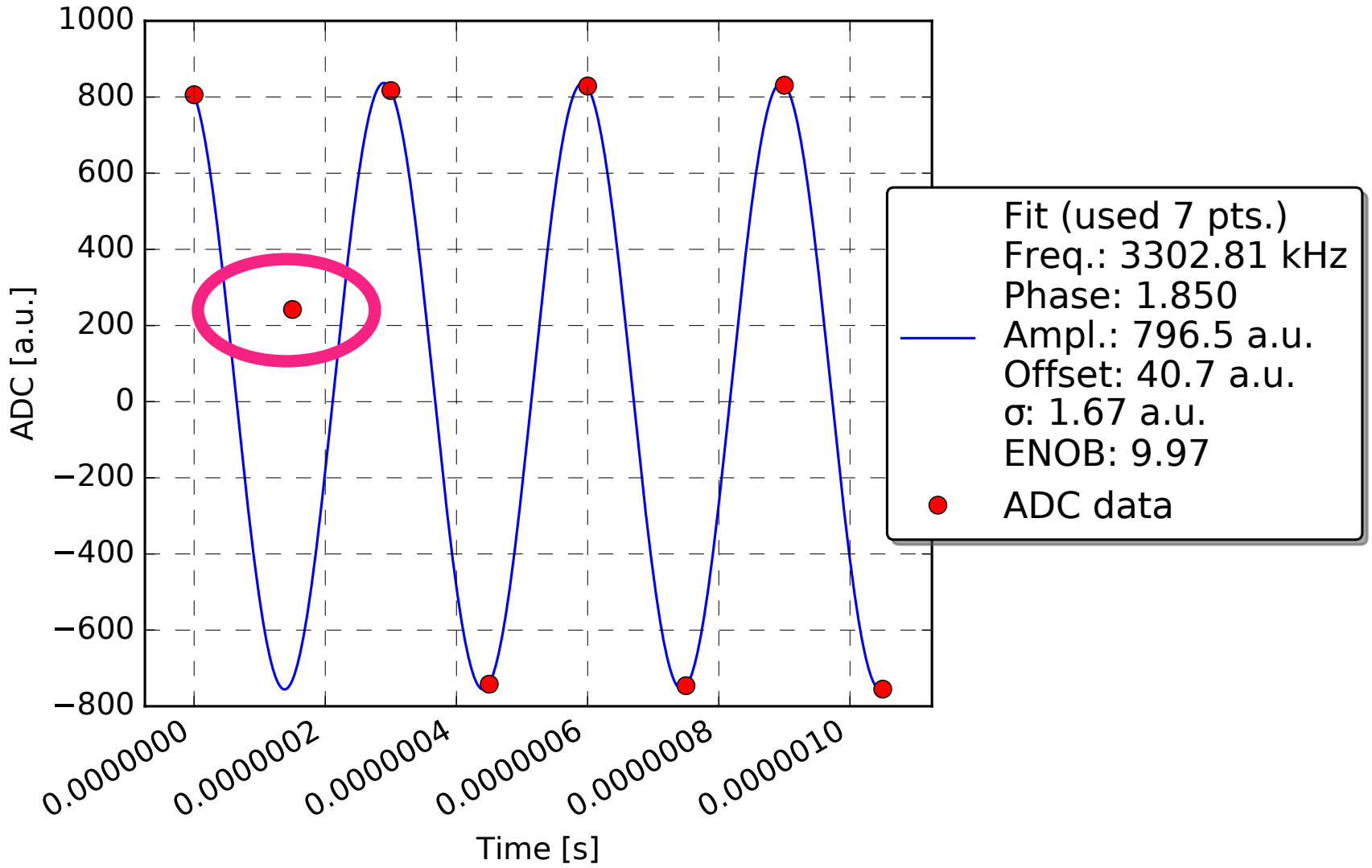


ENOB Comparison



It is not all roses

Input frequency: 3.3 MHz; sampling rate: 6.67 MS/s; half amplitude



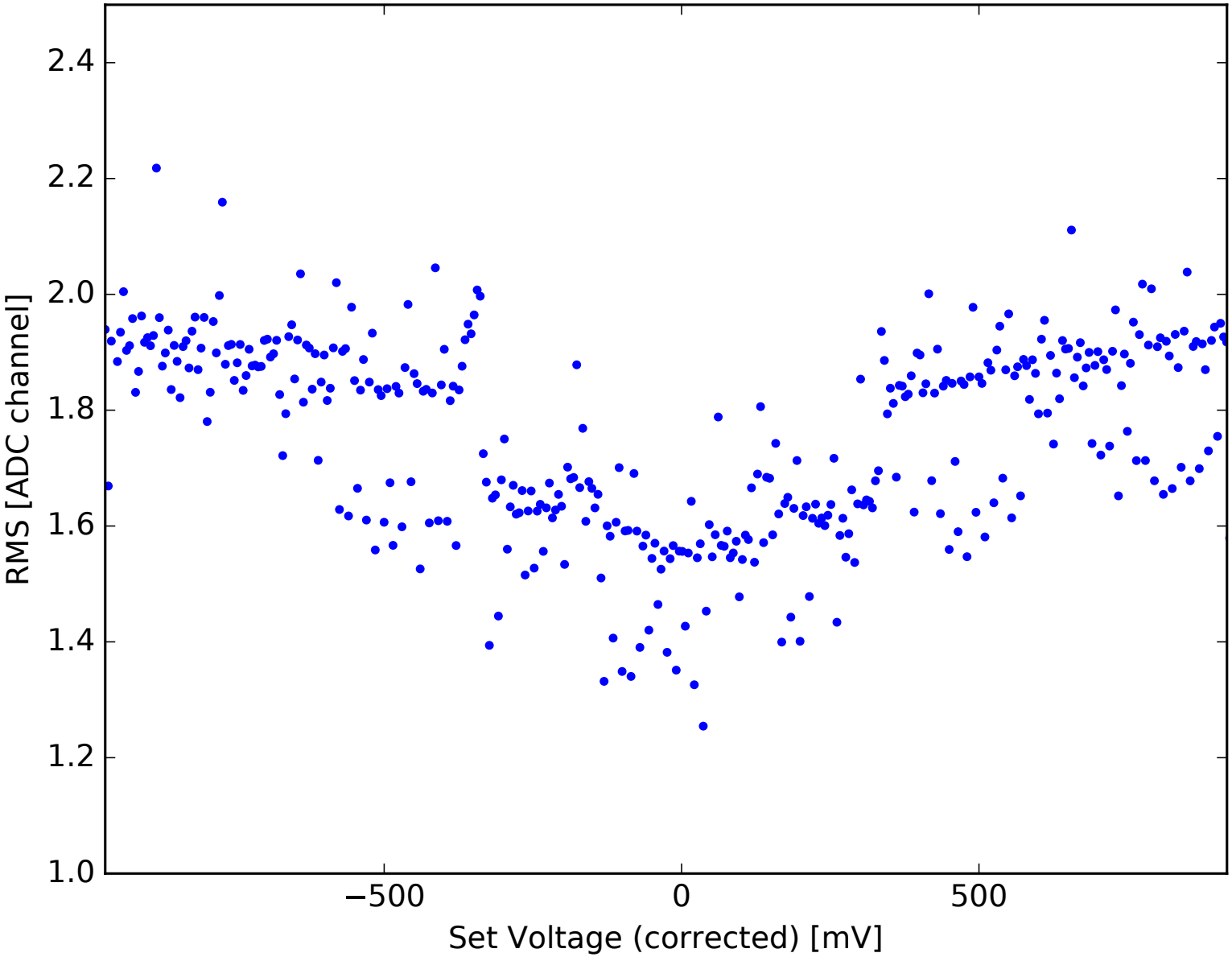
Summary and Outlook

- Teststand was set up including automatized measurements
- ADC has an INL of 2.26 LSB
- ADC has an ENOB of about 10
- ADC test board is beeing developed
  $\rightarrow$ Dynamic tests can be made with higher sampling rates
  $\rightarrow$ A feature extraction can be tested
- Limitations of current version were identified

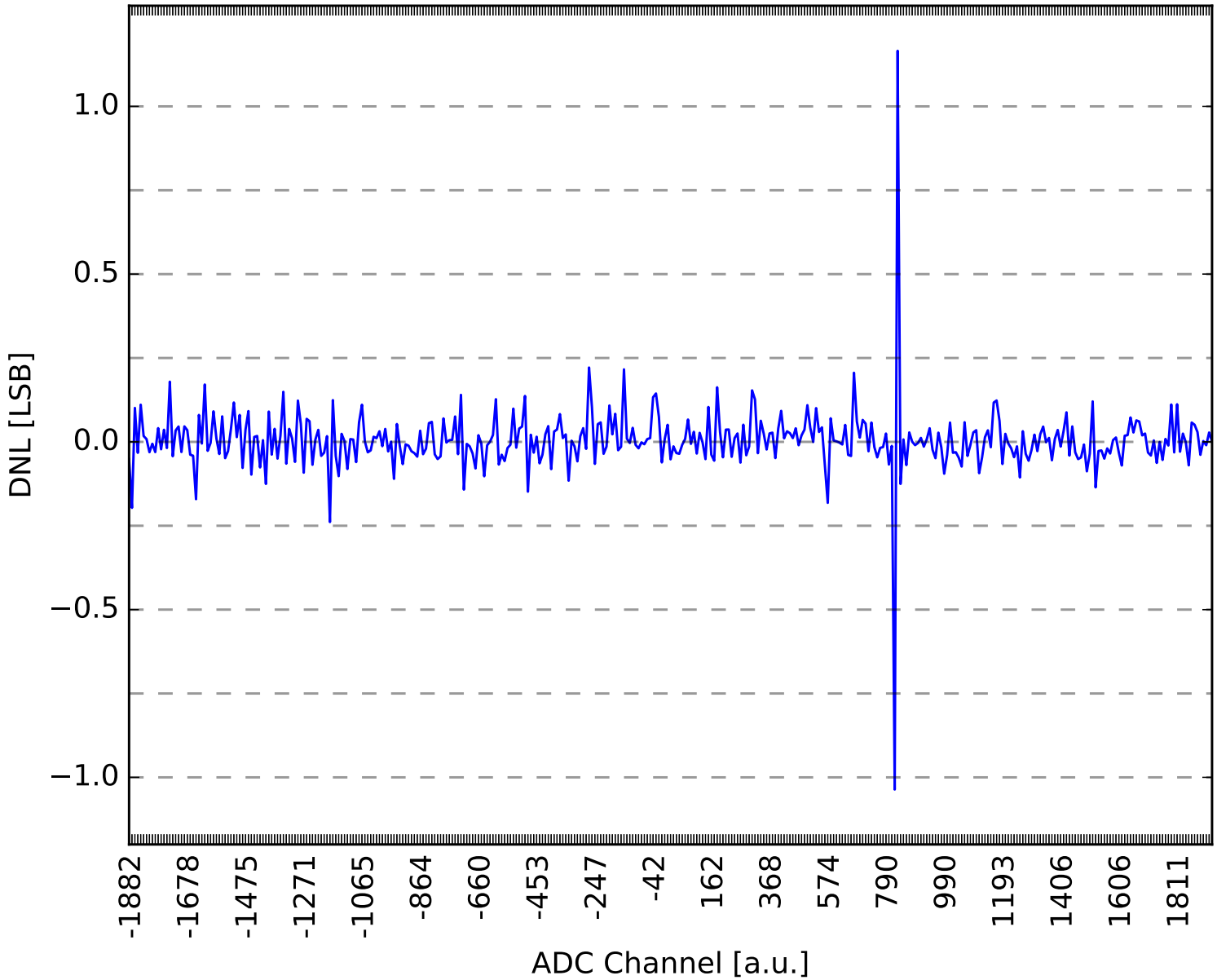
End

Thanks for your attention!

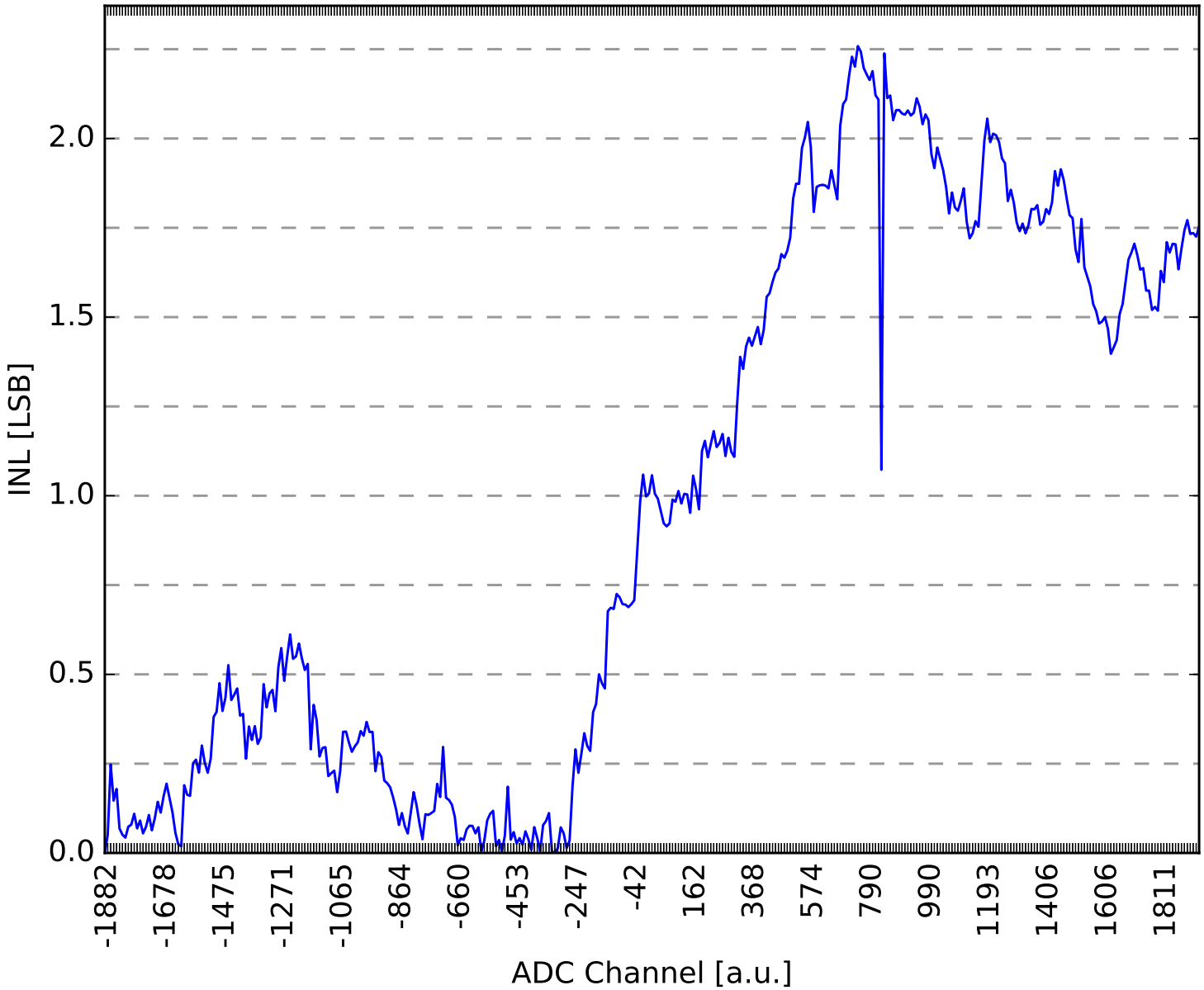
Effect of geometrical Layout



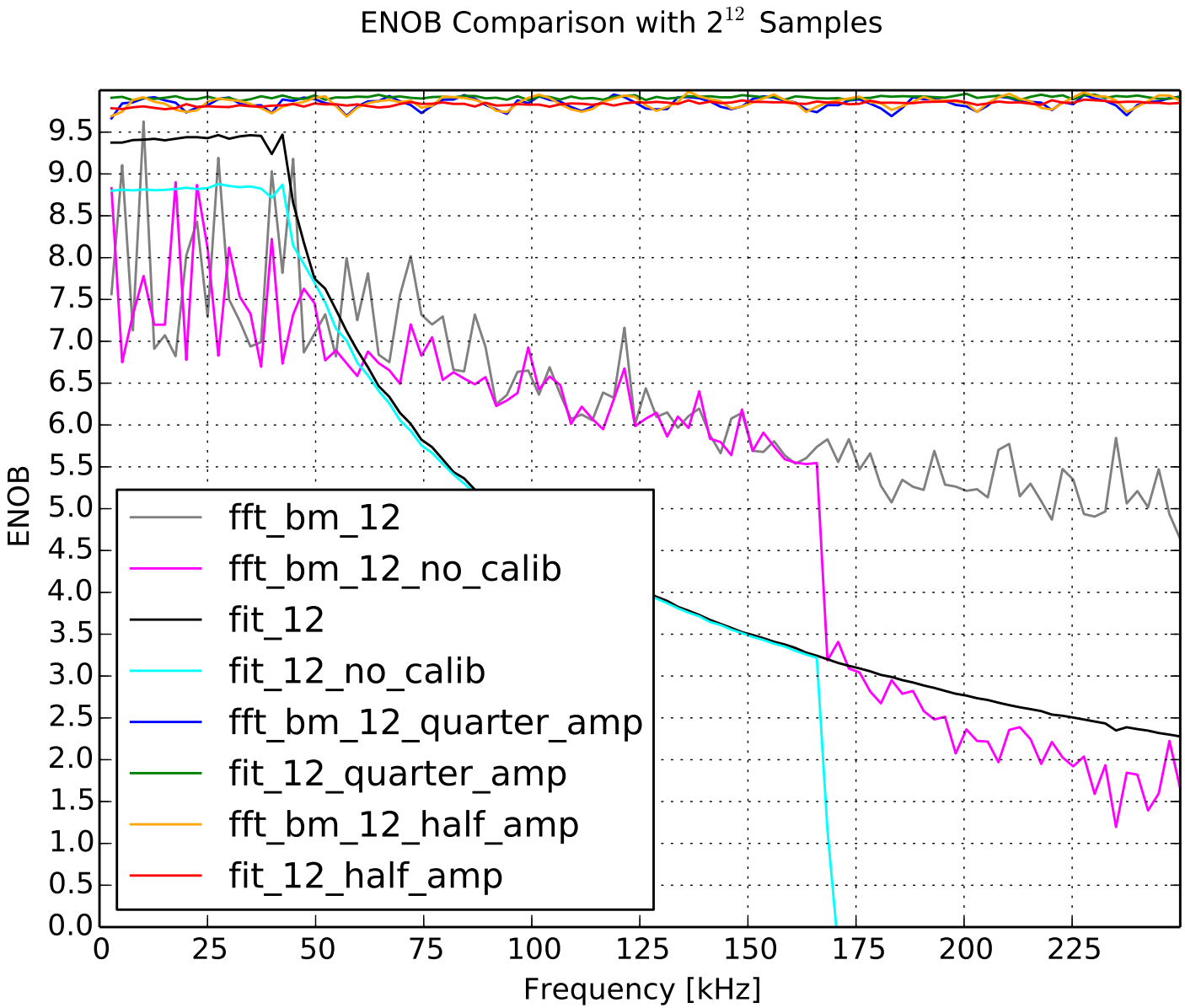
Differential Nonlinearity



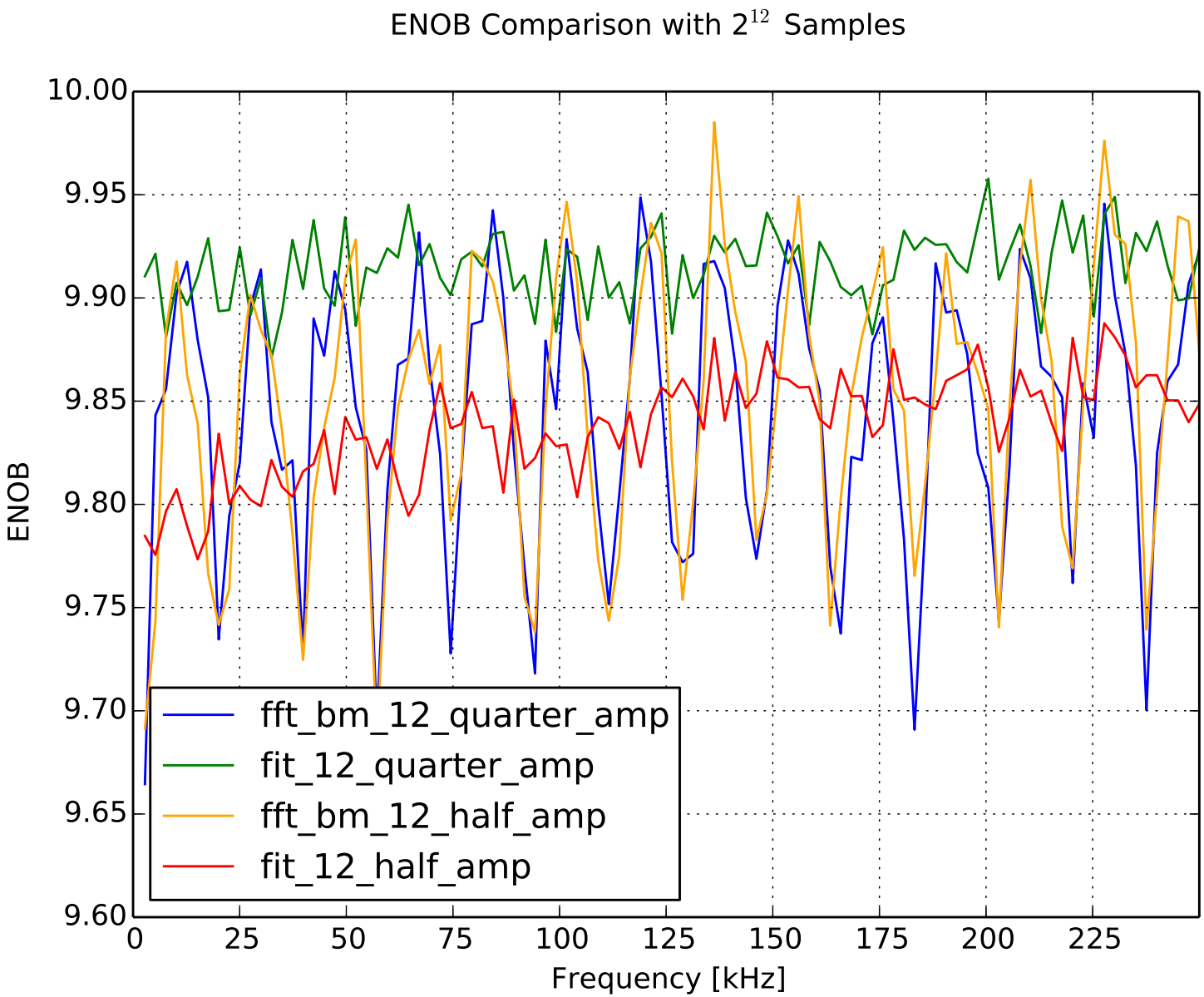
Integral Nonlinearity



Sampling Rate of 529 kS/s



Sampling Rate of 529 kS/s



ADC Dynamic

Two possibilities to obtain the Effective Number of bits (*ENOB*):

- Fit
- Fast Fourier Transformation (FFT)

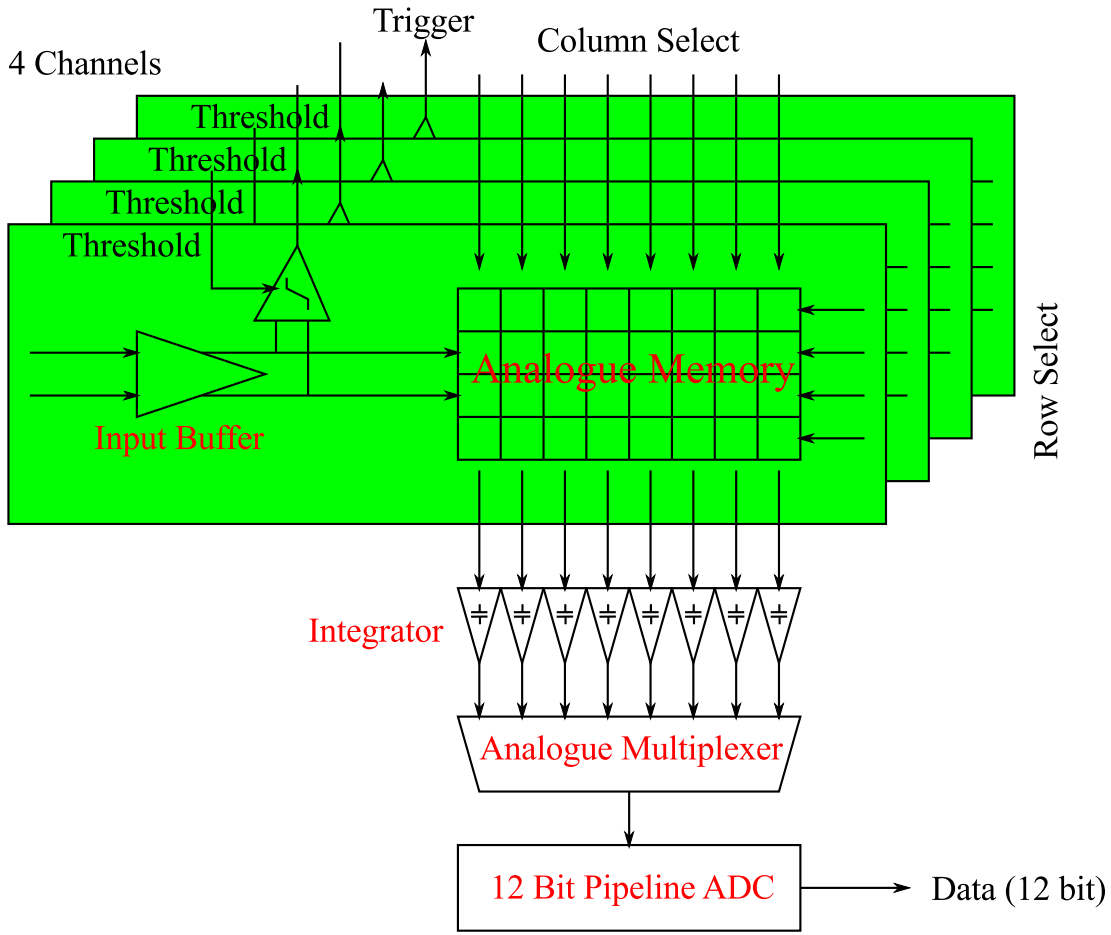
$$y_{\mathrm{Res}} = y_{\mathrm{ADC}} - y_{\mathrm{Fit}},$$
$$\sigma = \mathrm{std}(y_{\mathrm{Res}}),$$
$$S_N = 20 log_{10}\left(\frac{Ampl}{\sigma}\right),$$
$$SINAD = 10^{S_N/10},$$
$$ENOB = 0.5 log_2(SINAD) - 0.5 log_2(1.5) - log_2(Ampl/FS),$$

- $SINAD$: Signal to Noise and Distortion
- y_{Fit}: y_{ADC} corresponding value
- S_N: Signal-to-Noise
- y_{ADC}: ADC value
- $Ampl$: Amplitude
- FS: Full Scale

Analog Part

The analog part consists of 4 channels, each with

- Input buffer
- Threshold trigger
- Memory
- Integrator
- Multiplexer



[H. Deppe, H. Flemming, P. Wieczorek:
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