KVI

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GSI

Status of ASIC board development for Barrel EMC

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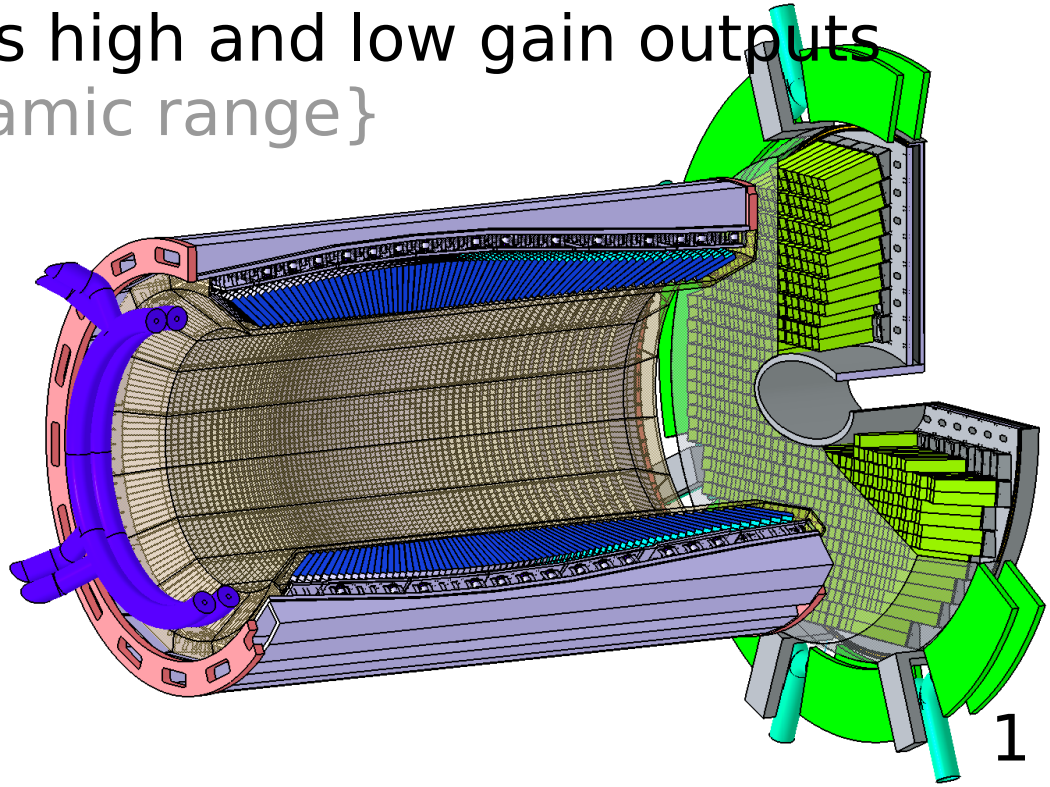
Barrel EMC

Construction summary:

- Barrel EMC consists of 11360 crystals
- Each crystal equipped with two LAAPDs {better light collection}
- Two LAAPDs are connected to one APFEL ASIC (hosts two independent preamplifiers)
- APFEL ASIC (two inputs) has high and low gain outputs (per each input) {high dynamic range}

ASIC integration challenges:

- ASIC power consumption
- Limited space

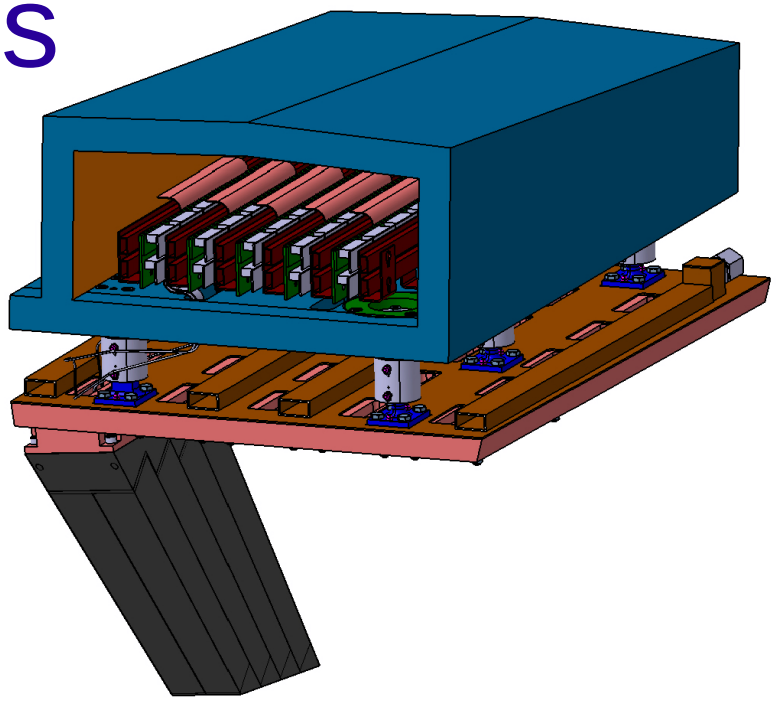


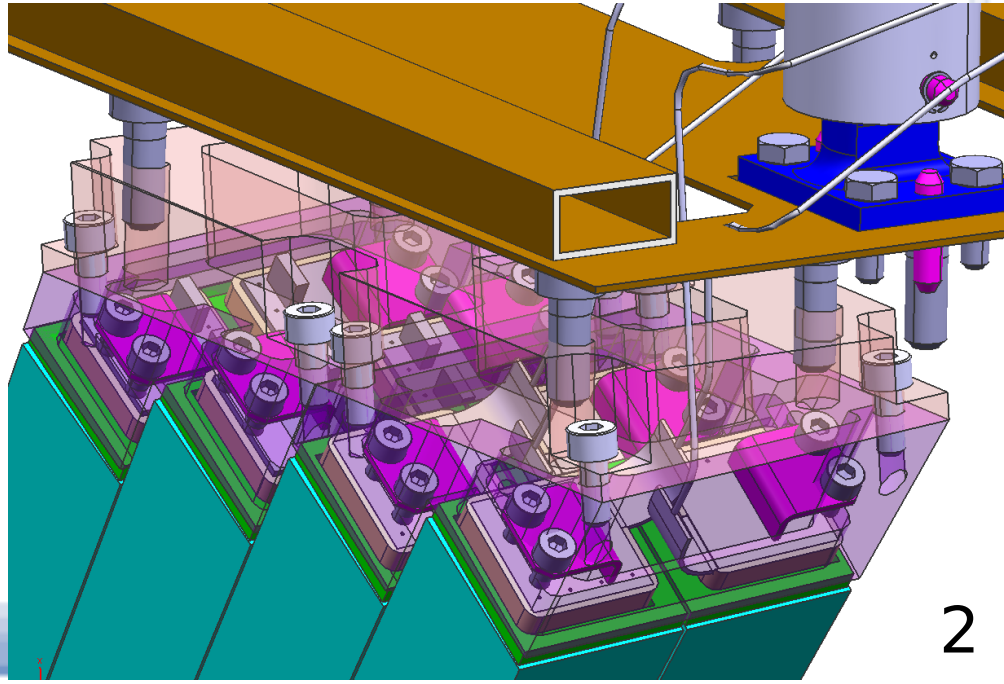
ASIC Integration Challenges

- To reduce ASIC power consumption APFEL has no low-ohmic line driver
- The space restriction/density of the ASIC outputs forces to use Kapton flexible flat cable
- Kapton cable has large capacitance

⇓

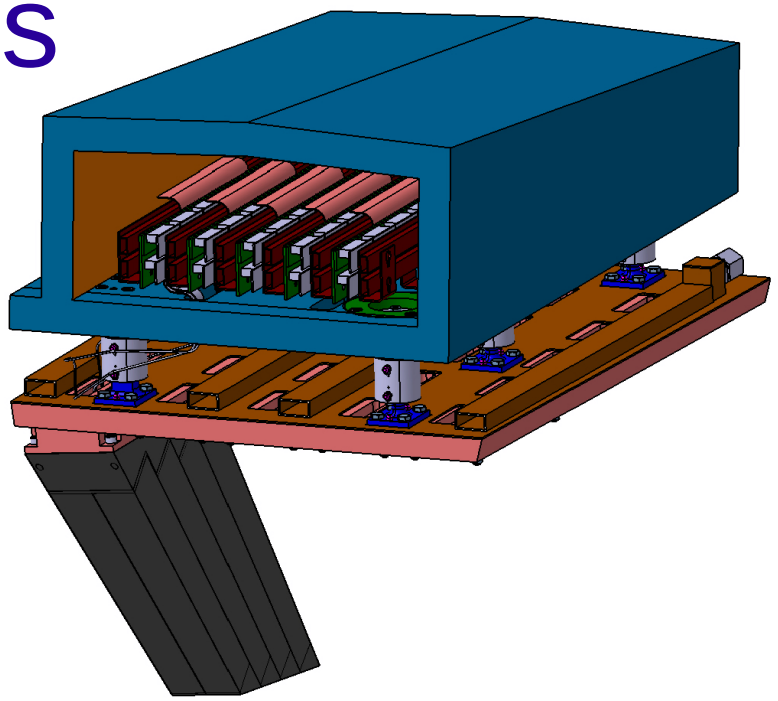
Limited band width





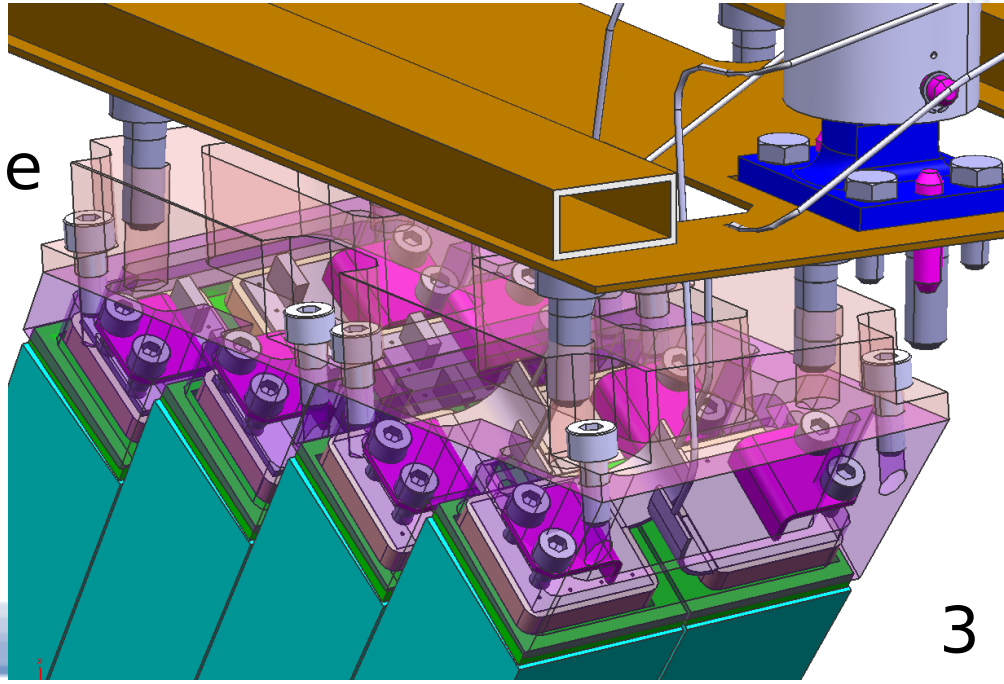
ASIC Integration Challenges

Limited band width

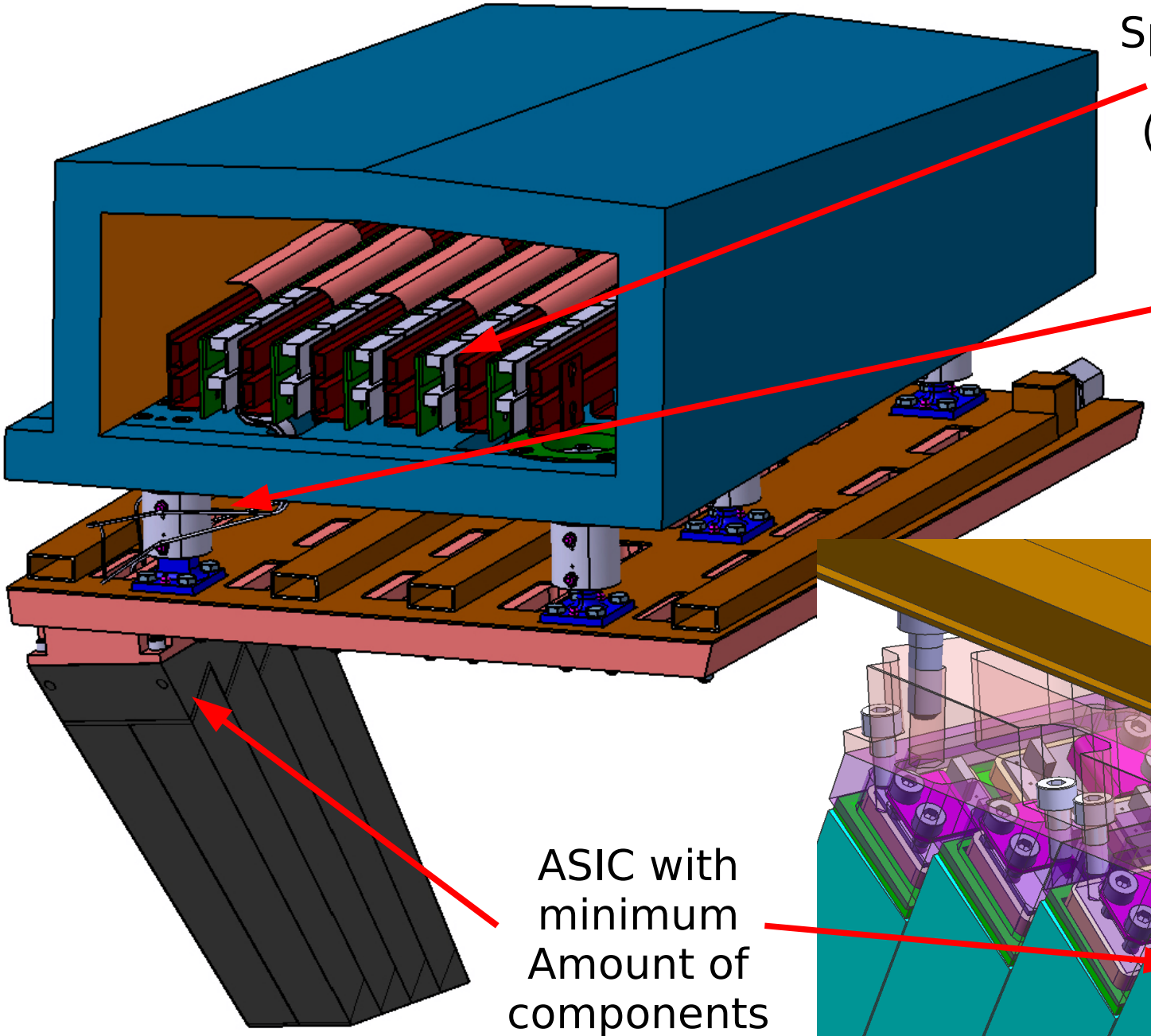


Solutions:

- Reduce length of the Kapton cable and to put additional line driver close to ASIC – no space
- Build low-ohmic line driver into the ASIC – 10× increase of power consumption
- Use different types of the cable between ASIC and SADC – complicated connector in the cold area



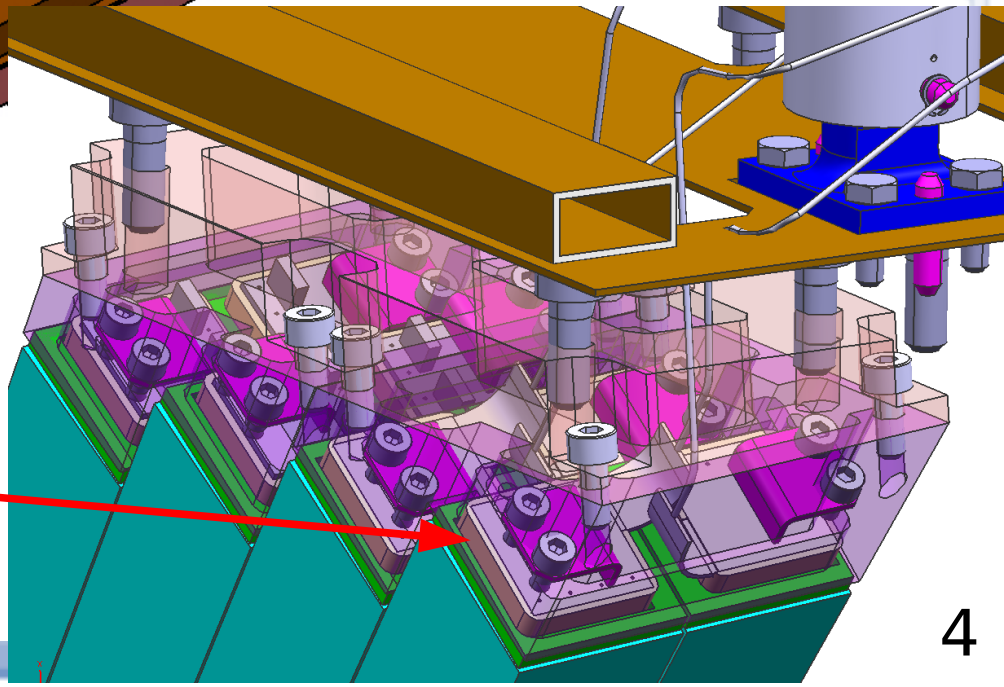
Available Space



Space for additional Electronics (line driver/SADC)

Cable ~**300 mm** long

ASIC with minimum Amount of components



To Be Investigated

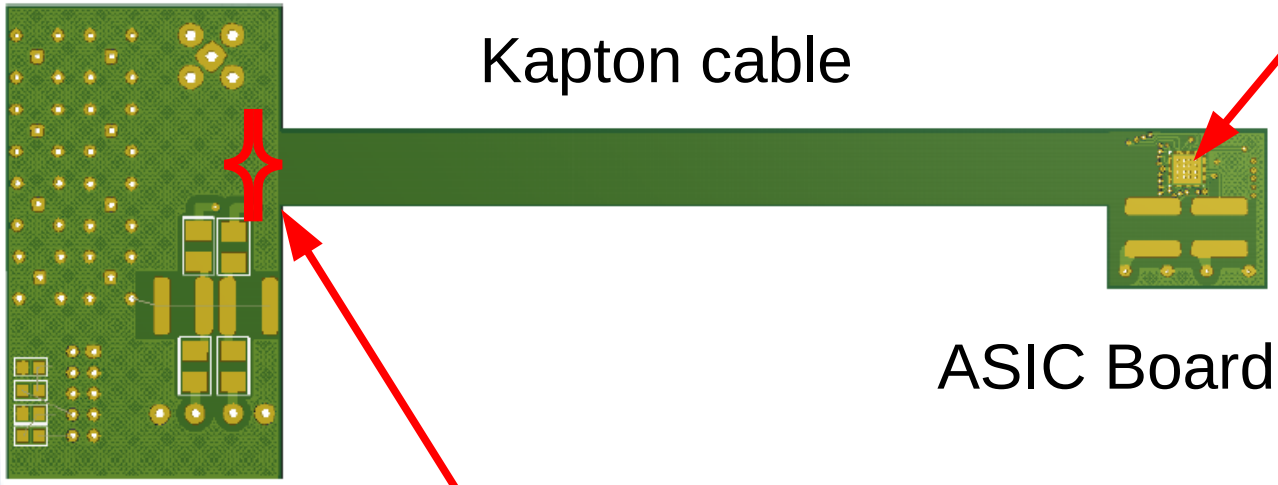
- Performance of the current APFEL ASIC with reasonably long Kapton cable (~150 mm)
- Design of the additional line driver
- The effect of additional cable between the ASIC and line driver

ASIC board has to have flexible design

ASIC Board

HV filter/Line driver Board (debugging version)

Mounting pad for ASIC



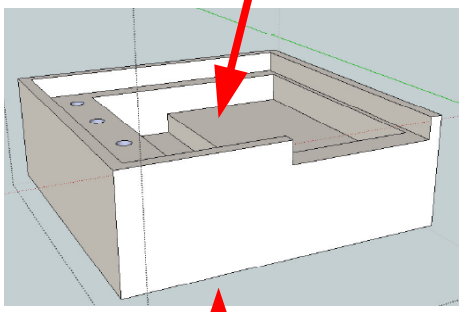
Kapton cable

ASIC Board

Possibility to break the board and mount a connector

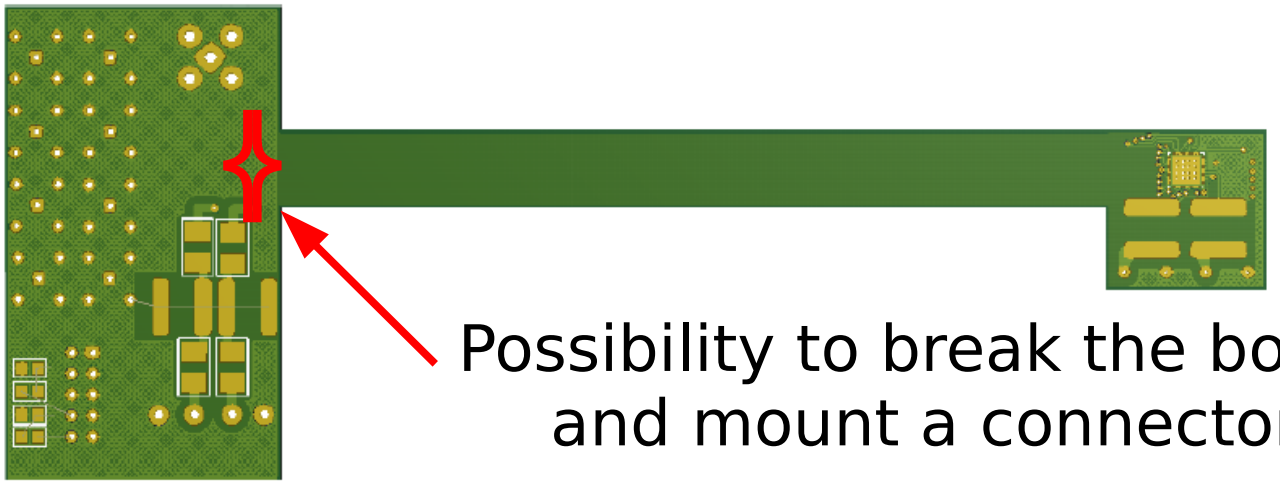
Space for the ASIC board

LAAPD capsule



LAAPD inserted From the bottom

ASIC Board



Separation of the line-driver board from ASIC board will allow:

- To investigate the effect of the connector
- To try different designs of the line-driver board (simple/smaller)

→ Test effect of the additional cable between ASIC board and line driver

ASIC Board
(current status)

- ✓ The design of the capsule part and cable is ready
- ✓ The design of the Line-driver part is finished
- → The design is adapted for prototype production; we are in contact with two companies:
  - ✗ Thales Nederland B.V. (www.thales-nederland.nl) – can not produce the board (too challenging)
  - → GS-swiss PCB AG (www.swisspcb.ch) – for prototype and mass production
- We expect to have boards produced in October-November

ASIC Development

(on behalf of Peter Wieczorek, GSI)

- The APFEL-III ASIC will be submitted for production in October-November
- Before submission we have to decide on the parameters of ASIC build-in line driver (optimize for the Kapton cable)

- Test setup of 4×4 crystals equipped with ASIC APFEL-II ASIC preamplifiers is being built at GSI (first measurements October). The Goals:
  - Investigate APFEL-II performance with cosmic rays/beams in the close to ideal environment (no Kapton cable)

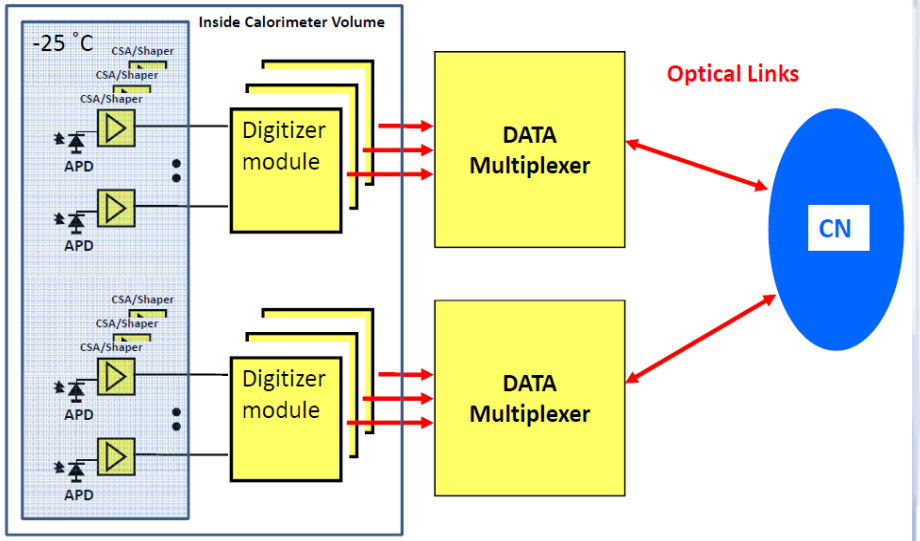
Feature Extraction Algorithms
(VHDL implementation)

At present:

- All test measurements done with SADC (~10 μs long traces are stored for each event)
- Feature extraction algorithms implemented in software (C++ programs) and tested on collected data

- Feature extraction algorithm should analyse data on-line on digitizer module (FPGA)
- No prototype of PANDA Digitizer is available

Data-collection chain

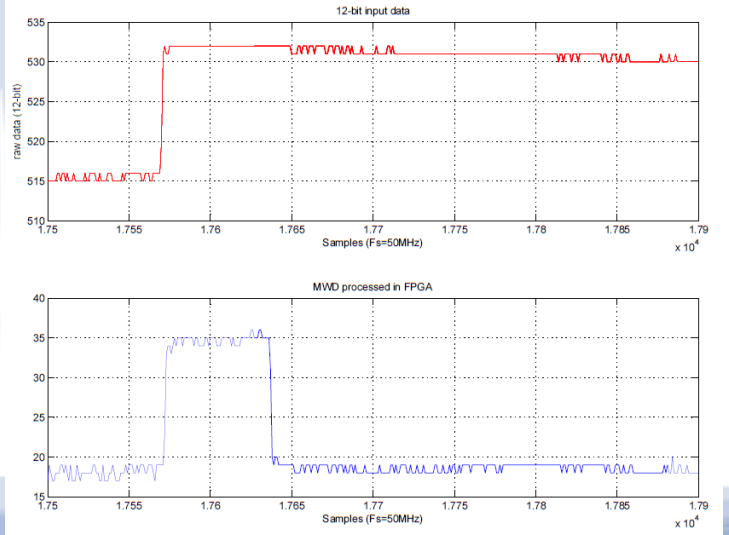


Feature Extraction Algorithms
(VHDL implementation)

PANDA SADC prototypes:

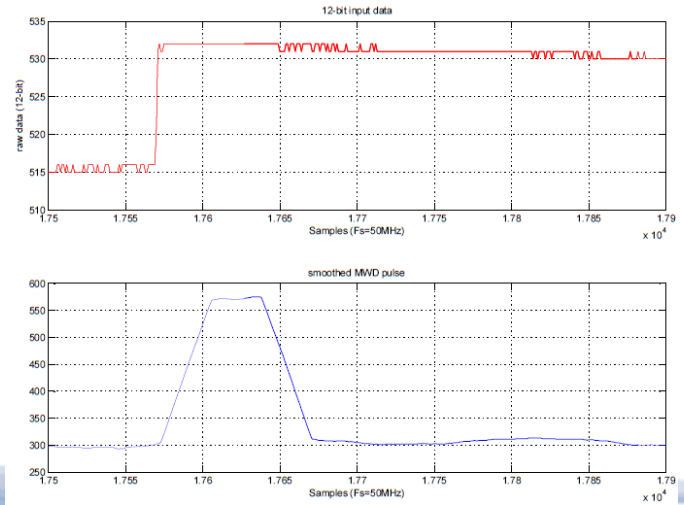
- PANDA SADC prototype (Pawel Marciniewski, Uppsala):
  - 16 channels, 14 bit, >100 MHz, optical link output
  - Available next year
- FEBEX 1/16 SADC developed at GSI (Jan Hoffman)
  - 16 channels, 12 bit, 67 MHz, optical link output
  - Board available in October

Using FPGA development board to analyse measured data:



Measured data

Intermediate output from FPGA



Feature Extraction Algorithms
(VHDL implementation)

VHDL implementation status and perspective:

- Analysis of measured data using FPGA test board – almost ready
- “Porting” feature extraction algorithm to FEBEX 1/16 SADC board – beginning of 2010
- “Porting” for PANDA SADC prototype – second part of 2010

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Thank You for Your Attention!